Features

- Temperature Proportional Fan Speed for Reduced Acoustic Noise and Longer Fan Life
- FanSense™ Protects against Fan Failure and Eliminates the Need for 3-wire Fans
- Over Temperature Detection (TC665)
- Efficient PWM Fan Drive
- Provides RPM Data
- 2-Wire SMBus™-Compatible Interface
- Supports Any Fan Voltage
- Software Controlled Shutdown Mode for "Green" Systems
- Supports Low Cost NTC/PTC Thermistors
- Space Saving 10-Pin MSOP Package
- Temperature Range: -40°C to +85°C

Applications

- Personal Computers & Servers
- LCD Projectors
- Datacom & Telecom Equipment
- Fan Trays
- File Servers
- Workstations
- General Purpose Fan Speed Control

Package Type

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN</td>
</tr>
<tr>
<td>2</td>
<td>CF</td>
</tr>
<tr>
<td>3</td>
<td>SCLK</td>
</tr>
<tr>
<td>4</td>
<td>SDA</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>FAULT</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
</tr>
<tr>
<td>8</td>
<td>SENSE</td>
</tr>
<tr>
<td>9</td>
<td>VOUT</td>
</tr>
<tr>
<td>10</td>
<td>VDD</td>
</tr>
</tbody>
</table>

Description

The TC664/TC665 devices are PWM mode fan speed controllers with FanSense technology for use with brushless DC fans. These devices implement temperature proportional fan speed control which lowers acoustic fan noise and increases fan life. The voltage at \( V_{IN} \) (Pin 1) represents temperature and is typically provided by an external thermistor or voltage output temperature sensor. The PWM output \( (V_{OUT}) \) is adjusted between 30% and 100%, based on the voltage at \( V_{IN} \). The PWM duty cycle can also be programmed via SMBus to allow fan speed control without the need for an external thermistor. If \( V_{IN} \) is not connected, the TC664/TC665 will start driving the fan at a default duty cycle of 39.33%. See Section 4.3, "Fan Startup", for more details.

In normal fan operation, a pulse train is present at the SENSE pin (Pin 8). The TC664/TC665 use these pulses to calculate the fan revolutions per minute (RPM). The fan RPM data is used to detect a worn out, stalled, open or unconnected fan. An RPM level below the user-programmable threshold causes the TC664/TC665 to assert a logic low alert signal (FAULT). The default threshold value is 500 RPM. Also, if this condition occurs, FF (bit 0<0>) in the Status Register will also be set to a '1'.

An over-temperature condition is indicated when the voltage at \( V_{IN} \) exceeds 2.6 V (typical). The TC664/TC665 devices indicate this by setting OTF(bit 5<X>) in the Status Register to a '1'. The TC665 device also pulls the FAULT line low during an over-temperature condition.

The TC664/TC665 devices are available in a 10-Pin MSOP package and consume 150 µA during operation. The devices can also enter a low-power shutdown mode (5 µA, typ.) by setting the appropriate bit in the Configuration Register. The operating temperature range for these devices is -40°C to +85°C.

SMBus is a trademark of Intel Corporation
Note: OTF condition applies for the TC665 device only.
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings *

- $V_{DD}$ .......................................................... 6.5 V
- Input Voltages ........................................... -0.3 V to $(V_{DD} + 0.3 \text{ V})$
- Output Voltages ........................................... -0.3 V to $(V_{DD} + 0.3 \text{ V})$
- Storage temperature .................................. -65°C to +150°C
- Ambient temp. with power applied .............. -40°C to +125°C
- Maximum Junction Temperature, $T_J$ .............. 150°C

*Notice: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise noted, all limits are specified for $V_{DD} = 3.0 \text{ V} \text{ to } 5.5 \text{ V}$, $-40^\circ \text{C} < T_A < +85^\circ \text{C}$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage $V_{DD}$</td>
<td></td>
<td>3.0</td>
<td></td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating Supply Current $I_{DD}$</td>
<td></td>
<td>150</td>
<td></td>
<td>300</td>
<td>$\mu A$</td>
<td>Pins 8, 9 Open</td>
</tr>
<tr>
<td>Shutdown Mode Supply Current $I_{DDSHDN}$</td>
<td></td>
<td>5</td>
<td></td>
<td>10</td>
<td>$\mu A$</td>
<td>Pins 8, 9 Open</td>
</tr>
</tbody>
</table>

**VOUT PWM Output**

- $V_{OUT}$ Rise Time $t_R$ ................. — | — | 50 | $\mu s e c$ | $I_{OH} = 5 \text{ mA, Note 1}$
- $V_{OUT}$ Fall Time $t_F$ ................. — | — | 50 | $\mu s e c$ | $I_{OL} = 1 \text{ mA, Note 1}$
- Sink Current at $V_{OUT}$ Output $I_{OL}$ | 1.0 | — | — | mA | $V_{OL} = 10\% \text{ of } V_{DD}$
- Source Current at $V_{OUT}$ Output $I_{OH}$ | 5.0 | — | — | mA | $V_{OH} = 80\% \text{ of } V_{DD}$
- PWM Frequency $F$ ........................... 26 | 30 | 34 | Hz  | $C_F = 1 \mu F$             

**VIN Input**

- $V_{IN}$ Input Voltage for 100% PWM duty-cycle $V_{CMAX}$ | 2.45 | 2.6 | 2.75 | V |
- $V_{CMAX} - V_{CMIN}$ $V_{CRANGE}$ | 1.25 | 1.4 | 1.55 | V |
- $V_{IN}$ Input Resistance .................. — | 10M | — | $\Omega$ | $V_{DD} = 5.0 \text{ V}$
- $V_{IN}$ Input Leakage Current $I_{IN}$ | 1.0 | — | — | $\mu A$ |

**SENSE Input**

- SENSE Input Threshold Voltage with Respect to GND $V_{THSENSE}$ | 80 | 100 | 120 | mV |

**FAULT Output**

- FAULT Output LOW Voltage $V_{OL}$ | — | — | 0.3 | V | $I_{OL} = 2.5 \text{ mA}$
- FAULT Output Response Time $t_{FAULT}$ | — | 2.4 | — | sec |

**Fan RPM-to-Digital Output**

- Fan RPM ERROR ............................... -15 | — | +15 | % | RPM > 1600 |

2-Wire Serial Bus Interface

- Logic Input High $V_{IH}$ .......................... 2.1 | — | — | V  | Note 2 |
- Logic Input Low $V_{IL}$ .......................... — | — | 0.8 | V  |
- Logic Output Low $V_{OL}$ .......................... — | — | 0.4 | V  | $I_{OL} = 3 \text{ mA}$
- Input Capacitance SDA, SCLK $C_{IN}$ | — | 10 | 15 | pF  | Note 1 |
- I/O Leaks Current $I_{LEAK}$ | -1.0 | — | — | $\mu A$ |
- SDA Output Low Current $I_{OLSDA}$ | 6 | — | — | mA  | $V_{OL} = 0.6 \text{ V}$ |

**Note 1:** Not production tested, ensured by design, tested during characterization.

**Note 2:** For $5.0 \text{ V} < V_{DD} \leq 5.5 \text{ V}$, the limit for $V_{IH} = 2.2 \text{ V}$. 

© 2002 Microchip Technology Inc.
## TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at $V_{DD} = 3.0\, V$ to $5.5\, V$

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Ranges:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specified Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td></td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td></td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_A$</td>
<td>-65</td>
<td></td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

**Thermal Package Resistances:**

| Thermal Resistance, 10 Pin MSOP | $\theta_{JA}$ | —   | 113 | —   | °C/W |

## TIMING SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise noted, all limits are specified for $V_{DD} = 3.0\, V$ to $5.5\, V$, $-40°C < T_A < +85°C$

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBus Interface (See Figure 1-1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial Port Frequency</td>
<td>$f_{SC}$</td>
<td>0</td>
<td>—</td>
<td>100</td>
<td>kHz</td>
<td>Note 1</td>
</tr>
<tr>
<td>Low Clock Period</td>
<td>$t_{LOW}$</td>
<td>4.7</td>
<td>—</td>
<td>—</td>
<td>µsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>High Clock Period</td>
<td>$t_{HIGH}$</td>
<td>4.7</td>
<td>—</td>
<td>—</td>
<td>µsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>SCLK and SDA Rise Time</td>
<td>$t_R$</td>
<td>—</td>
<td>—</td>
<td>1000</td>
<td>nsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>SCLK and SDA Fall Time</td>
<td>$t_F$</td>
<td>—</td>
<td>—</td>
<td>300</td>
<td>nsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>Start Condition Setup Time</td>
<td>$t_{SU(START)}$</td>
<td>4.7</td>
<td>—</td>
<td>—</td>
<td>µsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>SCLK Clock Period Time</td>
<td>$t_{SC}$</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>µsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>Start Condition Hold Time</td>
<td>$t_{H(START)}$</td>
<td>4.0</td>
<td>—</td>
<td>—</td>
<td>µsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>Data in Setup Time to SCLK High</td>
<td>$t_{SU-DATA}$</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>nsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>Data in Hold Time after SCLK Low</td>
<td>$t_{H-DATA}$</td>
<td>300</td>
<td>—</td>
<td>—</td>
<td>nsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>Stop Condition Setup Time</td>
<td>$t_{SU(STOP)}$</td>
<td>4.0</td>
<td>—</td>
<td>—</td>
<td>µsec</td>
<td>Note 1</td>
</tr>
<tr>
<td>Bus Free Time Prior to New</td>
<td>$t_{IDLE}$</td>
<td>4.7</td>
<td>—</td>
<td>—</td>
<td>µsec</td>
<td>Note 1 and Note 2</td>
</tr>
<tr>
<td>Transition</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Not production tested, ensured by design, tested during characterization.

**Note 2:** Time the bus must be free before a new transmission can start.
FIGURE 1-1: Bus Timing Data.
2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.
FIGURE 2-7:  SDA \( I_{OL} \) vs. Temperature.

FIGURE 2-8:  \( V_{CMAX} \) vs. Temperature.

FIGURE 2-9:  \( V_{CMIN} \) vs. Temperature.

FIGURE 2-10:  RPM \% error vs. Temperature.

FIGURE 2-11:  Sense Threshold (\( V_{THSENSE} \)) Hysteresis vs. Temperature.

FIGURE 2-12:  SDA, SCLK Hysteresis vs. Temperature.
3.0 PIN FUNCTIONS
The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Analog Input</td>
</tr>
<tr>
<td>CF</td>
<td>Analog Output</td>
</tr>
<tr>
<td>SCLK</td>
<td>Serial Clock Input</td>
</tr>
<tr>
<td>SDA</td>
<td>Serial Data In/Out (Open Drain)</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>FAULT</td>
<td>Digital (Open Drain) Output</td>
</tr>
<tr>
<td>NC</td>
<td>No Connection</td>
</tr>
<tr>
<td>SENSE</td>
<td>Analog Input</td>
</tr>
<tr>
<td>VOUT</td>
<td>Digital Output</td>
</tr>
<tr>
<td>VDD</td>
<td>Power Supply Input</td>
</tr>
</tbody>
</table>

3.1 Analog Input (VIN)
A voltage range of 1.62 V to 2.6 V (typical) on this pin drives an active duty-cycle of 30% to 100% on the VOUT pin.

3.2 Analog Output (CF)
Positive terminal for the PWM ramp generator timing capacitor. The recommended CF is 1 μF for 30 Hz PWM operation.

3.3 SMBus Serial Clock Input (SCLK)
Clocks data into and out of the TC664/TC665. See Section 5.0 for more information on the serial interface.

3.4 Serial Data (Bi-directional) (SDA)
Serial data is transferred on the SMBus in both directions using this pin. See Section 5.0 for more information on the serial interface.

3.5 Digital (Open Drain) Output (FAULT)
When the fan’s RPM falls below the user-set RPM threshold (or OTF occurs with TC665), a logic low signal is asserted.

3.6 Analog Input (SENSE)
Fan current pulses are detected at this pin. These pulses are counted and used in the calculation of the fan RPM.

3.7 Digital Output (VOUT)
This active high complimentary output drives the base of an external transistor or the gate of a MOSFET.

3.8 Power Supply Input (VDD)
The VDD pin with respect to GND provides power to the device. This bias supply voltage may be independent of the fan power supply.
4.0 DEVICE OPERATION

The TC664/TC665 devices allow you to control, monitor and communicate (via SMBus) fan speed for 2-wire and 3-wire DC brushless fans. By pulse width modulating (PWM) the voltage across the fan, the TC664/TC665 controls fan speed according to the system temperature. The goal of temperature proportional fan speed control is to reduce fan power consumption, increase fan life and reduce system acoustic noise. With the TC664/TC665 devices, fan speed can be controlled by the analog input V_IN or the SMBus interface, allowing for high system flexibility.

The TC664/TC665 devices also measure and monitor fan revolutions per minute (RPM). A fan's speed (RPM) is a measure of its health. As a fan's bearings wear out, the fan slows down and eventually stops (locked rotor). By monitoring the fan's RPM level, the TC664/TC665 devices can detect open, shorted, unconnected and locked rotor fan conditions. The fan speed threshold can be set to provide a predictive fan failure feature. This feature can be used to give a system warning and, in many cases, help to avoid a system thermal shut-down condition. The fan RPM data and threshold registers are available over the SMBus interface which allows for complete system control.

The TC664/TC665 devices are identical in every aspect except for how they indicate an over-temperature condition. When V_IN voltage exceeds 2.6 V (typical), both devices will set OTF (bit 5<X>) in the Status Register to a '1'. The TC665 will additionally pull the FAULT output low during an over-temperature condition.

![FIGURE 4-1: Typical Application Circuit.](image-url)
4.1 Fan Speed Control Methods

The speed of a DC brushless fan is proportional to the voltage across it. For example, if a fan's rating is 5000 RPM at 12 V, its speed would be 2500 RPM at 6 V. This, of course, will not be exact, but should be close.

There are two main methods for fan speed control. The first is pulse width modulation (PWM) and the second is linear. Using either method the total system power requirement to run the fan is equal. The difference between the two methods is where the power is consumed.

The following example compares the two methods for a 12 V, 120 mA fan running at 50% speed. With 6 V applied across the fan, the fan draws an average current of 68 mA. Using a linear control method, there is 6V across the fan and 6V across the drive element. With 6 V and 68 mA, the drive element is dissipating 410 mW of power. Using the PWM approach, the fan is modulated at a 50% duty cycle, with most of the 12 V being dropped across the fan. With 50% duty cycle, the fan draws an RMS current of 110 mA and an average current of 72 mA. Using a MOSFET with a 1 Ω \( R_{DS(on)} \) (a fairly typical value for this low current) the power dissipation in the drive element would be: 12 mW \( (I_{rms}^2 \times R_{DS(on)}) \). Using a standard 2N2222A NPN transistor (assuming a \( V_{ce-sat} \) of 0.8 V), the power dissipation would be 58 mW \( (I_{avg} \times V_{ce-sat}) \).

The PWM approach to fan speed control causes much less power dissipation in the drive element. This allows smaller devices to be used and will not require any special heatsinking to get rid of the power being dissipated in the package.

The other advantage to the PWM approach is that the voltage being applied to the fan is always near 12 V. This eliminates any concern about not supplying a high enough voltage to run the internal fan components which is very relevant in linear fan speed control.

4.2 PWM Fan Speed Control

The TC664/TC665 devices implement PWM fan speed control by varying the duty cycle of a fixed frequency pulse train. The duty cycle of a waveform is the on time divided by the total period of the pulse. For example, given a 100 Hz waveform (10 msec.) with an on time of 5.0 msec., the duty cycle of this waveform is 50% \( (5.0 \text{ msec.} / 10.0 \text{ msec.}) \). An example of this is shown in Figure 4-2.

![FIGURE 4-2: Duty Cycle Of A PWM Waveform.](image)

The TC664/TC665 devices generate a pulse train with a typical frequency of 30 Hz \( (C_f = 1 \mu F) \). The duty cycle can be varied from 30% to 100%. The pulse train generated by the TC664/TC665 devices drives the gate of an external N-channel MOSFET or the base of an NPN transistor (Figure 4-3). See Section 7.5 for more information on output drive device selection.

![FIGURE 4-3: PWM Fan Drive.](image)

By modulating the voltage applied to the gate of the MOSFET \( Q_{drive} \), the voltage applied to the fan is also modulated. When the \( V_{OUT} \) pulse is high, the gate of the MOSFET is turned on, pulling the voltage at the drain of \( Q_{drive} \) to zero volts. This places the full 12 V across the fan for the \( Ton \) period of the pulse. When the duty cycle of the drive pulse is 100% \( (\text{full on, } Ton = T) \), the fan will run at full speed. As the duty cycle is decreased \( (\text{pulse on time } "Ton" \text{ is lowered}) \), the fan will slow down proportionally. With the TC664/TC665 devices, the duty cycle can be controlled through the analog input pin \( V_{IN} \), or through the SMBus interface, by using the Duty-Cycle Register. See Section 4.5 for more details on duty cycle control.
4.3 Fan Startup

Often overlooked in fan speed control is the actual startup control period. When starting a fan from a non-operating condition (fan speed is zero RPM), the desired PWM duty cycle or average fan voltage cannot be applied immediately. Since the fan is at a rest position, the fan's inertia must be overcome to get it started. The best way to accomplish this is to apply the full rated voltage to the fan for one second. This will ensure that in all operating environments, the fan will start and operate properly.

The TC664/TC665 devices implement this fan control feature without any user programming. During a power up or release from shutdown condition, the TC664/TC665 devices force the VOUT output to a 100% duty cycle, turning the fan full on for one second (C_F = 1.0 µF). Once the one second period is over, the TC664/TC665 devices will look to see if SMBus or VIN control has been selected in the Configuration Register (DUTYC bit 5<0>). Based on this register, the device will choose which input will control the VOUT duty cycle. Duty cycle control based on VIN is the default state. If VIN control is selected and the VIN pin is open (nothing is connected to the VIN pin), then the TC664/TC665 will default to a duty cycle of 39.33%. This sequence is shown in Figure 4-4. This integrated one second startup feature will ensure the fan starts up every time.

![FIGURE 4-4: Power-up Flow Chart.](image)

4.4 PWM Drive Frequency (C_F)

As previously discussed, the TC664/TC665 devices operate with a fixed PWM frequency. The frequency of the PWM drive output (VOUT) is set by a capacitor at the C_F pin. With a 1 µF capacitor at the C_F pin, the typical drive frequency is 30 Hz. This frequency can be raised, by decreasing the capacitor value, or lowered, by increasing the capacitor value. The relationship between the capacitor value and the PWM frequency is linear. If a frequency of 15 Hz is desired, a capacitor value of 2.0 µF should be used. The frequency should be kept in the range of 15 Hz to 35 Hz. See Section 7.2 for more details.

4.5 Duty Cycle Control (V_IN and Duty-Cycle Register)

The duty cycle of the VOUT PWM drive signal can be controlled by either the VIN analog input pin or by the Duty-Cycle Register, which is accessible via the SMBus interface. The control method is selectable via DUTYC (bit 5<0>) of the Configuration Register. The default state is for VIN control. If VIN control is selected and the VIN pin is open, the PWM duty cycle will default to 39.33%. The duty cycle control method can be changed at any time via the SMBus interface.

VIN is an analog input pin. A voltage in the range of 1.62 V to 2.6 V (typical) at this pin commands a 30% to 100% duty cycle on the VOUT output, respectively. If the voltage at VIN falls below the 1.62 V level, the duty cycle will not go below 30%. The relationship between the voltage at VIN and the PWM duty cycle is shown in Figure 4-5.

![FIGURE 4-5: PWM Duty Cycle vs. Input Voltage, VIN (Typical).](image)

For the TC665 device, if the voltage at VIN exceeds the 2.6 V (typical) level, an over temperature fault indication will be given by asserting a low at the FAULT output and setting OTF (bit 5<X>) in the Status Register to a ‘1’.

A thermistor network or any other voltage output thermal sensor can be used to provide the voltage to the VIN input. The voltage supplied to the VIN pin can actually be thought of as a temperature. For example, the circuit shown in Figure 4-6 represents a typical solution for a thermistor based temperature sensing network. See Section 7.3 for more details.
The second method for controlling the duty cycle of the PWM output (V\text{OUT}) is via the SMBus interface. In order to control the PWM duty cycle via the SMBus, DUTYC (bit 5<0>) of the Configuration Register (Register 6.3) must be set to a ‘1’. This tells the TC664/TC665 device that the duty cycle should be controlled by the Duty Cycle Register. Next, the Duty Cycle Register must be programmed to the desired value. The Duty Cycle Register is a 4 Bit read/write register that allows duty cycles from 30% to 100% to be programmed. Table 4-1 shows the binary codes for each possible duty cycle.

TABLE 4-1: DUTY-CYCLE REGISTER (DUTY-CYCLE) 4-BITS, READ/WRITE

<table>
<thead>
<tr>
<th>Duty-Cycle Register (Duty Cycle)</th>
<th>D(3)</th>
<th>D(2)</th>
<th>D(1)</th>
<th>D(0)</th>
<th>Duty-Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>30%</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>34.67%</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>39.33%</td>
</tr>
<tr>
<td>(default for V\text{IN} open and when SMBus is not selected)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>44%</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>48.67%</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>53.33%</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>58%</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>62.67%</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>67.33%</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>72%</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>76.67%</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>81.33%</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>86%</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>90.67%</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>95.33%</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>100%</td>
</tr>
</tbody>
</table>

This method of control allows for more sophisticated algorithms to be implemented by utilizing microcontrollers or microprocessors in the system. In this way, multiple system temperatures can be taken into account for determining the necessary fan speed.

As shown in Table 4-1, the duty cycle has more of a step function look than did the \text{V_IN} control approach. Because the step changes in duty cycle are small, they are rarely audibly noticeable, especially when the fans are integrated into the system.

4.6 PWM Output (V\text{OUT})

The V\text{OUT} pin is designed to drive a low cost NPN transistor or N-channel MOSFET as the low side switching element in the system, as is shown in Figure 4-7. The switching element is used to turn the fan on and off at the PWM duty cycle commanded by the V\text{OUT} output. This output has complementary drive (pull up and pull down) and is optimized for driving NPN transistors or N-channel MOSFETs (see typical characteristic curves for sink and source current capability of the V\text{OUT} drive stage).

The external device needs to be chosen to fit the voltage and current rating of the fan in a particular application (Refer to Section 7.5 Output Drive Device Selection). NPN transistors are often a good choice for low current fans. If a NPN transistor is chosen, a base current limiting resistor should be used. When using a MOSFET as the switching element, it is sometimes a good idea to have a gate resistor to help slow down the turn on and turn off of the MOSFET. As with any switching waveform, fast rising and falling edges can sometimes lead to noise problems.

As previously stated, the V\text{OUT} output will go to 100% duty cycle during power up and release from shutdown conditions. The V\text{OUT} output only shuts down when commanded to do so via the Configuration Register (SDM (bit 0<0>). Even when a locked rotor condition is detected, the V\text{OUT} output will continue to pulse at the programmed duty cycle.

4.7 Sensing Fan Operation (SENSE)

The TC664/TC665 devices also feature Microchip’s proprietary FanSense technology. During normal fan operation, commutation occurs as each pole of the fan is energized. The fan current pulses created by the fan commutation are sensed using a low value current sense resistor in the ground return leg of the fan circuit. The voltage pulses across the sense resistor are then AC coupled through a capacitor to the SENSE pin of the TC664/TC665 device. These pulses are utilized for calculating the RPM of the fan. The threshold voltage for the SENSE pin is 100 mV (typical). The peak of the voltage pulse at the SENSE pin must exceed the 100 mV (typical) threshold in order for the pulse to be counted in the fan RPM measurement.
See Section 7.4 for more details on selecting the appropriate current sense resistor and coupling capacitor values.

FIGURE 4-7: Fan Current Sensing.

By selecting FPPR (bits 2-1<01>) in the Configuration Register, the TC664/TC665 devices can be programmed to calculate RPM data for fans with 1, 2, 4 or 8 current pulses per rotation. The default state assumes a fan with 2 pulses per rotation.

The measured RPM data is then stored in the RPM-OUTPUT (RPM) Register. This register is a 9-Bit read-only register which stores RPM data with 25 RPM resolution. By setting RES (bit 6<0>) of the Configuration Register to a ‘1’, the RPM data can be read with 25 RPM resolution. If this bit is left in the default state of ‘0’, the RPM data will only be readable with resolution of 50 RPMs, which represents 8-bit data.

The maximum fan RPM reading is 12775 RPM. If this value is exceeded, a counter overflow bit in the Status Register is set. RCO (bit 3<0>) in the Status Register represents the RPM counter overflow bit for the RPM-OUTPUT Register. This bit will automatically be reset to zero if the fan RPM reading has been below the maximum value of 12775 RPM for 2.4 seconds.

See Table 6-1 for RPM and Status Register command byte assignments.

4.8 Fan Fault Threshold and Indication (FAULT)

For the TC664/TC665 devices, a fault condition exists whenever a fan’s sensed RPM level falls below the user programmable threshold. The RPM threshold value for fan fault detection is set in the FAN_FAULT Register (8-bit, read/write).

The RPM threshold represents the fan speed at which the TC664/TC665 devices will indicate a fan fault. This threshold can be set at lower levels to indicate fan locked rotor conditions, or set to higher levels to give indications for predictive fan failure. It is recommended that the RPM threshold be at least 10% lower than the minimum fan speed which occurs at the lowest duty cycle set point. The default value for the fan RPM threshold is 500 RPM. If the fan’s sensed RPM is less than the fan fault threshold for 2.4 seconds (typical), a fan fault condition is indicated.

When a fault condition, due to low fan RPM, occurs, a logic low is asserted at the FAULT output and the FF (bit 0<0>) in the Status Register is set to ‘1’. The FAULT output and the fault bit in the Status Register can be reset by setting FFCLR (bit 7<0>) in the Configuration Register to a ‘1’.

For the TC665 device, a fault condition is also indicated when an Over Temperature Fault condition occurs. This condition occurs when the V_OUT duty cycle exceeds the 100% value, indicating that no additional cooling capability is available. For this condition, a logic low is asserted at the FAULT output and OTF (bit 5<X>) of the Status Register, the over temperature fault indicator, is set to a ‘1’ (The TC664 also indicates an over temperature condition via the OTF bit in the status register). If the duty cycle then decreases below 100%, the FAULT output will be released and OTF (bit 5<X>) of the Status Register will be reset to ‘0’.

4.9 Low Power Shutdown Mode

Some applications may have operating conditions where fan cooling is not required as a result of low ambient temperature or light system load. During these times it may be desirable to shut the fans down to save power and reduce system noise.

The TC664/TC665 devices can be put into a low power shutdown mode by setting SDM (bit 0<0>) in the Configuration Register to a ‘1’ (this bit is the shutdown bit). When the TC664/TC665 devices are in shutdown mode, all functions except for the SMBus interface are suspended. During this mode of operation, the TC664 and TC665 devices will draw a typical supply current of only 5 µA. Normal operation will resume as soon as Bit 0 in the Configuration Register is reset to ‘0’.

When the TC664/TC665 devices are brought out of a shutdown mode by resetting SDM (bit 0<0>) in the Configuration Register, all of the registers, except for the Configuration and FAN_FAULT Registers assume
their default power up states. The Configuration Register and the FAN_FAULT Register maintain the states they were in prior to the device being put into the shutdown mode. Since these are the registers which control the parts operation, the part does not have to be reprogrammed for operation when it comes out of shutdown mode.

4.10 SMBus Interface (SCLK & SDA)

The TC664/TC665 feature an industry standard, 2-wire serial interface with factory-set addresses. By communicating with the TC664/TC665 device's registers, functions like PWM duty cycle, low power shutdown mode and fan RPM threshold can be controlled. Critical information, such as fan fault, over temperature and fan RPM, can also be obtained via the device data registers. The available data and control registers make the TC664/TC665 devices very flexible and easy to use. All of the available registers are detailed in Section 6.0.

4.11 SMBus Slave Address

The slave address of the TC664/TC665 devices is 0011 011. This is a fixed address. This address is different from industry-standard digital temperature sensors (like the TCN75) and, therefore, allows the TC664/TC665 to be utilized in systems in conjunction with these components. Please contact Microchip Technology if alternate addresses are required.
5.0 SERIAL COMMUNICATION

5.1 SMBus 2-Wire Interface

The Serial Clock Input (SCLK) and the bi-directional data port (SDA) form a 2-wire bi-directional serial port for communicating with the TC664/TC665. The following bus protocols have been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following Serial Bus conventions have been defined.

**TABLE 5-1: TC664/TC665 SERIAL BUS CONVENTIONS**

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td>The device sending data to the bus.</td>
</tr>
<tr>
<td>Receiver</td>
<td>The device receiving data from the bus.</td>
</tr>
<tr>
<td>Master</td>
<td>The device which controls the bus: initiating transfers (START), generating the clock and terminating transfers (STOP).</td>
</tr>
<tr>
<td>Slave</td>
<td>The device addressed by the master.</td>
</tr>
<tr>
<td>Start</td>
<td>A unique condition signaling the beginning of a transfer indicated by SDA falling (High to Low) while SCLK is high.</td>
</tr>
<tr>
<td>Stop</td>
<td>A unique condition signaling the end of a transfer indicated by SDA rising (Low to High) while SCLK is high.</td>
</tr>
<tr>
<td>ACK</td>
<td>A Receiver acknowledges the receipt of each byte with this unique condition. The Receiver pulls SDA low during SCLK high of the ACK clock-pulse. The Master provides the clock pulse for the ACK cycle.</td>
</tr>
<tr>
<td>Busy</td>
<td>Communication is not possible because the bus is in use.</td>
</tr>
<tr>
<td>NOT Busy</td>
<td>When the bus is idle, both SDA and SCLK will remain high.</td>
</tr>
<tr>
<td>Data Valid</td>
<td>The state of SDA must remain stable during the high period of SCLK in order for a data bit to be considered valid. SDA only changes state while SCLK is low during normal data transfers. (See START and STOP conditions)</td>
</tr>
</tbody>
</table>

5.1.1 DATA TRANSFER

The TC664/TC665 support a bi-directional 2-Wire bus and data transmission protocol. The serial protocol sequencing is illustrated in Figure 1-1. Data transfers are initiated by a start condition (START), followed by a device address byte and one or more data bytes. The device address byte includes a Read/Write selection bit. Each access must be terminated by a Stop Condition (STOP). A convention call Acknowledge (ACK) confirms the receipt of each byte. Note that SDA can only change during periods when SCLK is LOW (SDA changes while SCLK is HIGH are reserved for Start and Stop conditions). All bytes are transferred MSB (most significant bit) first.

5.1.2 MASTER/SLAVE

The device that sends data onto the bus is the transmitter and the device receiving data is the receiver. The bus is controlled by a master device which generates the serial clock (SCLK), controls the bus access and generates the START and STOP conditions. The TC664/TC665 always work as a slave device. Both master and slave devices can operate as either transmitter or receiver, but the master device determines which mode is activated.

5.1.3 START CONDITION (START)

A HIGH to LOW transition of the SDA line while the clock (SCLK) is HIGH determines a START condition. All commands must be preceded by a START condition.

5.1.4 ADDRESS BYTE

Immediately following the Start Condition, the host must transmit the address byte to the TC664/TC665. The 7-bit SMBus address for the TC664/TC665 is **0011 011**. The 7-bit address transmitted in the serial bit stream must match for the TC664/TC665 to respond with an Acknowledge (indicating the TC664/TC665 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read-Write Bit. This bit is a ‘1’ for a read operation or ‘0’ for a write operation. During the first phase of any transfer, this bit will be set = 0 to indicate that the command byte is being written.

5.1.5 STOP CONDITION (STOP)

A LOW to HIGH transition of the SDA line while the clock (SCLK) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

5.1.6 DATA VALID

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

© 2002 Microchip Technology Inc.
The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is unlimited.

5.1.7 ACKNOWLEDGE (ACK)

Each receiving device, when addressed, is obliged to generate an acknowledge bit after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Setup and hold times must be taken into account. During reads, a master device must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (TC664/TC665) will leave the data line HIGH to enable the master device to generate the STOP condition.

5.2 SMBus Protocols

The TC664/TC665 devices communicate with three standard SMBus protocols. These are the write byte, read byte and receive byte. The receive byte is a shortened method for reading from or writing to a register which had been selected by the previous read or write command. These transmission protocols are shown in Figures 5-1, 5-2 and 5-3.

<table>
<thead>
<tr>
<th>S ADDRESS</th>
<th>WR</th>
<th>ACK</th>
<th>COMMAND</th>
<th>ACK</th>
<th>DATA</th>
<th>ACK</th>
<th>P</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 Bits</td>
<td>8 Bits</td>
<td></td>
<td>Command Byte: selects which register you are writing to.</td>
<td>8 Bits</td>
<td>Data Byte: data goes into the register set by the command byte.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 5-1:** SMBus Protocol: Write Byte Format.

<table>
<thead>
<tr>
<th>S ADDRESS</th>
<th>RD</th>
<th>ACK</th>
<th>DATA</th>
<th>NACK</th>
<th>P</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 Bits</td>
<td>8 Bits</td>
<td></td>
<td>Data Byte: reads from the register set by the command byte.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 5-2:** SMBus Protocol: Read Byte Format.

<table>
<thead>
<tr>
<th>S ADDRESS</th>
<th>RD</th>
<th>ACK</th>
<th>DATA</th>
<th>NACK</th>
<th>P</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 Bits</td>
<td>8 Bits</td>
<td></td>
<td>Data Byte: reads data from the register commanded by the last Read Byte or Write Byte transmission</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 5-3:** SMBus Protocol: Receive Byte Format.

S = Start Condition
P = Stop Condition
Shaded = Slave Transmission
ACK = Acknowledge = 0
NACK = Not Acknowledged = 1
WR = Write = 0
RD = Read = 1

S = Start Condition
P = Stop Condition
Shaded = Slave Transmission
ACK = Acknowledge = 0
NACK = Not Acknowledged = 1
WR = Write = 0
RD = Read = 1
6.0 REGISTER SET

The TC664/TC665 devices contain 7 registers that provide a variety of data and functionality control to the outside system. These registers are listed in Table 6-1. Of key importance is the command byte information, which is needed in the read and write protocols to select the individual registers.

### TABLE 6-1: COMMAND BYTE ASSIGNMENTS

<table>
<thead>
<tr>
<th>Register</th>
<th>Command</th>
<th>Read</th>
<th>Write</th>
<th>POR Default State</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPM</td>
<td>0000 0000</td>
<td>X</td>
<td>—</td>
<td>0 0000 0000</td>
<td>RPM Output</td>
</tr>
<tr>
<td>FAN_FAULT</td>
<td>0000 0010</td>
<td>X</td>
<td>X</td>
<td>0000 1010</td>
<td>Fan Fault Threshold</td>
</tr>
<tr>
<td>CONFIG</td>
<td>0000 0100</td>
<td>X</td>
<td>X</td>
<td>0000 1010</td>
<td>Configuration</td>
</tr>
<tr>
<td>STATUS</td>
<td>0000 0101</td>
<td>X</td>
<td>—</td>
<td>00X0 0000</td>
<td>Status. See Section 6.4, Status Register explanation of X</td>
</tr>
<tr>
<td>DUTY_CYCLE</td>
<td>0000 0110</td>
<td>X</td>
<td>X</td>
<td>0000 0010</td>
<td>Fan Speed Duty Cycle</td>
</tr>
<tr>
<td>MFR_ID</td>
<td>0000 0111</td>
<td>X</td>
<td>—</td>
<td>0010 0100</td>
<td>Manufacturer Identification</td>
</tr>
<tr>
<td>VER_ID</td>
<td>0000 1000</td>
<td>X</td>
<td>—</td>
<td>0000 00XX</td>
<td>Version Identification: XX = '10’ TC664, XX = ‘11’ TC665</td>
</tr>
</tbody>
</table>

6.1 RPM-OUTPUT Register (RPM)

As discussed in Section 4.7, fan current pulses are detected at the SENSE input of the TC664/TC665 device. The current pulse information is used to calculate the fan RPM. The fan RPM data is then written to the RPM register. RPM is a 9-bit register that provides the RPM information in 50 RPM (8-bit) or 25 RPM (9-bit) increments. This is selected via RES (bit 6<0>) in the Configuration Register, with ‘0’ = 50 RPM and ‘1’ = 25 RPM. The default state is zero (50 RPM). The maximum fan RPM value that can be read is 12775 RPM. If this value is exceeded, RCO (bit 3<0>) in the Status Register will be set to a ‘1’ to indicate that a counter overflow of the RPM Register has occurred.

Register 6-1 shows the RPM output register 9-bit format.

### REGISTER 6-1: RPM OUTPUT REGISTER (RPM)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>25</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>12750</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>12775</td>
</tr>
</tbody>
</table>
6.2 FAN_FAULT Threshold Register (FAN_FAULT)

The FAN_FAULT Threshold Register is used to set the fan fault threshold level for the fan. The Fan Fault Threshold Register is an 8-bit read/writable register that allows the fan fault RPM threshold to be set in 50 RPM increments. The default setting for the Fan Fault Register is 500 RPM (0000 1010). The maximum set point value is 12750 RPM.

If the measured fan RPM (stored in the RPM Register) drops below the value that is set in the Fan Fault Register for more than 2.4 sec, FF (bit 0<0>) in the Status Register will be set to a ’1’ and the FAULT output will be pulled low. See Register 6-2 for the Fan Fault Threshold Register 8-bit format.

REGISTER 6-2: FAN FAULT THRESHOLD REGISTER (FAN_FAULT)

<table>
<thead>
<tr>
<th>D(7)</th>
<th>D(6)</th>
<th>D(5)</th>
<th>D(4)</th>
<th>D(3)</th>
<th>D(2)</th>
<th>D(1)</th>
<th>D(0)</th>
<th>RPM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>50</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>12700</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>12750</td>
</tr>
</tbody>
</table>
6.3 CONFIGURATION REGISTER (CONFIG)

The Configuration Register is an 8-bit, read/writeable, multi-function control register. This register allows the user to clear fan faults, select RPM resolution, select V<sub>OUT</sub> duty cycle (fan speed) control method, select the fan current pulses per rotation for the fan (for fan RPM calculation) and put the TC664/TC665 device into a shutdown mode to reduce power consumption. See Register 6-3 below for the Configuration Register bit descriptions.

REGISTER 6-3: CONFIGURATION REGISTER (CONFIG)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFCLR</td>
<td>RES</td>
<td>DUTYC</td>
<td>---</td>
<td>---</td>
<td>FPPR</td>
<td>FPPR</td>
<td>SDM</td>
</tr>
</tbody>
</table>

bit 7  FFCLR: Fan Fault Clear
1 = Clear Fan Fault, this will reset the Fan Fault bit in the Status Register and the FAULT output.
0 = Normal Operation (default)

bit 6  RES: Resolution Selection for RPM Output Register
1 = RPM Output Register (RPM) will be set for 25 RPM (9-bit) resolution.
0 = RPM Output Register (RPM) will be set for 50 RPM (8-bit) resolution. (default)

bit 5  DUTYC: Duty-Cycle Control Method
1 = The V<sub>OUT</sub> duty-cycle will be controlled via the SMBus interface. The value for the V<sub>OUT</sub> duty-cycle will be taken from the duty-cycle register (DUTY_CYCLE).
0 = The V<sub>OUT</sub> duty-cycle will be controlled via the V<sub>IN</sub> analog input pin. The V<sub>OUT</sub> duty-cycle value will be between 30% and 100% for V<sub>IN</sub> values between 1.62 V and 2.6 V typical. If the V<sub>IN</sub> pin is open when this mode is selected, the V<sub>OUT</sub> duty-cycle will default to 39.33%. (default)

bit 4  Unimplemented: Read as '0'

bit 3  Unimplemented: Read as '1'

bit 2-1 FPPR: Fan Pulses Per Rotation
The TC664/TC665 device uses this setting to understand how many current pulses per revolution the fan should have. It then uses this as part of the calculation for the fan RPM value for the RPM Register. See Section 7.7 for application information on determining your fan's number of current pulses per revolution.
00 = 1
01 = 2 (default)
10 = 4
11 = 8

bit 0  SDM: Shutdown Mode
1 = Shutdown Mode. See Section 4.9 for more information on low power shutdown mode.
0 = Normal Operation. (default)

Legend:
R = Readable bit      W = Writable bit   U = Unimplemented bit
-n = Value at POR     '1' = Bit is set   '0' = Bit is cleared   x = Bit is unknown
6.4 STATUS REGISTER (STATUS)

The Status Register provides all the information about what is going on within the TC664/TC665 devices. Fan fault information, \( V_{IN} \) status, RPM counter overflow and over temperature indication are all available in the Status Register. The Status Register is an 8-bit Read only register with bits 1, 4, 6 and 7 unused. See Register 6-4 below for the bit descriptions.

### REGISTER 6-4: STATUS REGISTER (STATUS)

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>R-X</td>
<td>U-0</td>
<td>R-0</td>
<td>R-X</td>
<td>U-X</td>
</tr>
<tr>
<td>O</td>
<td>T</td>
<td>F</td>
<td>RCO</td>
<td>VSTAT</td>
<td></td>
<td>FF</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7**: Unimplemented: Read as ‘0’
- **bit 5**: OTF: Over Temperature Fault Condition
  
  For the TC664/TC665 device, this bit is set to the proper state immediately at startup and is therefore treated as an unknown (X). If \( V_{IN} \) is greater than the threshold required for 100% duty cycle on \( V_{OUT} \) (2.6 V typical), then the bit will be set to a ‘1’. If it is less than the threshold, the bit will be set to ‘0’. This is determined at power-up.

  - 1 = Over temperature condition has occurred.
  - 0 = Normal operation, \( V_{IN} \) is less than 2.6 V.

- **bit 4**: Unimplemented: Read as ‘0’

- **bit 3**: RCO: RPM Counter Overflow

  1 = Fault condition. The maximum RPM reading of 12775 RPM in register RPM has been exceeded. This bit will automatically reset to zero when the RPM reading comes back into range.

  0 = Normal operation. RPM reading is within limits (default).

- **bit 2**: VSTAT: \( V_{IN} \) Input Status

  For the TC664/TC665 devices, the \( V_{IN} \) pin status is checked immediately at power-up. If no external thermistor or voltage output network is connected (\( V_{IN} \) is open), this bit is set to a ‘1’.

  If an external network is detected, this bit is set to ‘0’. If the \( V_{IN} \) pin is open and SMBus operation has not been selected in the Configuration Register, the \( V_{OUT} \) duty cycle will default to 39.33%.

  - 1 = \( V_{IN} \) is open.
  - 0 = Normal operation. Voltage present at \( V_{IN} \).

- **bit 1**: Unimplemented: Read as ‘unknown’

- **bit 0**: FF: Fan Fault

  1 = Fault Condition. The value for fan RPM in the RPM Register has fallen below the value set in the FAN_FAULT Threshold Register. The speed of the fan is too low and a fault condition is being indicated. The FAULT output will be pulled low at the same time. This fault bit can be cleared using the Fan Fault Clear bit (FFCLR (bit 7<0>)) in the Configuration Register.

  0 = Normal Operation (default).
6.5 DUTY-CYCLE Register (DUTY_CYCLE)

The DUTY_CYCLE register is a 4-bit read/write register used to control the duty cycle of the V_OUT output. The controllable duty cycle range via this register is 30% to 100%, with programming steps of 4.67%. This method of duty cycle control is mainly used with the SMBus interface. However, if the V_IN method of duty cycle control has been selected (or defaulted to), and the V_IN pin is open, the duty cycle will go to the default setting for this register, which is \(0010\) (39.33%). The duty cycle settings are shown in Register 6-5.

### REGISTER 6-5: DUTY-CYCLE REGISTER (DUTY_CYCLE)

<table>
<thead>
<tr>
<th>D(3)</th>
<th>D(2)</th>
<th>D(1)</th>
<th>D(0)</th>
<th>Duty-Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>30%</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>34.67%</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>39.33% (default for V_IN open and when SMBus is not selected)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>44%</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>48.67%</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>53.33%</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>58%</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>62.67%</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>67.33%</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>72%</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>76.67%</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>81.33%</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>86%</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>90.67%</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>95.33%</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>100%</td>
</tr>
</tbody>
</table>

6.6 Manufacturer’s Identification Register (MFR_ID)

This register allows the user to identify the manufacturer of the part. The MFR_ID register is an 8-bit Read only register. See Register 6-6 for the Microchip manufacturer ID.

### REGISTER 6-6: MANUFACTURER’S IDENTIFICATION REGISTER (MFR_ID)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

6.7 Version ID Register (VER_ID)

This register is used to indicate which version of the device is being used, either the TC664 or the TC665. This register is a simple 2-bit Read only register.

### REGISTER 6-7: VERSION ID REGISTER (VER_ID)

<table>
<thead>
<tr>
<th>D[1]</th>
<th>D[0]</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>TC664</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>TC665</td>
</tr>
</tbody>
</table>
7.0 APPLICATIONS INFORMATION

7.1 Connecting to the SMBus

The SMBus is an open collector bus, requiring pull-up resistors connected to the SDA and SCLK lines. This configuration is shown in Figure 7-1.

**FIGURE 7-1:** Pull-up Resistors On SMBus.

The number of devices connected to the bus is limited only by the maximum rise and fall times of the SDA and SCLK lines. Unlike I2C specifications, SMBus does not specify a maximum bus capacitance value. Rather, the SMBus specification calls out that the maximum current through the pull-up resistor be 350 µA (minimum, 100 µA, is also specified). Therefore, the value of the pull-up resistors will vary depending on the system’s bias voltage, VDD. Minimizing bus capacitance is still very important as it directly affects the rise and fall times of the SDA and SCLK lines. The range for pull-up resistor values for a 5 V system are shown in Figure 7-1.

Although SMBus specifications only require the SDA and SCLK lines to pull down 350 µA, with a maximum voltage drop of 0.4 V, the TC664/TC665 devices have been designed to meet a maximum voltage drop of 0.4 V with 3 mA of current. This allows lower values of pull-up resistors to be used, which will allow higher bus capacitance. If this is to be done, all devices on the bus must be able to meet the same pull down current requirements as well.

A possible configuration using multiple devices on the SMBus is shown in Figure 7-2.

**FIGURE 7-2:** Multiple Devices on SMBus.

7.2 Setting the PWM Frequency

The PWM frequency of the VOUT output is set by the capacitor value attached to the CF pin. The PWM frequency will be 30 Hz (typical) for a 1 µF capacitor. The relationship between frequency and capacitor value is linear, making alternate frequency selections easy.

As stated in previous sections, the PWM frequency should be kept in the range of 15 Hz to 35 Hz. This will eliminate the possibility of having audible frequencies when varying the duty cycle of the fan drive.

A very important factor to consider when selecting the PWM frequency for the TC664/TC665 devices is the RPM rating of the selected fan and the minimum duty cycle that you will be operating at. For fans that have a full speed rating of 3000 RPM or less, it is desirable to use a lower PWM frequency. A lower PWM frequency allows for a longer time period to monitor the fan current pulses. The goal is to be able to monitor at least two fan current pulses during the on time of the VOUT output.

**Example:** Your system design requirement is to operate the fan at 50% duty cycle when ambient temperatures are below 20°C. The fan full speed RPM rating is 3000 RPM and has four current pulses per rotation. At 50% duty cycle, the fan will be operating at approximately 1500 RPM.

\[
\text{Time for one revolution (msec.)} = \frac{60 \times 1000}{1500} = 40
\]

If one fan revolution occurs in 40 msec, then each fan pulse occurs 10 msec apart. In order to detect two fan current pulses, the on time of the VOUT pulse must be at least 20 msec. With the duty cycle at 50%, the total period of one cycle must be at least 40 msec, which makes the PWM frequency 25 Hz. For this example, a PWM frequency of 20 Hz is recommended. This would define a CF capacitor value of 1.5 µF.
7.3 Temperature Sensor Design

As discussed in previous sections, the $V_{IN}$ analog input has a range of 1.62 V to 2.6 V (typical), which represents a duty cycle range on the $V_{OUT}$ output of 30% to 100%, respectively. The $V_{IN}$ voltages can be thought of as representing temperatures. The 1.62 V level is the low temperature at which the system only requires 30% fan speed for proper cooling. The 2.6 V level is the high temperature, for which the system needs maximum cooling capability, so the fan needs to be at 100% speed.

One of the simplest ways of sensing temperature over a given range is to use a thermistor. By using an NTC thermistor as shown in Figure 7-3, a temperature variant voltage can be created.

**FIGURE 7-3: Temperature Sensing Circuit.**

Figure 7-3 represents a temperature dependent voltage divider circuit. $R_t$ is a conventional NTC thermistor, $R_1$ and $R_2$ are standard resistors. $R_1$ and $R_t$ form a parallel resistor combination that will be referred to as $R_{TEMP}$ ($R_{TEMP} = R_1 * R_t / (R_1 + R_t)$). As the temperature increases, the value of $R_t$ decreases and the value of $R_{TEMP}$ will decrease with it. Accordingly, the voltage at $V_{IN}$ increases as temperature increases, giving the desired relationship for the $V_{IN}$ input. The purpose of $R_1$ is to help linearize the response of the sensing network. Figure 7-4 shows an example of this.

There are many values that can be chosen for the NTC thermistor. There are also thermistors that have a linear resistance, instead of logarithmic, which can help to eliminate $R_1$. If less current draw from $V_{DD}$ is desired, then a larger value thermistor should be chosen. The voltage at the $V_{IN}$ pin can also be generated by a voltage output temperature sensor device. The key is to get the desired $V_{IN}$ voltage to system (or component) temperature relationship.

The following equations apply to the circuit in Figure 7-3.

**EQUATION**

$$V(t1) = \frac{V_{DD} \times R_2}{R_{TEMP}(t1) + R_2}$$

$$V(t2) = \frac{V_{DD} \times R_2}{R_{TEMP}(t2) + R_2}$$

In order to solve for the values of $R_1$ and $R_2$, the values for $V_{IN}$ and the temperatures at which they are to occur, need to be selected. The variables, $t1$ and $t2$, represent the selected temperatures. The value of the thermistor at these two temperatures can be found in the thermistor data sheet. With the values for the thermistor and the values for $V_{IN}$, you now have two equations from which the values for $R_1$ and $R_2$ can be found.

**Example:** The following design goals are desired:

- Duty Cycle = 50% ($V_{IN} = 1.9$ V) with Temperature ($t1$) = 30°C
- Duty Cycle = 100% ($V_{IN} = 2.6$ V) with Temperature ($t2$) = 60°C

Using a 100 kΩ thermistor (25°C value), we look up the thermistor values at the desired temperatures:

- $R_t = 79428 \, \Omega$ @ 30°C
- $R_t = 22593 \, \Omega$ @ 60°C

Substituting these numbers into the given equations, we come up with the following numbers for $R_1$ and $R_2$.

- $R_1 = 34.8 \, k\Omega$
- $R_2 = 14.7 \, k\Omega$

**FIGURE 7-4: How Thermistor Resistance, $V_{IN}$, And $R_{TEMP}$ Vary With Temperature.**

Figure 7-4 graphs three parameters versus temperature. They are $R_t$, $R_1$ in parallel with $R_t$, and $V_{IN}$. As described earlier, you can see that the thermistor has a logarithmic resistance variation. When put in parallel with $R_t$, though, the combined resistance becomes more linear, which is the desired effect. This gives us the linear looking curve for $V_{IN}$. 
7.4 FanSense Network ($R_{\text{SENSE}}$ & $C_{\text{SENSE}}$)

The network comprised of $R_{\text{SENSE}}$ and $C_{\text{SENSE}}$ allows the TC664/TC665 devices to detect commutation of the fan motor. $R_{\text{SENSE}}$ converts the fan current into a voltage. $C_{\text{SENSE}}$ AC couples this voltage signal to the SENSE pin. The goal of the SENSE network is to provide a voltage pulse to the SENSE pin that has a minimum amplitude of 120 mV. This will ensure that the current pulse caused by the fan commutation is recognized by the TC664/TC665 device.

A 0.1 µF ceramic capacitor is recommended for $C_{\text{SENSE}}$. Smaller values will require larger sense resistors to be used. Using a 0.1 µF capacitor results in reasonable values for $R_{\text{SENSE}}$. Figure 7-5 illustrates a typical SENSE network.

![Typical Sense Network](image)

**FIGURE 7-5:** Typical Sense Network.

The value of $R_{\text{SENSE}}$ will change with the current rating of the fan. A key point is that the current rating of the fan specified by the manufacturer may be a worst case rating. The actual current drawn by the fan may be lower than this rating. For the purpose of setting the value for $R_{\text{SENSE}}$, the operating fan current should be measured.

Table 7-1 shows values of $R_{\text{SENSE}}$ according to the nominal operating current of the fan. The fan currents are average values. If the fan current falls between two of the values listed, use the higher resistor value.

![Typical Fan Current and Sense Pin Waveforms](image)

**FIGURE 7-6:** Typical Fan Current and Sense Pin Waveforms.

### TABLE 7-1: $R_{\text{SENSE}}$ VS. FAN CURRENT

<table>
<thead>
<tr>
<th>Nominal Fan Current (mA)</th>
<th>$R_{\text{SENSE}}$ (ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>9.1</td>
</tr>
<tr>
<td>100</td>
<td>4.7</td>
</tr>
<tr>
<td>150</td>
<td>3.0</td>
</tr>
<tr>
<td>200</td>
<td>2.4</td>
</tr>
<tr>
<td>250</td>
<td>2.0</td>
</tr>
<tr>
<td>300</td>
<td>1.8</td>
</tr>
<tr>
<td>350</td>
<td>1.5</td>
</tr>
<tr>
<td>400</td>
<td>1.3</td>
</tr>
<tr>
<td>450</td>
<td>1.2</td>
</tr>
<tr>
<td>500</td>
<td>1.0</td>
</tr>
</tbody>
</table>

7.5 Output Drive Device Selection

The TC664/TC665 devices are designed to drive two external NPN transistors or two external N-channel MOSFETs as the fan speed modulating elements. These two arrangements are shown in Figure 7-7. For lower current fans, NPN transistors are a very economical choice for the fan drive device. It is recommended that, for higher current fans (500 mA and above), MOSFETs be used as the fan drive device. Table 7-2 provides some possible part numbers for use as the fan drive element.

When using an NPN transistor as the fan drive element, a base current limiting resistor must be used. This is shown in Figure 7-7.

When using MOSFETs as the fan drive element, it is very easy to turn the MOSFETs on and off at very high rates. Because the gate capacitances of these small
MOSFETs are very low, the TC664/TC665 devices can charge and discharge them very quickly leading to very fast edges. Of key concern is the turn-off edge of the MOSFET. Since the fan motor winding is essentially an inductor, when the MOSFET is turned off, the current that was flowing through the motor wants to continue to flow. If the fan does not have internal clamp diodes around the windings of the motor, there is no path for this current to flow through and the voltage at the drain of the MOSFET may rise until the drain to source rating of the MOSFET is exceeded. This will most likely cause the MOSFET to go into avalanche mode. Since there is very little energy in this occurrence, it will probably not fail the device, but it would be a long term reliability issue. The following is recommended:

- Ask how the fan is designed. If the fan has clamp diodes internally, you will not experience this problem. If the fan does not have internal clamp diodes, it is a good idea to put one externally (Figure 7-8). You can also put a resistor between \( V_{OUT} \) and the gate of the MOSFET, which will help slow down the turn-off and limit this condition.

**FIGURE 7-7:** Output Drive Device Configurations.

**TABLE 7-2:** FAN DRIVE DEVICE SELECTION TABLE (NOTE 2)

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Max Vbe sat / Vgs(V)</th>
<th>Min hfe</th>
<th>Vce/(V_{DS})</th>
<th>Fan Current (mA)</th>
<th>Suggested Rbase (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MMBT2222A</td>
<td>SOT-23</td>
<td>1.2</td>
<td>50</td>
<td>40</td>
<td>150</td>
<td>800</td>
</tr>
<tr>
<td>MPS2222A</td>
<td>TO-92</td>
<td>1.2</td>
<td>50</td>
<td>40</td>
<td>150</td>
<td>800</td>
</tr>
<tr>
<td>MPS6602</td>
<td>TO-92</td>
<td>1.2</td>
<td>50</td>
<td>40</td>
<td>500</td>
<td>301</td>
</tr>
<tr>
<td>SI2302</td>
<td>SOT-23</td>
<td>2.5</td>
<td>NA</td>
<td>20</td>
<td>500</td>
<td>301</td>
</tr>
<tr>
<td>MGSF1N02E</td>
<td>SOT-23</td>
<td>2.5</td>
<td>NA</td>
<td>20</td>
<td>500</td>
<td>Note 1</td>
</tr>
<tr>
<td>SI4410</td>
<td>SO-8</td>
<td>4.5</td>
<td>NA</td>
<td>30</td>
<td>1000</td>
<td>Note 1</td>
</tr>
<tr>
<td>SI2308</td>
<td>SOT-23</td>
<td>4.5</td>
<td>NA</td>
<td>60</td>
<td>500</td>
<td>Note 1</td>
</tr>
</tbody>
</table>

**Note 1:** A series gate resistor may be used in order to control the MOSFET turn-on and turn-off times.  
**Note 2:** These drive devices are suggestions only. Fan currents listed are for individual fans.
FIGURE 7-8: Clamp Diode For Fan Turn-off.

7.6 Bias Supply Bypassing and Noise Filtering

The bias supply (VDD) for the TC664/TC665 devices should be bypassed with a 1 µF ceramic capacitor. This capacitor will help supply the peak currents that are required to drive the base/gate of the external fan drive devices.

As the VIN pin controls the duty cycle in a linear fashion, any noise on this pin can cause duty cycle jittering. For this reason, the VIN pin should be bypassed with a 0.01 µF capacitor.

In order to keep fan noise off of the TC664/TC665 device ground, individual ground returns for the TC664/TC665 and the low side of the fan current sense resistor should be used.

7.7 Determining Current Pulses Per Revolution of Fans

There are many different fan designs available in the marketplace today. The motor designs can vary and, along with it, the number of current pulses in one fan revolution. In order to correctly measure and communicate the fan speed, the TC664/TC665 devices must be programmed for the proper number of fan current pulses per revolution. This is done by setting the FPPR bit in the Configuration Register to the proper values (see Section 6.3 for settings). A fan's current pulses per revolution can be determined in the following manner.

The first piece of information required is the fan's full speed RPM rating. The fan RPM rating can then be converted to give the time for one revolution using the following equation:

\[
\text{Time for one revolution (msec.)} = \frac{60 \times 1000}{\text{Fan RPM}}
\]

The fan current can now be monitored over this time period. The number of pulses occurring in this time period is the fan's "Current Pulses per Rotation" rating which is needed in order to accurately read fan RPM.

Example: The full speed fan RPM rating is 8200 RPM. From this, the time for one fan revolution is calculated to be 7.3 msec, using the previously discussed equation. Using a current probe, the fan current can be monitored as the fan is operating at full speed. Figure 7-9 shows the fan current pulses for this example. The 7.44 msec window, marked by the cursors, is very near the 7.3 msec calculated above and is within the tolerance of the fan ratings. Four current pulses occur within this 7.44 msec time frame. Given this information, FPPR (bits 2-1<01>) in the Configuration Register should be set to '10' to indicate 4 current pulses per revolution.

FIGURE 7-9: Four Current Pulses Per Revolution Fan.

7.8 How to Eliminate False Current Pulse Sensing

During the PWM mode of operation, some fans will generate an extra current pulse. This pulse occurs when the external drive device is turned on and is, in most cases, caused by the fan's electronics that control the fan motor. This pulse does not represent true fan current and needs to be blanked out. This is particularly important for detecting a fan in a locked rotor condition.
Figure 7-10 shows the voltage pulse at the Sense pin, which is caused by the fan’s "extra" current pulse during PWM output turn-on.

**FIGURE 7-10: Extra Pulse at Sense Pin.**

This problem occurs mainly with fans that have a current waveshape like the one shown in Figure 7-9. For configurations where an NPN transistor is being used as the external drive device, the typical Rsense and CSENSE scheme can continue to be used to sense the fan current pulses. In order to eliminate the extra current pulse, a slow down capacitor can be placed from the base of the transistor to ground. A 0.1 µF capacitor is appropriate in most cases. This arrangement is shown in Figure 7-11. This capacitor will help to slow down the turn-on edge of the transistor and reduce the amplitude of the extra current pulse.

For configurations using an N-channel MOSFET as the drive device, the slow down capacitor does not fix all conditions and the current sensing scheme must be changed. Since the current for this type of fan always returns to zero, the coupling capacitor, CSENSE, is not needed. Instead, it will be replaced by an R-C configuration to eliminate the voltage pulse generated by the extra current pulse. This new sensing configuration is shown in Figure 7-12. The values of the resistor/capacitor combination should be adjusted so that the voltage pulse generated by the extra current pulse is smoothed and is not registered by the TC664/TC665 as a true fan current pulse. Typical values for RsLOW and CsLOW are 1 kΩ and 1000 pF, respectively.
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

Legend:

1. Part Number and temperature range
2. Part Number and temperature range
3. Year and work week
4. Lot ID

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard device marking consists of Microchip part number, year code, week code, and traceability code.
8.2 Taping Form

Component Taping Orientation for 10-Pin MSOP Devices

User Direction of Feed

Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size:

<table>
<thead>
<tr>
<th>Package</th>
<th>Carrier Width (W)</th>
<th>Pitch (P)</th>
<th>Part Per Full Reel</th>
<th>Reel Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>10-Pin MSOP</td>
<td>12 mm</td>
<td>8 mm</td>
<td>2500</td>
<td>13 in.</td>
</tr>
</tbody>
</table>

8.3 Package Information

10-Pin MSOP

Dimensions: inches (mm)
ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User’s Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

• Latest Microchip Press Releases
• Technical Support Section with Frequently Asked Questions
• Design Tips
• Device Errata
• Job Postings
• Microchip Consultant Program Member Listing
• Links to other useful web sites related to Microchip Products
• Conferences for products, Development Systems, technical information and more
• Listing of seminars and events

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip’s development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and
1-480-792-7302 for the rest of the world.
READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this Data Sheet.

To: Technical Publications Manager
RE: Reader Response
From: Name
Company
Address
City / State / ZIP / Country
Telephone: (_____) _________ - _________
FAX: (_____ ) _________ - _________
Application (optional):

Would you like a reply? ___ Y ___ N

Device: TC664/TC665

Questions:
1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.            X            /XX

Device  | Temperature Range  | Package
---------|--------------------|---------
TC664    |                    |         |
TC664T   |                    |         |
TC665    |                    |         |
TC665T   |                    |         |

Device: TC664: PWM Fan Speed Controller w/Fault Detection
         TC664T: PWM Fan Speed Controller w/Fault Detection (Tape and Reel)
         TC665: PWM Fan Speed Controller w/Fault Detection
         TC665T: PWM Fan Speed Controller w/Fault Detection (Tape and Reel)

Temperature Range: E = -40°C to +85°C

Package: UN = Plastic Micro Small Outline (MSOP), 10-lead

Examples:

a) TC664EUN: PWM Fan Speed Controller w/ Fault Detection
b) TC664EUNTR: PWM Fan Speed Controller w/Fault Detection (Tape and Reel)
c) TC665EUN: PWM Fan Speed Controller w/ Fault Detection
d) TC665EUNTR: PWM Fan Speed Controller w/Fault Detection (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.
Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip’s products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELoC, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, MXLAB, PICC, PICDEM, PICDEM.net, rfPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.
AMERICAS
Corporate Office
2335 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2335 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
Kokomo, Indiana 46902
Tel: 765-864-2950 Fax: 765-864-3858

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIAPACIFIC
Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wuji Road
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wuji Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

EUROPE

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lastrup vej 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9910 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Boulogne-Billancourt 92100 France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144-0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza Milan Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham Berkshire England RG41 5TU
Tel: 44 118 921 5869 Fax: 44 118 921 5820

Austria
Microchip Technology Austria GmbH
Duriolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399 Fax: 43-7242-2244-393