**Obsolete Device**

# TC1142

## Inductorless -2x Boost/Buck Regulator

### Features

- Input Range 2.5V to 5.5V
- Regulated Output Options from -3.0 to -5.0V
- Output Current 20mA (max)
- 200kHz Internal Oscillator Frequency
- External Synchronizing Clock Input
- Logic Level Shutdown
  - 1µA (max) Supply Current
- Available in 8-Pin MSOP Package

### Applications

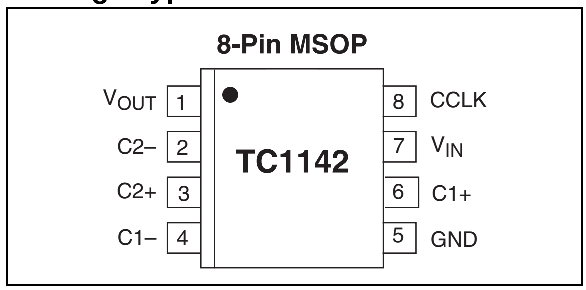
- Cellular Phones
- Battery Powered/Portable Equipment

### Device Selection Table

| Part Number | Output Voltage (V)* | Package | Operating Temp. Range |
|---|---|---|---|
| TC1142-3.0EUA | 3.0 | 8-Pin MSOP | -40°C to +85°C |
| TC1142-4.0EUA | 4.0 | 8-Pin MSOP | -40°C to +85°C |
| TC1142-5.0EUA | 5.0 | 8-Pin MSOP | -40°C to +85°C |

*Other output voltages are available (-3.5V and -4.5V). Please contact Microchip Technology Inc. for details.

### Package Type



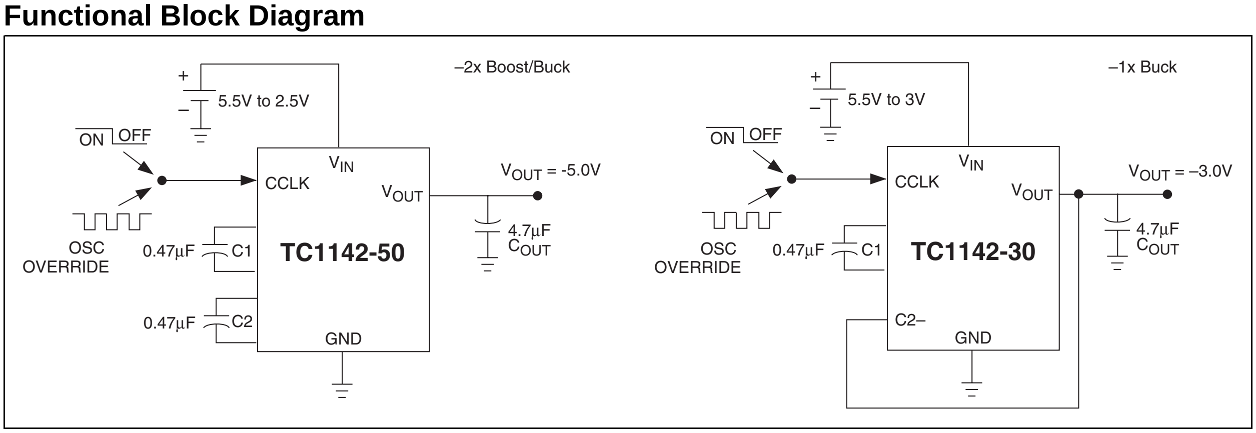

### General Description

The TC1142 generates a regulated negative voltage from -3V to -5V at 20mA from an input of 2.5V to 5.5V, using only three external capacitors. Other boost/buck switching regulators must use an inductor, which is larger and radiates EMI. An internal voltage comparator inhibits the charge pump when $V_{OUT}$ is more negative than the regulated value (per the ordering option). The values of flying capacitors C1 and C2 are chosen to be less than $C_{OUT}$ in order to reduce the ripple generated from regulating $V_{OUT}$ in this manner. The TC1142 also can be used as a -1x buck regulator by omitting C2, and connecting the C2 pin to $V_{OUT}$.

The part goes into shutdown when the CCLK input is driven low. When in shutdown mode, the part draws a maximum of 1µA. When CCLK is pulled high, the part runs from the internal 200kHz oscillator. The device may be run with an external clock, provided the frequency is greater than 3kHz and less than 500kHz.

The TC1142 comes in a space-saving MSOP package.

### Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings*

Supply Voltage ($V_{IN}$) with $C_{OUT}$ Connected ..........6.5V
CCLK Voltage................................-0.3V to ($V^+$ + 0.3V)
Power Dissipation............................................320mW
Operating Temperature Range
8-Pin MSOP .................................-40°C to +85°C
Storage Temperature Range ..............-65°C to +160°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### TC1142 ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** $R_L = \infty$, $V_{IN}$ = 3.2V, Mode = -2x, C1 = C2 = 0.47µF (Note 1), CCLK = $V_{IH}$, $C_{OUT}$ = 4.7µF, for $V_R$ = 3V, $V_{IN}$ = 3.5V, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| Symbol | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Supply Voltage | 2.5 | — | 5.5 | V | |
| $V_{OUT}$ | Output Voltage | -($V_R$ + 0.2) | -$V_R$ | -($V_R$ – 0.2) | V | $I_L$ = 0mA (Note 2) |
| $V_{P-P}$ | Output Ripple | — | 100 | — | mV | $I_L$ = 10mA |
| $I_{SUPPLY}$ | Supply Current | — | 200 | 400 | µA | |
| $I_{SUPPLY1}$ | | — | 0.1 | 1 | µA | CCLK = 0V |
| $R_{OUTCL}$ | Closed-Loop Output Resistance | — | 2 | 6 | Ω | |
| $R_{OUT}$ | Open-Loop Output Resistance | — | 30 | — | Ω | (Note 3) |
| $f_{OSC}$ | Internal Oscillator Frequency | 150 | 200 | 275 | kHz | |
| $f_{CCLK}$ | External Clock Frequency, Typical | 3 | — | 500 | kHz | (Note 4) |
| $P_{EFF}$ | Power Efficiency | 70 | 76 | — | % | $I_L$ = 10mA, $V_R$ = 5V; (See Equation 3-5) |
| $V_{IH}$ | CCLK Input High Threshold | 2.2 | — | — | V | |
| $V_{IL}$ | CCLK Input Low Threshold | — | — | 1.0 | V | |

**Note 1:** Assume C1 and C2 have an ESR of 1Ω.
**2:** $V_R$ is the voltage output specified in the ordering option.
**3:** Measured in -1x Mode. For $V_R$ = 3V, $V_{IN}$ = 2.5V.
**4:** CCLK is driven with an external clock. Minimum frequency = $1/2t_0$ at 50% duty cycle, where $t_0$ is the counter timeout period.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

### TABLE 2-1: PIN FUNCTION TABLE

| Pin No. (8-Pin MSOP) | Symbol | Description |
|---|---|---|
| 1 | $V_{OUT}$ | Regulated negative output voltage. |
| 2 | C2– | Negative terminal of flying capacitor C2. |
| 3 | C2+ | Positive terminal of flying capacitor C2. |
| 4 | C1– | Negative terminal of flying capacitor C1. |
| 5 | GND | Power supply ground. |
| 6 | C1+ | Positive terminal of flying capacitor C1. |
| 7 | $V_{IN}$ | Power supply positive voltage input (2.5V to 5.5V). |
| 8 | CCLK | Clock control input:<br>If low, the TC1142 is in Shutdown mode (1µA, max).<br>If high, the TC1142 runs off the internal oscillator (200kHz, typ.).<br>CCLK can be overridden by an external oscillator from 3kHz to 500kHz. |

## 3.0 DETAILED DESCRIPTION

The TC1142 inductorless -2x boost/buck regulator is an inverting charge pump that uses a pulse-frequency modulation (PFM) control scheme to produce a regulated negative output voltage, $-V_R$, between -3V and -5V (depending on the output voltage option) at 20mA maximum load. Output voltage regulation is achieved by gating ON the clock to the charge pump for a single half-clock period whenever the output is more positive than $V_R$, and gating it OFF when the output is more negative than $-V_R$. The resulting PFM of the clock applied to the charge pump has a high frequency spectral content consisting only of clock harmonics. When using an external clock, the transient noise is then synchronized to the clock and is easier to filter in sensitive applications.

The TC1142 also can be used as a -1x boost/buck regulator by omitting the C2 capacitor and connecting the C2– pin to $V_{OUT}$.

The PFM control scheme minimizes supply current at small loads and permits the use of low value flying capacitors, which saves on printed circuit board space and cost. Due to the TC1142's doubling and inverting charge pump mechanism, the output voltage is limited to $-2V_{IN}$. To produce a -5V regulated output, for example, a minimum input voltage of 2.5V is required at $V_{IN}$.

The CCLK pin of the TC1142 has three functions: It can select the internal 200kHz oscillator (when held HIGH), put the TC1142 into shutdown (when held LOW), or provide an external clock input. To achieve this functionality, an internal counter is reset by any positive transition at the CCLK pin, but will time out in typically 160 µsec (i.e., a frequency higher than about 3kHz). If the counter times out following the last positive transition, then the internal clock will be gated through to the charge pump if CCLK is HIGH, or the device will enter shutdown mode if it is LOW. To enter shutdown, CCLK must be LOW and the counter must have timed out. These timing diagrams are shown in Figure 3-4.

A functional circuit diagram of the TC1142 is shown in Figure 3-1. The output voltage $V_{OUT}$ is compared to an on-chip reference voltage, and the comparator output is used to gate the charge pump clock. The charge pump is a negative voltage doubler and has two phases of operation which are further illustrated in Figure 3-2 and Figure 3-3. In phase 1, shown in Figure 3-2, the flying capacitor C1 charges the flying capacitor C2 while the device load is totally serviced by the charge stored on the reservoir capacitor $C_{OUT}$. In phase 2, shown in Figure 3-3, the capacitor C1 is recharged to $V_{IN}$ while the capacitor C2 transfers its charge to the reservoir capacitor $C_{OUT}$.

In normal operation, the TC1142 charge pump stays in phase 2 and only switches to phase 1 as required to maintain output voltage regulation.

**FIGURE 3-1: FUNCTIONAL CIRCUIT DIAGRAM**

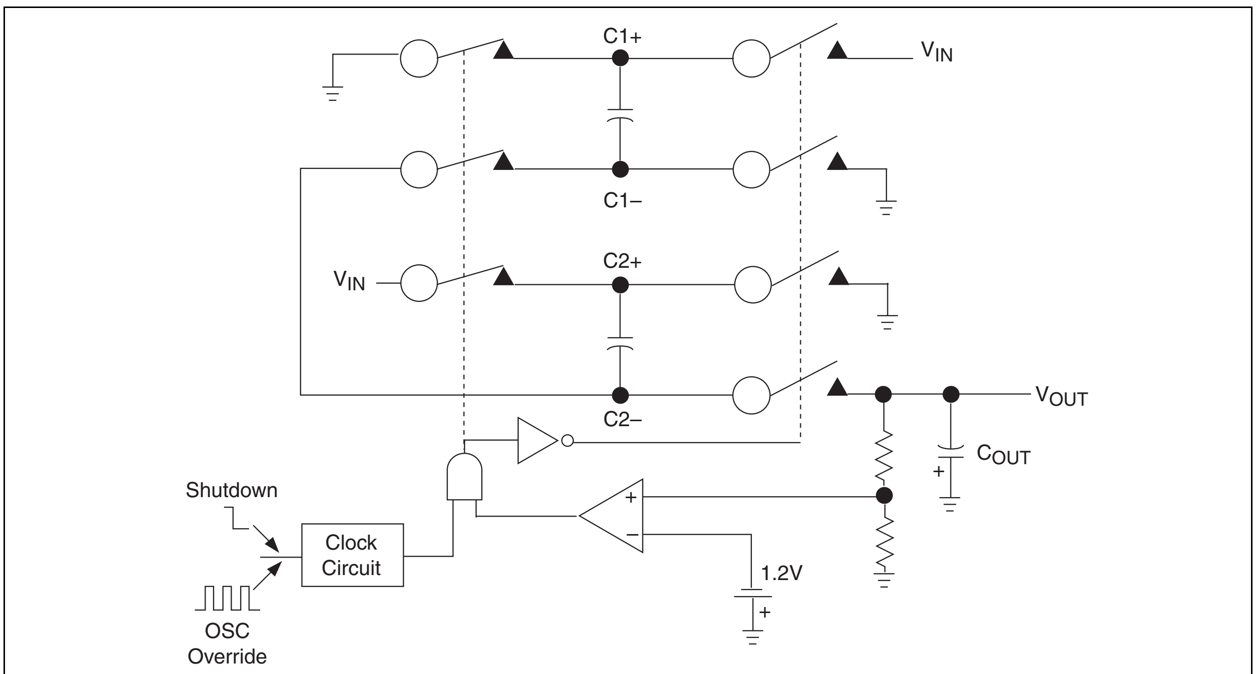
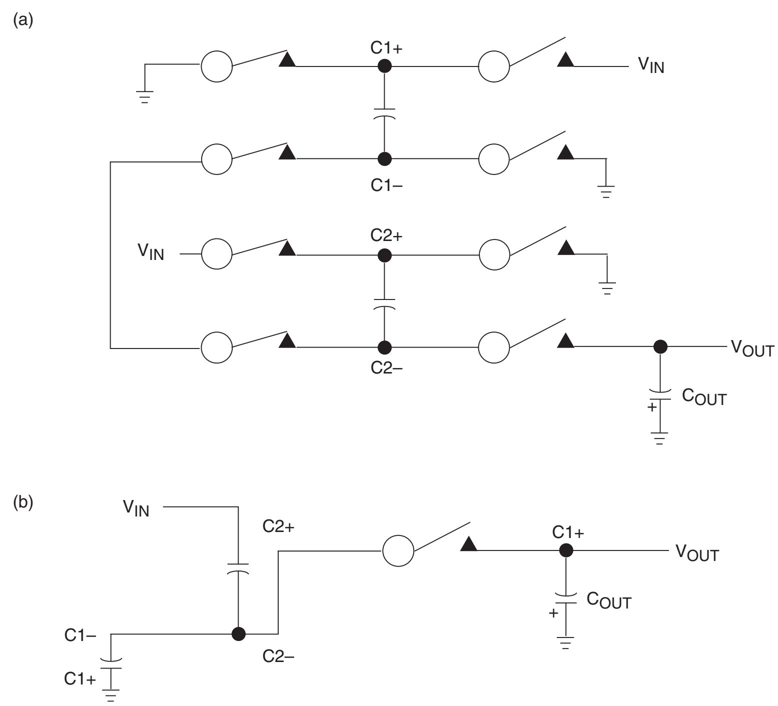
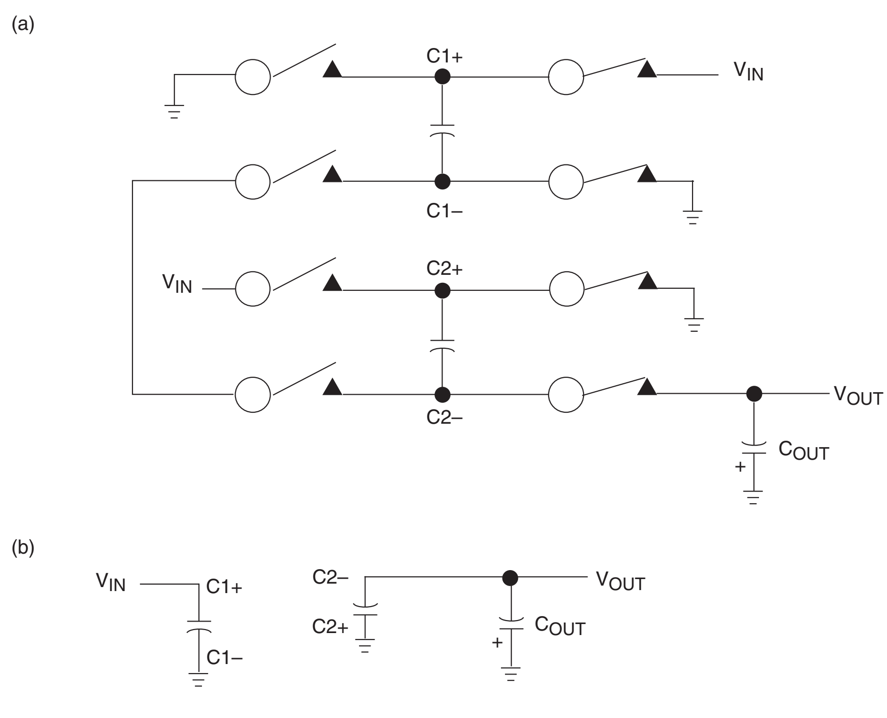


**FIGURE 3-2: TC1142 PHASE 1**




(a) Switch positions during phase 1.
(b) The equivalent circuit of the charging phase of operation.

**FIGURE 3-3: TC1142 PHASE 2**




(a) Switch positions during phase 2.
(b) The equivalent circuit of the discharging phase of operation.

## 3.1 Output Voltage and Ripple

For a -2x boost:

a.) For unregulated operation when $V_{IN} \leq \left|\frac{V_R}{2}\right|$.

In this case, the output voltage is given by:

**EQUATION 3-1:**

$$V_{OUT} = -|2V_{IN}| + I_O R_{OUT}$$

$$\text{where } R_{OUT} = \frac{1}{f}\left(\frac{1}{C1} + \frac{1}{C2}\right) + \frac{R_S C2}{(C2 + C_{OUT})}$$

Here, f is the clock frequency and $R_S$ is the total ON resistance of the switches connecting C2 to GND and $V_{OUT}$ in phase 2 of the charge pump operating cycle with the equivalent series resistance (ESR) of C2.

The output ripple voltage is given by:

**EQUATION 3-2:**

$$V_{RIPPLE} = I_O R_{RIPPLE}$$

$$\text{where } R_{RIPPLE} = \frac{1}{2f(C2 + C_{OUT})} + \frac{1}{2fC_{OUT}} + \frac{ESR\ C2}{(C2 + C_{OUT})}$$

Here, ESR is the equivalent series resistance of $C_{OUT}$.

b.) For regulated operation when $V_{IN} > \left|\frac{V_R}{2}\right|$.

In this case, the TC1142 is held in phase 2 until the output voltage drops below $V_R$. When this occurs, the TC1142 reverts to phase 1 for a half period of the clock, during which C2 is charged from C1. At the end of this half-period, C2 is reconnected to $C_{OUT}$ to boost the output voltage. During the phase 1 time period, the output voltage will drop below $V_R$ before it is boosted back, so the minimum output voltage is approximated by:

**EQUATION 3-3:**

$$V_{OUTMIN} = -|V_R| + I_O R_{OUT}$$

$$\text{where } R_{OUT} = \frac{1}{2fC_{OUT}} + \frac{ESR\ C2}{(C2 + C_{OUT})}$$

The output ripple voltage is given approximately by:

**EQUATION 3-4:**

$$V_{RIPPLE} = \frac{(2V_{IN} - |V_R| + ESR\ I_O C2\left(\frac{1}{C1} + \frac{1}{C2}\right))}{N}$$

$$\text{where } N = \left(\frac{1}{C1} + \frac{1}{C2}\right)(C2 + C_{OUT})$$

For values of $V_{IN}$ higher than $|V_R/2|$ by several hundred mV, the effect on ripple of the ESR of $C_{OUT}$ can be neglected compared to the “overdrive” effect of $V_{IN}$.

Here, it can be seen that $V_{RIPPLE}$ increases with increasing $V_{IN}$, but can be minimized by choosing small C1 and C2 values and a large $C_{OUT}$ value.

## 3.2 Capacitor Selection

To maintain low output impedance and ripple, it is recommended that capacitors with low equivalent series resistance (ESR) be used. Additionally, larger values of the output capacitor and smaller values of the flying capacitors will reduce output ripple. For a capacitor value of 4.7µF for $C_{OUT}$, and values of 0.47µF for C1 and C2, the typical output impedance of the TC1142 in regulation is 0.5Ω. For the capacitor ESR not to have a noticeable effect on output impedance, it should not be larger than $1/2fC_{OUT}$. This also makes its effect on ripple voltage negligible. For $V_{IN}$ = 3.2V and $V_R$ = -5V, the output ripple voltage is less than 70 $mV_{PP}$. Table 3-1 summarizes output ripple versus capacitor size for an input voltage of 3.2V and a regulated output voltage of -5V.

Surface mount ceramic capacitors are preferred for their small size, low cost and low ESR. Low ESR tantalum capacitors also are acceptable. See Table 3-2 for a list of suggested capacitor suppliers.

**TABLE 3-1: VOLTAGE RIPPLE VS. C1/C2 FLYING CAPACITORS AND OUTPUT CAPACITOR $C_{OUT}$ ESR = 0.1Ω, $I_{OUT}$ = 20mA**

| C1, C2 (µF) | $C_{OUT}$ (µF) | $V_{IN}$ (V) | $V_{OUT}$ (V) | $V_{RIPPLE}$ (mV) |
|---|---|---|---|---|
| 0.1 | 4.7 | 3.2 | -5 | 14.6 |
| 0.22 | 4.7 | 3.2 | -5 | 31.4 |
| 0.33 | 4.7 | 3.2 | -5 | 46.1 |
| 0.47 | 4.7 | 3.2 | -5 | 63.9 |
| 0.68 | 4.7 | 3.2 | -5 | 88.7 |
| 1.0 | 4.7 | 3.2 | -5 | 123.2 |
| 0.1 | 10 | 3.2 | -5 | 7.0 |
| 0.22 | 10 | 3.2 | -5 | 15.1 |
| 0.33 | 10 | 3.2 | -5 | 22.4 |
| 0.47 | 10 | 3.2 | -5 | 31.5 |
| 0.68 | 10 | 3.2 | -5 | 44.7 |
| 1.0 | 10 | 3.2 | -5 | 63.8 |

**TABLE 3-2: LOW ESR SURFACE-MOUNT CAPACITOR MANUFACTURERS**

| Manufacturer | Type | Phone |
|---|---|---|
| AVX Corp. | TPS series surface-mount tantalum<br>X7R type surface-mount ceramic | 803-448-9411 |
| Matsuo | 267 series surface-mount tantalum<br>X7R type surface-mount ceramic | 714-969-2491 |
| Sprague | 593D, 594D, 595D series surface-mount tantalum | 207-324-4140 |
| Murata | Ceramic chip capacitors | 800-831-9172 |
| Taiyo Yuden | Ceramic chip capacitors | 800-348-2496 |
| Tokin | Ceramic chip capacitors | 408-432-8020 |

## 3.3 Power Efficiency

Assuming the output is loaded with at least 20% of the maximum available output current, the power efficiency of the TC1142 can be estimated using the following equation:

**EQUATION 3-5:**

$$\eta = \frac{|V_R|}{2(V_{IN})}$$

For example, a 3.2 Volt $V_{IN}$, and a -5 Volt $V_R$ will have an efficiency of approximately 78%. For loads less than 20% of the maximum available output current, the power efficiency will be substantially reduced. Other factors that affect the actual efficiency include:

1. Losses from power consumed by the internal oscillator (if used).
2. $I^2R$ losses due to the on-resistance of the MOSFET charge pump switches.
3. Charge pump capacitor losses due to ESR.
4. Losses that occur during charge transfer (from the flying capacitors to the output capacitor) when a voltage difference exists between these capacitors.

## 3.4 Choice of -2x or -1x Connections

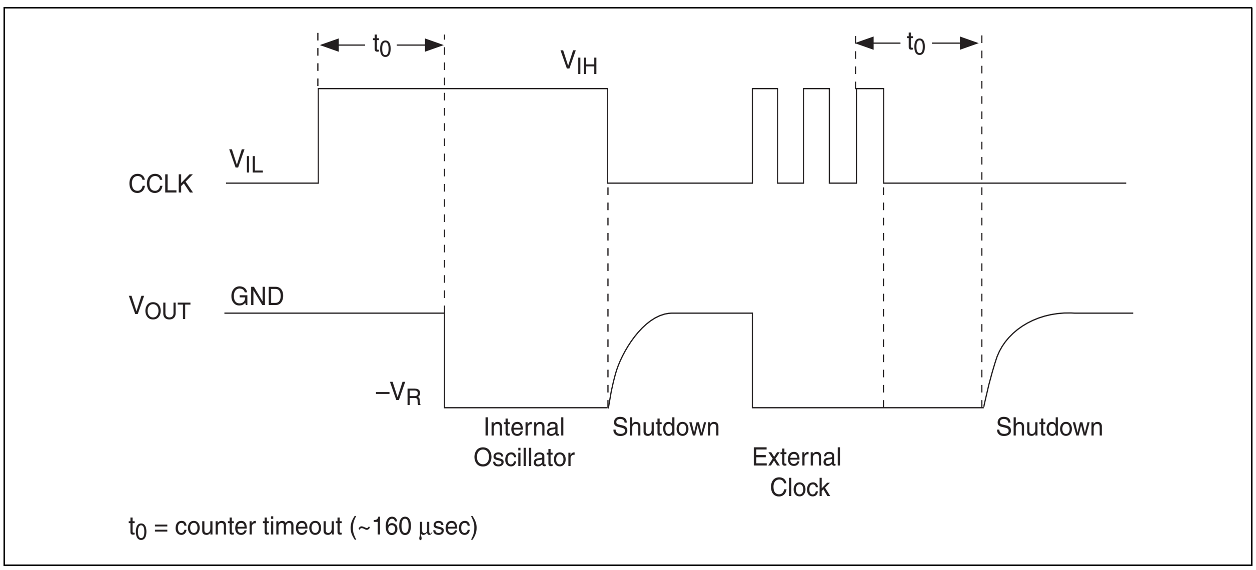
If required output voltage can be achieved using a -1x configuration then this is preferred for the following reasons:

1. Power efficiency is improved from $V_R/2V_{IN}$ to $V_R/V_{IN}$
2. Only one flying capacitor needed
3. The output ripple becomes proportional to $V_{IN} – V_R$ rather than $2\ V_{IN} – V_R$.

## 3.5 Layout Considerations

Proper layout is important to obtain optimal performance. Mount capacitors as close to their connecting device pins as possible to minimize stray inductance and capacitance. It is recommended that a large ground plane be used to reduce noise leakage into other circuitry.

**FIGURE 3-4: TIMING DIAGRAM**



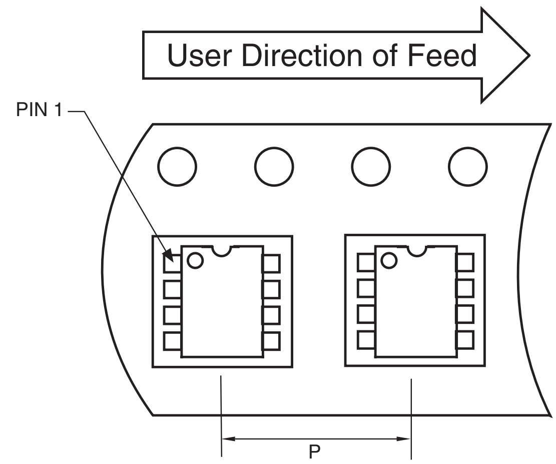
# 4.0 PACKAGING INFORMATION

## 4.1 Package Marking Information

Package marking data not available at this time.

## 4.2 Taping Form

**Component Taping Orientation for 8-Pin MSOP Devices**



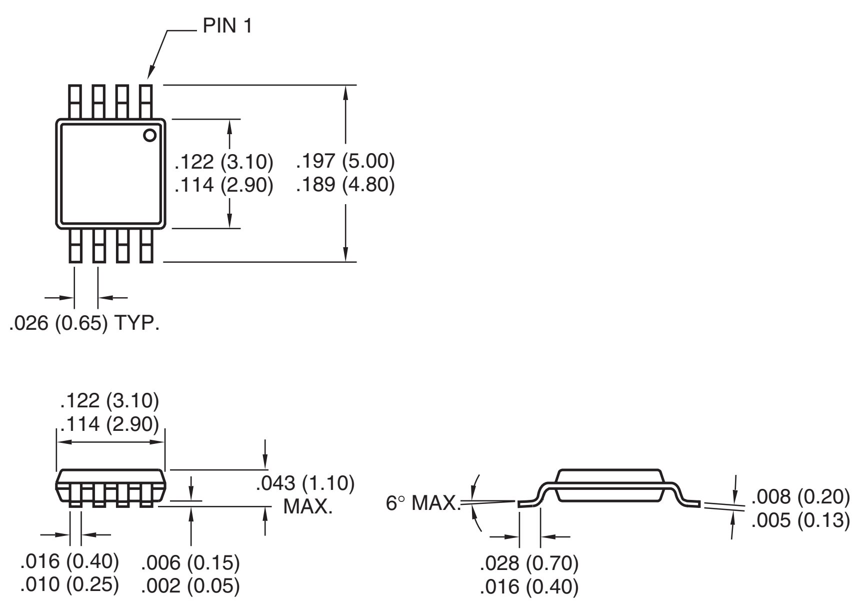

Standard Reel Component Orientation for TR Suffix Device

**Carrier Tape, Number of Components Per Reel and Reel Size**

| Package | Carrier Width (W) | Pitch (P) | Part Per Full Reel | Reel Size |
|---|---|---|---|---|
| 8-Pin MSOP | 12 mm | 8 mm | 2500 | 13 in |

## 4.3 Package Dimensions

**8-Pin MSOP**




**Dimensions: inches (mm)**

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