TB3071

Voltage-Controlled Oscillator with Linear Frequency Output

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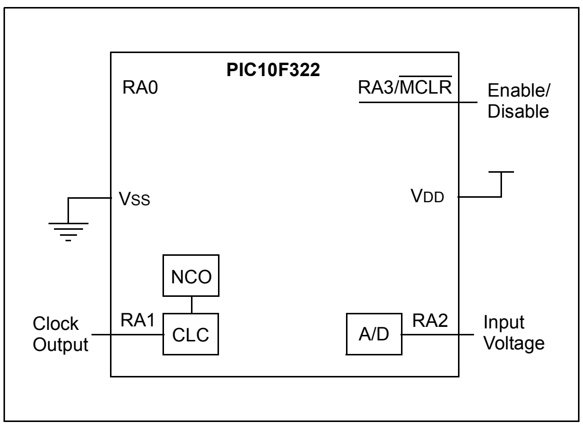
INTRODUCTION

In this technical brief, a PIC10F322 is being used to implement a simple voltage-controlled oscillator (VCO). Output frequencies range from 16 Hz to 500 kHz, with an internally generated clock source (no external crystal required). The VCO operates from a supply voltage of 2.3 to 5.5V, with current consumption of approximately 2.4 mA (5.0V VDD).

This example illustrates the use of the Analog-to-Digital Converter (ADC), and the Numerically Controlled Oscillator (NCO). Also, the Configurable Logic Cell (CLC) is being used to re-route the NCO output signal and make use of its dynamic update capabilities.

The voltage present on the RA2 pin controls the frequency of the clock output. The RA3/MCLR pin enables/disables the clock output on the RA1 pin. The application makes use of the Configurable Logic Cell (CLC) to re-route the NCO output signal to the RA1 pin. The RA0 pin is available to the user for alternate I/O functions, if desired.

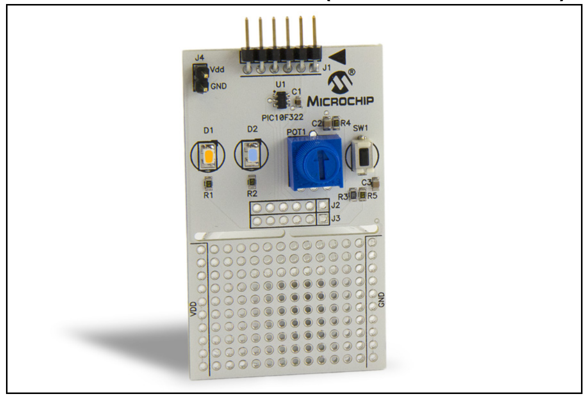
FIGURE 1: PIC10F322 PIN CONNECTIONS



The application has been developed with the low-cost PIC10F322 demo board (part #AC103011). It should be noted that the PIC10F322 (and its associated development board) does not have debug capabilities. If debug capabilities are required, the external debug header (part # AC244045) should be sourced for development.

The on-board potentiometer (POT1) provides the analog input voltage and the clock output can be disabled by pressing the push-button switch (SW1). As the potentiometer is rotated, the frequency at which D1 blinks will change.

FIGURE 2: PIC10F322 DEVELOPMENT BOARD (PART # AC103011)



For flexibility, the VCO has been written in both assembly and 'C'. The assembly language version uses only 60 locations of program memory and 1 RAM location have been used. Language tool versions: MPASMWIN.exe v5.45, mplink.exe v4.43, mplib.exe v4.43. The assembly version can be found in **"Appendix A – VCO.asm"**, Figure A1 (Part 1 of 2). The 'C' version can be found in **"Appendix A – VCO.asm"**, Figure A1 (Part 2 of 2).

In order to re-route the NCO output (normally present on RA2) to the RA1 pin, we are using the Configurable Logic Cell (CLC) module. The CLC Designer Tool GUI allows easy configuration of the CLC block. The diagram below (Figure 3) shows how the "NCO" signal is routed to the output of the CLC1 block.

Note that the output of "Gate 1" has been inverted. This creates a "`1`" at the output. However, when the output signal is disabled (via the RA3/MCLR pin), the application removes the inversion at the output of "GATE 1". This illustrates that the CLC module is "dynamic" – you are not forced to keep the configuration that is created initially and can modify signal inputs "on the fly".

The NCO (Numerically Controlled Oscillator) comprises a 16-bit increment register which feeds a 20-bit accumulator. When the 20-bit accumulator overflows, the clock output toggles (as used in this application).

Due to successive remainders being added together in the accumulator, eventually you will get a pulse which is "one clock short". While in some systems, this property would be referred to as "jitter", and would be undesirable, it can be used advantageously by the designer for precise control of how much energy is delivered to a given load.

FIGURE 3: CLC DESIGNER TOOL – OUTPUT OF 'NCO' SIGNAL

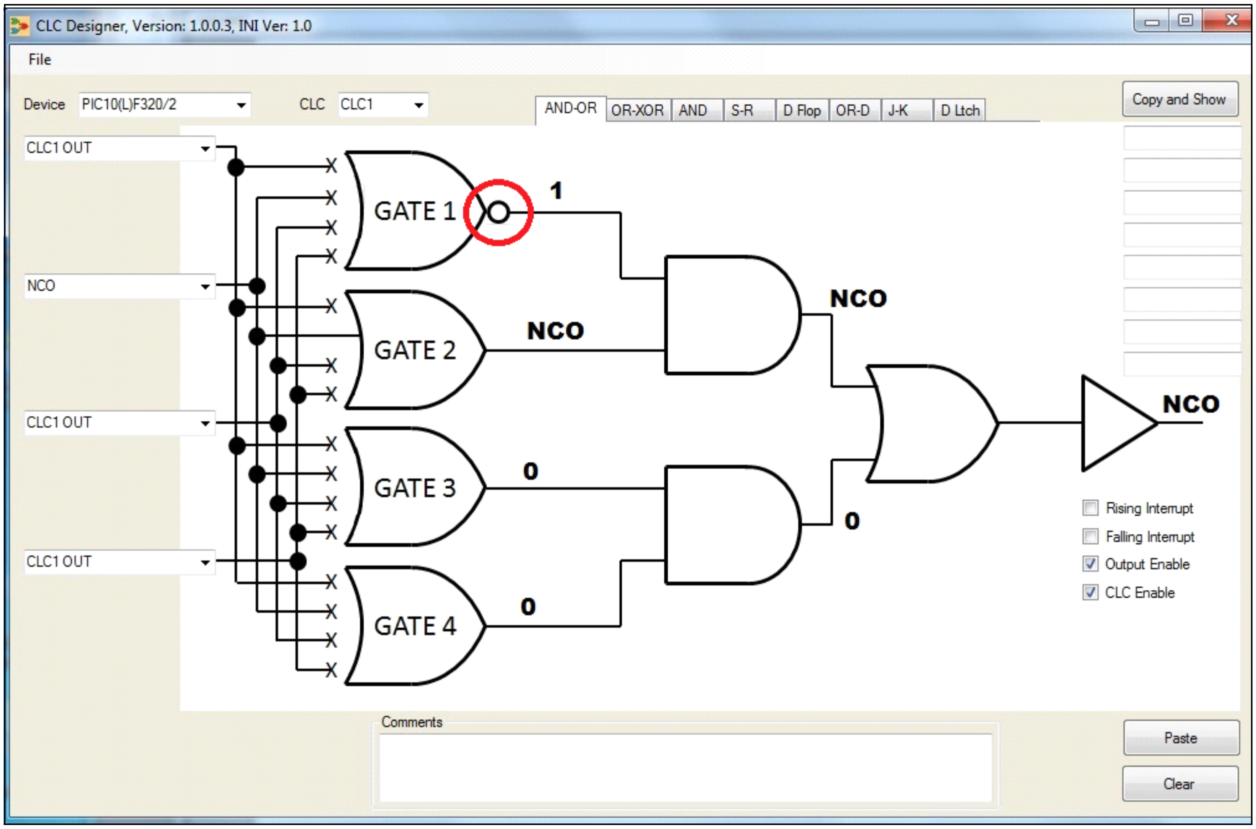
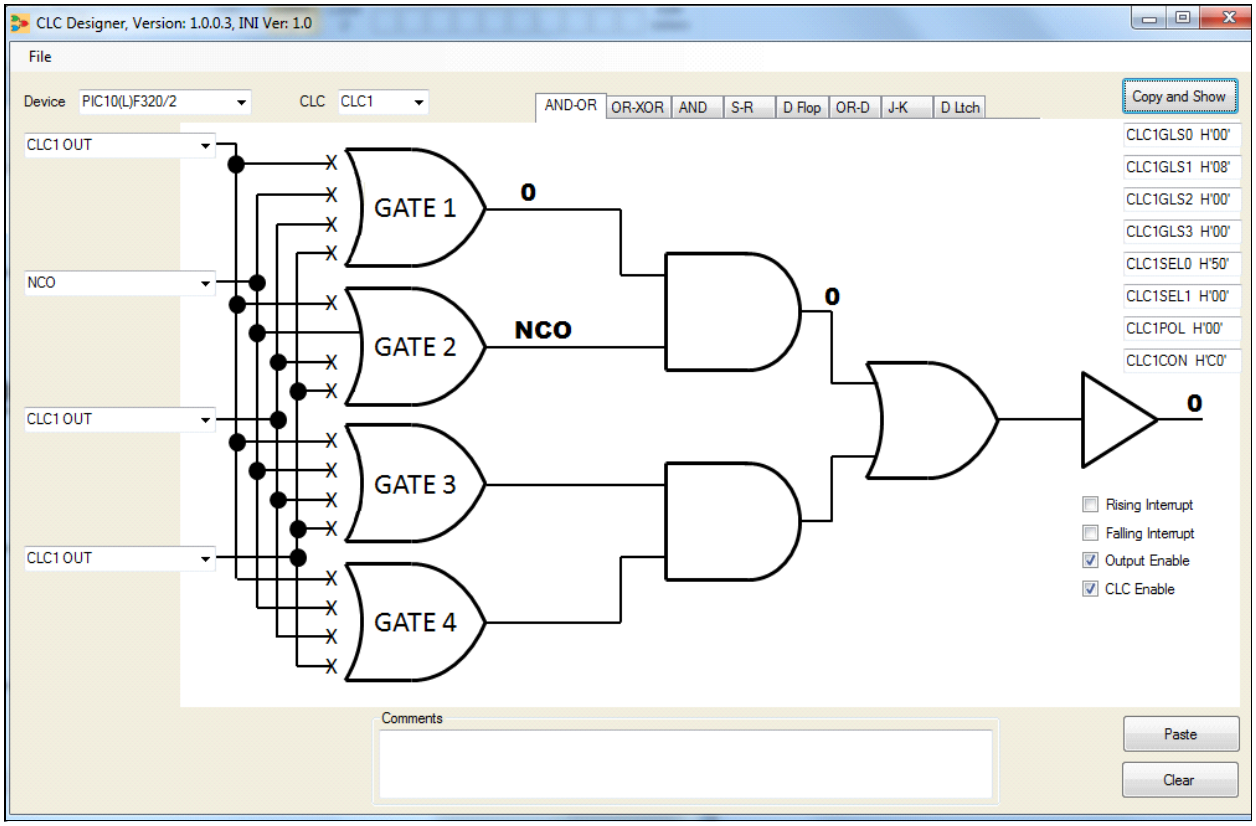


FIGURE 4: CLC DESIGNER TOOL – OUTPUT FORCED TO '0'



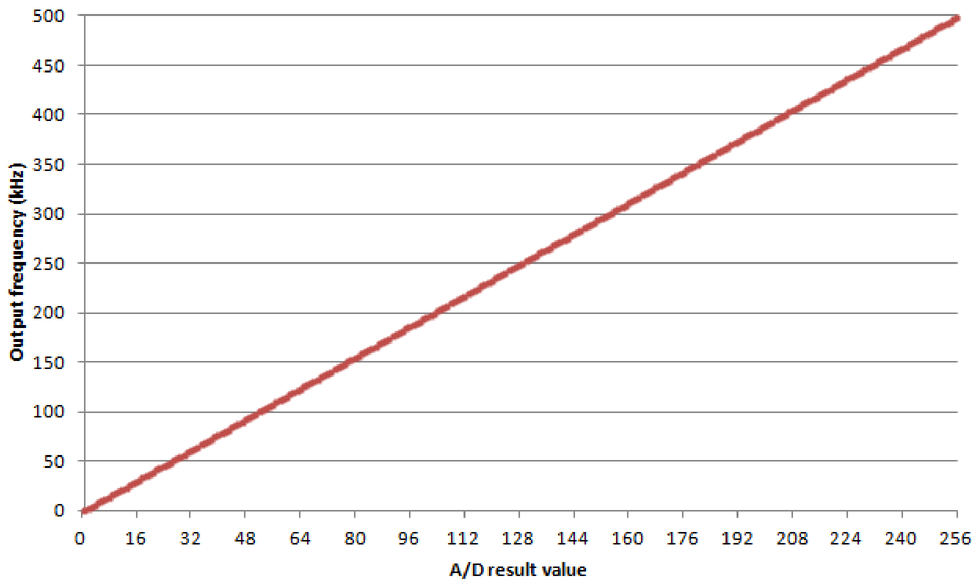
The use of the NCO in conjunction with "Fixed Duty Cycle" mode creates an output with a linear frequency response. This is in contrast with a PWM peripheral, which would create a linear period response. Because the NCO increment register is a 16-bit wide register, and the A/D result register is 8-bits wide, the upper byte of the NCO increment register (NCO1INCH) is loaded with the A/D result. A special case exists for A/D results, which result in zero as a value. In this case, the high byte is loaded with `0x00`, and the lower byte is loaded with `0x01` to produce the lowest possible frequency (16 Hz).

The output frequency can be calculated with the following formula (with FOSC = 16 MHz):

EQUATION 1:

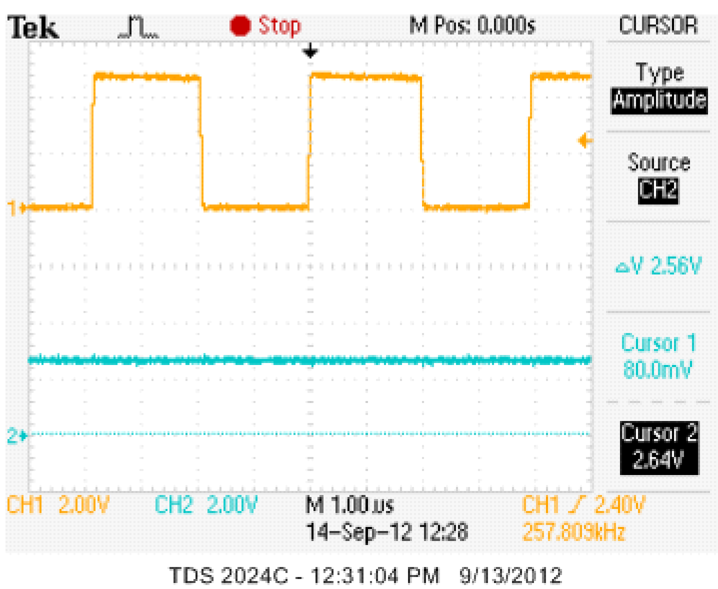
$$f = \frac{Fosc \times ADRES \times 256}{2^{21}}$$

FIGURE 5: OUTPUT FREQUENCY VS. A/D RESULT VALUE



The scope shot below (Figure 6) shows the clock at 250 kHz with RA2 input voltage = 2.56V. VDD = 5.12V for this example.

FIGURE 6: VCO OUTPUT CLOCK AND ANALOG INPUT SIGNAL



The VCO as described in this tech brief demonstrates many of the capabilities of the PIC10F322 ranging from A/D, configurable logic, to the Numerically Controlled Oscillator. The generation of a linear transfer function for the output clock has advantages in simplifying control system design.

The PIC10F322 is one of Microchip's lowest cost parts, and it is our hope that the code provided can serve as a starting point for your application, if not used directly.

APPENDIX A – VCO.ASM

`VCO.asm` is the assembly language source code for the Voltage Controlled Oscillator.

FIGURE A1: PART 1 OF 2

```
#include <p10f322.inc>

     list p=p10f322

     ; PIN_CLC1 is being used for NCO output.
#define PIN_CLC1 PORTA,1
     ; PIN_OE is the pin that is used for output enable
#define     PIN_OE     PORTA,3
     ; TACQ is the number of loops that will be executed for A/D conversion acquisition time
#define     TACQ     0x30
     ; countdown_timer is the RAM location used for countdown timer.
#define     countdown_timer     0x40

;; Configuration Fuses

     __config  _FOSC_INTOSC & _BOREN_OFF & _WDTE_OFF & _PWRTE_OFF & _MCLRE_OFF & _CP_OFF & _WRT_OFF &
_LVP_OFF

;; pin-out
;; 1 - RA0 - user defined output - useful for scope trigger or other indicator signals.
;; 2 - VSS
;; 3 - RA1 - NCO output routed to this pin through CLC block
;; 4 - RA2 - Analog input for VCO
;; 5 - VDD
;; 6 - MCLR/RA3 - enable/disable signal


     org     0x00

start

     bcf          LATA,1                        ; RA1 output low by default.
     movlw     0x0C
     movwf     TRISA                        ; RA3, RA2 input; RA1, RA0 output
     movlw     0x04
     movwf     ANSELA                        ; RA2 analog, RA1 and RA0 are digital.
     movlw     0x70
     movwf     OSCCON                       ; 16 MHz clock - change this value to change clock frequency
                                             ; and to lower current consumption.

     #include "pass-through.inc"          ; routes NCO output to the RA1 pin.

     bcf          NCO1CLK,N1CKS1               ; this sets the FOSC as input for the NCO
     bsf          NCO1CLK,N1CKS0               ; rev. A of the datasheet is incorrect for the N1CKSx
settings,
                                             ; but is shown correctly in the errata

     bsf          NCO1CON,N1EN               ; enable NCO module

     movlw     0xc8
     movwf     ADCON                        ; select AN2 analog input channel, div by 64 clock
     bsf       ADCON,ADON                   ; turn on A/D
```

FIGURE A1: PART 1 OF 2 (CONTINUED)

```
     btfss     PIN_OE                          ; Is output enabled?
     goto     output_disabled                ; No.

output_enabled
     movlw     TACQ                           ; load acquisition time
     movwf     countdown_timer                 ; to countdown timer
tacqdelay
     decfsz     countdown_timer                 ; Has countdown timer expired?
     goto     tacqdelay                     ; No - continue to wait.
     bsf         ADCON,GO_NOT_DONE             ; Yes - start A/D conversion.

a2dconversion
     btfsc     ADCON,GO_NOT_DONE           ; Am I done with the A/D conversion?
     goto     a2dconversion                ; No.
     movf     ADRES,W                          ; Yes - move A/D result to
     btfsc     STATUS,Z                      ; Was A/D result = 0?
     goto     minimum_frequency           ; Yes.

     movwf     NCO1INCH                      ; NCO increment high register = ADRES
     movlw     0x00
     movwf     NCO1INCL                      ; and this causes the update to occur.
     bsf         NCO1CON,N1EN                  ; enable NCO1 module after update of NCO1INCx registers.
     goto     enable_check

minimum_frequency
     clrf     NCO1INCH                     ; A value of 0 would cause the NCO to never overflow.
     movlw     0x01                            ; A value of 1 gives the minimum frequency.
     movwf     NCO1INCL

enable_check
     btfsc     PIN_OE                          ; Is output disabled?
     goto      output_enabled                ; No.

output_disabled                                ; Yes.
     bcf         CLC1POL,LC1G1POL            ; clear inversion at "GATE 1" output to disable output
     btfss     PIN_OE                          ; has output been re-enabled?
     goto     output_disabled                ; No.

     bcf         NCO1CON,N1EN                  ; Yes - disable NCO,
     clrf     NCO1ACCU                     ; and clear out accumulator so that I get clean start-up.
     clrf     NCO1ACCH
     clrf     NCO1ACCL
     bsf         CLC1POL,LC1G1POL            ; set inversion at "GATE 1" output to enable "NCO" signal
output
     goto     output_enabled




     end
```

FIGURE A1: PART 2 OF 2

```
#include "pic.h";

__CONFIG (FOSC_INTOSC & BOREN_OFF & WDTE_OFF & PWRTE_OFF & MCLRE_OFF & CP_OFF & WRT_OFF & LVP_OFF);

#define PIN_CLC1        PORTA1
#define PIN_OE          PORTA3
#define TACQ            0x30

void main(void)
{
    // acquisition timer workspace
    char i;

    // initialization
    OSCCON = 0x70;  // 16 MHz
    LATA1  = 0;     // RA1 is freq output. Set latch output to 0.
    TRISA  = 0x0C;  // RA0,1 = outputs, RA2,3 = inputs
    ANSELA = 0x04;  // RA2 = analog input

    // CLC design output in C format
    #include "pass-through_C.inc";

    // set Fosc as NCO input and enable NCO
    // Note: Rev A of the data sheet has some clock source settings identified improperly
    //       See Errata document DS80529 for alternate clock clock source settings
    N1CKS1 = 0;
    N1CKS0 = 1;
    N1EN   = 1;

    // ADC: TAD = Fosc/32 (2 us), AN2 input, enabled
    ADCON  = 0x48;
    ADON   = 1;

    while(1)
    {
        // switch output on
        LC1G1POL = 1;

        // continue to read ADC and set NCO freq
        // as long as input pin is high
        while(PIN_OE == 1)
        {
            // wait for specified acquistion time
            for(i=TACQ;i!=0;i--);
            // start ADC and wait for result
            GO_nDONE = 1;
            while(GO_nDONE == 1);
            // if result is zero set minimum freq
            // otherwise set freq to ADC result
            if(ADRES == 0)
            {
                NCO1INCH = 0;
                NCO1INCL = 1;
            }
            else
            {
                NCO1INCH = ADRES;
                NCO1INCL = 0;
             }
        }

        // input pin was low - switch output off
        LC1G1POL = 0;
        // wait for pin input high to restart
        while(PIN_OE == 0);
    }
}
```

APPENDIX B – PASS-THROUGH.INC

`PASS-THROUGH.INC` defines the configuration of the Configurable Logic Cell block in assembly code, and was created using the CLC Designer tool.

FIGURE B1: PASS-THROUGH.INC

```
    BANKSEL  CLC1GLS0
    movlw   H'00'
    movwf   CLC1GLS0
    movlw   H'08'
    movwf   CLC1GLS1
    movlw   H'00'
    movwf   CLC1GLS2
    movlw   H'00'
    movwf   CLC1GLS3
    movlw   H'50'
    movwf   CLC1SEL0
    movlw   H'00'
    movwf   CLC1SEL1
    movlw   H'01'
    movwf   CLC1POL
    movlw   H'C0'
    movwf   CLC1CON
```

`pass-through_C.inc` defines the configuration of the Configurable Logic Cell block in 'C' code, and was created using the CLC Designer tool.

FIGURE B2: PASS-THROUGH_C.INC

```
// File: pass-through_C.inc
// Generated by CLC Designer, Version: 1.0.0
// Date: 11/5/2012 8:08 AM
// Device:PIC10(L)F320/2

    CLC1GLS0 = 0x00;
    CLC1GLS1 = 0x08;
    CLC1GLS2 = 0x00;
    CLC1GLS3 = 0x00;
    CLC1SEL0 = 0x50;
    CLC1SEL1 = 0x00;
    CLC1POL  = 0x01;
    CLC1CON  = 0xC0;
```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