MICROCHIP

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Using the ESD Parasitic Diodes on Mixed Signal Microcontrollers

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INTRODUCTION

Microchip application note, AN521 *"Interfacing to AC Power Lines"*, provides a number of guidelines for implementing low-cost, zero cross circuits by relying upon the parasitic ESD diodes in the I/O pins. These guidelines have been used successfully for many years, but, with the increase in analog functionality on the microcontrollers, the simple world in AN521 is now much more complex. Many recent devices are pin-compatible with older devices and can be inserted into an older socket, but the application can now exhibit strange behaviors unless the interaction with the new analog features are understood and avoided.

BACKGROUND

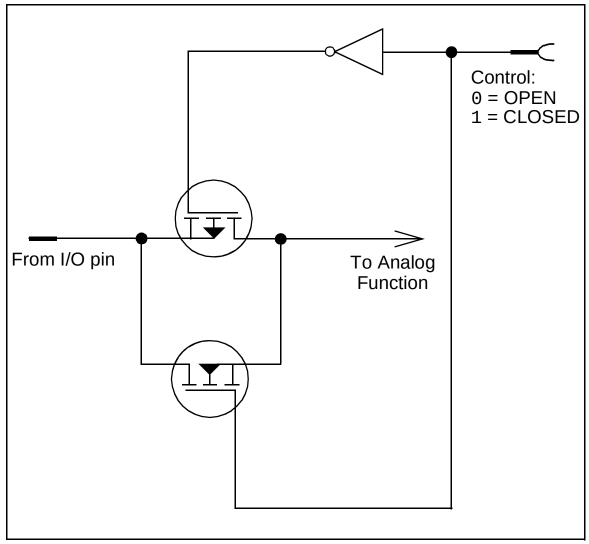
Adding analog to any digital system is an exercise in trade-offs. This is especially true in microcontrollers, where silicon space is at a premium. To reduce the size impact of peripheral circuitry, each analog module is attached to multiple I/O pins by analog pass-gates. This allows the microcontroller firmware to select the required analog input at any time based upon the needs of the application. As the demand for the analog functions goes up, more and more I/O pins are added to the pass-gate array and the probability increases for unexpected behaviors when the data sheet specifications are violated.

The ESD protection diodes shown in the data sheet and discussed in AN521 forward conduct at a voltage of approximately 0.6 to 0.7V. This is reflected in the absolute maximum ratings published in data sheets for older devices. The addition of the analog pass-gates reduces the possibilities of using the voltage clamping ability of the ESD diodes by adding an additional voltage sensitivity described in the next section.

Pass-gates

Pass-gates are simply two CMOS transistors connected in parallel (see Figure 1). The transistors are a P MOSFET and an N MOSFET. This arrangement allows the bidirectional current flow necessary for the proper operation of an analog circuit.

FIGURE 1: PASS-GATE



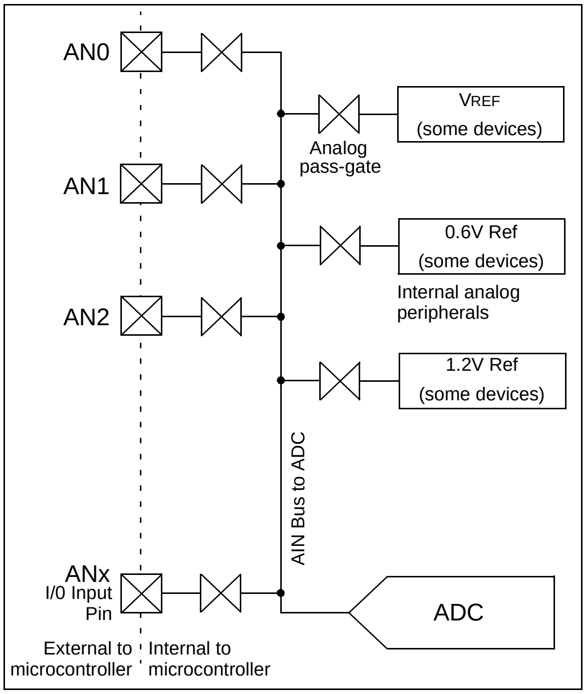
This pass-gate topology works very well and has been used for many years. The only potential problem occurs when the voltage on the I/O pin exceeds V_{DD}. Under these circumstances, the V_{GS} voltage on the PMOS device (the top transistor in Figure 1) becomes negative. PMOS transistors begin to conduct as V_{GS} becomes negative. When the voltage on the I/O pin exceeds V_{DD} by 0.4V (V_{GS} = -0.4V), then the PMOS device has become sufficiently conductive that secondary affects begin to appear. The data sheet absolute maximum voltage on the I/O pin is specified as V_{DD} + 0.3V. Whereas, older devices without analog circuitry specified V_{DD} + 0.6V. This specification is intended to guide engineers towards operating under conditions where the pass-gate operates as expected.

The voltages used in this document are typical values. These voltages tend to decrease with decreasing temperatures and increase with increasing temperatures. Use them as a guideline and not as an absolute value.

ADC Affects

The analog-to-digital converter has a single input that is routed to all the pass-gates of the pins with ADC functionality (see Figure 2).

FIGURE 2: ANALOG-TO-DIGITAL CONVERTER



The pass-gate array connects the analog sources to the ADC. The control logic determines which one of the channels will be seen by the ADC. If one of the analog channels is being driven beyond the specification, then the excess voltage will be added to the voltages on the ADC input, and the voltage seen by the ADC will no longer represent the voltage of the desired channel. The ADC analog pass-gates are bidirectional devices. If a pin is overdriven, a different analog input pin may source current. This will appear as crosstalk between the overdriven input and the selected ADC channel. This can cause problems with external or internal circuits if the overvoltage input is strong enough to affect the signal source.

Comparator Connections

The comparators also have a pass-gate array to select the inputs that are attached to the comparator. The pass-gate array allows overvoltages to appear on the comparator or on the selected comparator input pins. This affects the comparator or causes crosstalk on the I/O pins.

Some comparator inputs, such as the 0.6V reference, are internal. This reference, if present on the device, is the default comparator input after Reset.

LCD

Devices with LCD pins also use a pass-gate array to steer voltages between the V_{LCD} pins and the segment/common drives. Overvoltages applied to a segment or a common can appear on one or more V_{LCD} pins and may cause improper LCD operation or long-term damage.

Oscillator

The internal oscillator is stabilized by a 0.6V reference. Some devices make this reference available to the ADC. If an overvoltage is on V_{DD} while the 0.6V reference is selected for the ADC, the 0.6V reference can shut down. This will stop the internal oscillator until a Reset clears the ADC channel selection.

Some devices have a 1.2V reference. This reference is derived from the 0.6V reference so an overvoltage here can cause the same problems. When the oscillator is stopped by overvoltage, it most often looks like a continuous Reset. This is caused by the WDT triggering a device Reset and then the software reconfiguring the pins to cause the problem.

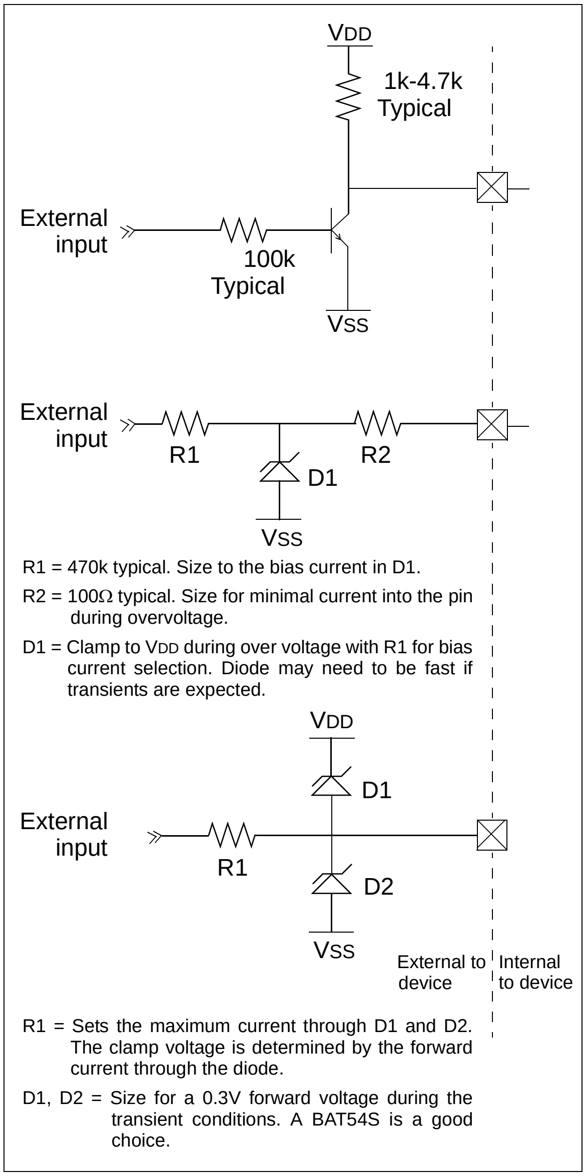
CORRECTIVE ACTION

With an understanding of pass-gates, the solution to the overvoltage input problem can be found.

Protect the Pin

The first solution is to prevent any overvoltage from appearing on the I/O pins of the microcontroller. This can be done by adding Schottky diodes to V_{DD} and from V_{SS} on each pin that could see a high voltage. This will clamp the voltages to V_{DD} + 0.3V, which will not cause the pass-gates to conduct. More protection examples are shown in Figure 3.

FIGURE 3: EXAMPLES OF INPUT PIN PROTECTION



Choose Your Pins Wisely

If the design simply does not allow the extra components, then choosing pins with no analog features is the best choice for overvoltage. Purely digital pins do not have pass-gates, therefore they are not subject to the same constraints. However, future devices with this pinout may have additional analog functions and therefore require a re-evaluation of the circuit and its performance. Never use $\overline{MCLR}$/V_{PP} for a input with overvoltage.

Clever Software

If digital-only I/O pins cannot be chosen and the input pins cannot have the voltage limited, the last option is to fix the problem in the software. One method is to simply drive the overvoltaged pin as an output while the ADC is converting. This will allow the output drivers in the pad to limit the input voltage to V_{DD} or V_{SS}. With the input voltage under control, there are no issues. After the ADC measurements are finished, switch the I/O pin back to an input to make the measurements.

When using this technique, series resistors need to be used to keep the I/O currents within specifications.

Undervoltage

Voltages below V_{SS} are a special case. These voltages cause negative currents in the die substrate. When the die substrate is negatively biased, the silicon structures change from field-effect devices to bipolar devices. All diodes on the die become transistors and shunt currents into the substrate. Many devices will not have adverse affects from this negative voltage. However, if enough current is injected into the device, it is possible to cause latch-up, which is a severe problem and must be corrected externally with diodes or power supply changes. If the device is caught by latch-up, it will consume many milliamps or hundreds of milliamps. This additional current can cause local overheating and hardware failures. Even if latch-up does not occur, the negative current can cause oscillator shifts, or POR Resets. The undervoltage sensitivity increases as the temperature increases, so test your application over the expected temperature range. The best way to handle the undervoltage condition is:

- prevent it with external circuit design, or
- characterize the I/O pins and choose a pin far away from the OSC pins or V_{DD}.
- work with Microchip Sales office to make an I/O pin recommendation.

One word of caution with repeated undervoltage: undervoltage conditions cause degrading damage to the oxide layers on the die. Problems may not appear until the product has been in the field a long time. Degradation is faster with higher current levels.

CONCLUSION

Exceeding the absolute maximum voltage ratio for the device I/O pins may not cause physical damage unless the maximum current specification is also violated. These conditions can be minimized by following the techniques described in this document. Even if the silicon is not damaged, the out-of-specification voltage can cause unexpected application problems. The techniques shown in this application note are not guaranteed to be appropriate for all situations and operating the device outside of the data sheet specification is not supported by Microchip without written documentation. This documentation can be obtained via NSCAR from your Sales office.

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