TB3009

Common 8-Bit PIC® Microcontroller I/O Pin Issues

Author: *Jonathan Dillon*
Microchip Technology Inc.

INTRODUCTION

This technical brief describes solutions for common I/O pin issues for 8-bit PIC® devices (PIC10, PIC12, PIC16 and PIC18).

TABLE 1: QUICK TROUBLESHOOTING GUIDE

Potential I/O Pin Issue	Solution
Cannot drive an output high/low	See **"TRIS Bits"**, **"Functionality on Pins"**, **"Input-Only Pins"**, **"Open-Collector Outputs"**, **"Comparators"**, **"Drive Contention"**, **"Un-Powered Device on the Line"**, **"In-Circuit Debugging"**, **"In-Circuit Serial Programming™"**, **"Manufacturing Error"**.
Input always reads low	See **"Functionality on Pins"**, **"Analog Inputs"**, **"Comparators"**, **"In-Circuit Debugging"**, **"In-Circuit Serial Programming™"**, **"Passing Currents through ESD Protection Diodes"**, **"Manufacturing Error"**.
Line voltage somewhere between logical high and low	See **"Drive Contention"**, **"Un-Powered Device on the Line"**, **"In-Circuit Debugging"**, **"In-Circuit Serial Programming™"**.
When setting an output high, it resets to low	See **"Read-Modify-Write Instructions on Port Registers"**.

TRIS BITS

Whether an I/O is configured as an input or output is determined by its associated TRIS bit in the TRIS register for that port. For example, TRISA0 (TRISA<0>) would configure pin RA0 of PORTA as an input or output. Setting a TRIS bit high sets its associated port pin as an input, providing the TRIS bit is not ignored or overwritten by a peripheral or another Configuration bit. Meanwhile, clearing a TRIS bit sets its associated port pin as an output.

> **Note 1:** For mid-range (14-bit program memory) devices, the TRIS registers are located in register Bank 1, while the PORT registers are located in Bank 0. Having the incorrect bank selected may lead to the TRIS register being modified when the programmer believes they are modifying the PORT register and vice-versa.

> **Note 2:** For baseline (12-bit program memory) devices, the TRIS registers are not mapped to memory and are written to using the TRIS instruction. The TRIS bit settings cannot be read by user code, though they can be examined in a Watch window when using the simulator in MPLAB® IDE.

FUNCTIONALITY ON PINS

The device data sheet defines the functionality of each pin in the chapter dedicated to I/O ports. However, for a quick reference, designers may want to check the pinout and pin descriptions printed in the start of the data sheet. Increasing numbers of features are being embedded into devices which has made a feature or peripheral asserting control over the pin an increasingly common issue.

INPUT-ONLY PINS

On a number of devices, the $\overline{MCLR}$ reset line can be configured as disabled where the line is internally pulled up. This frees the $\overline{MCLR}$ pin for use in an application as an input; typically, GP3 or RA3. The $\overline{MCLR}$ pin is also used to control entry into Programming mode for the microcontroller, where a specific voltage greater than V_{DD} is applied to the $\overline{MCLR}$ pin to enter Programming mode. As a result, the $\overline{MCLR}$ pin does not have an output drive circuit and has an ESD protection system, which operates at higher voltages than that of other I/O pins. If this pin is not used in an application, it should be tied to V_{DD} or V_{SS} through a resistor to prevent it from floating and causing the device to draw excessive current as its input buffer toggles.

> **Note 1:** The TRIS bit for the $\overline{MCLR}$ pin is always set and cannot be cleared.
>
> **2:** The $\overline{MCLR}$ reset can be selected as disabled where is internally pulled up. This is controlled by the Configuration Word bits.

OPEN-COLLECTOR OUTPUTS

On some devices, RA4 is an open-collector output, where it can be driven low, but cannot be driven high since there is no output high driver. The pin needs to be pulled up using an external pull-up resistor. The open-collector output allows voltages greater than V_{DD} to be pulled down by this pin. However, this feature is becoming less common due the newer gate geometries not supporting these higher voltages.

For voltages within the bus rails and of compatible logic levels, open-collector drives can be created from an I/O pin by switching it between a high-impedance input and an output driven low. When the I/O is configured as a high-impedance input, an external pull-up will cause the line to float high. This will configure the pin as a digital output driven low that will pull the line low.

ANALOG INPUTS

All pins which have analog functionality are configured as analog inputs at power-up except on a number of PIC18 devices which have a Configuration bit (PBADEN) to determine if specific pins are analog or digital on Reset. Reading a pin configured as an analog input as a digital input will always return a logical low. Whether a pin is configured as an analog input or a digital I/O is controlled by the ANSEL register(s) or through the ADCON1 and CMCON registers in earlier devices.

COMPARATORS

Many devices have analog comparators which are enabled by default at power-up. If a pin is configured for use by the comparators, the digital input may be disabled. On some devices, the pin is also disabled as a digital output. Whether digital inputs are affected, can be determined from the pin diagrams in the I/O ports chapter of the device data sheet. The comparators are controlled by the CMCON or CMxCON registers.

READ-MODIFY-WRITE INSTRUCTIONS ON PORT REGISTERS

Any instruction where the source and destination of the operation is a PORT register, or for bit sets and clears on the PORT register, there is potential for read-modify-write issues.

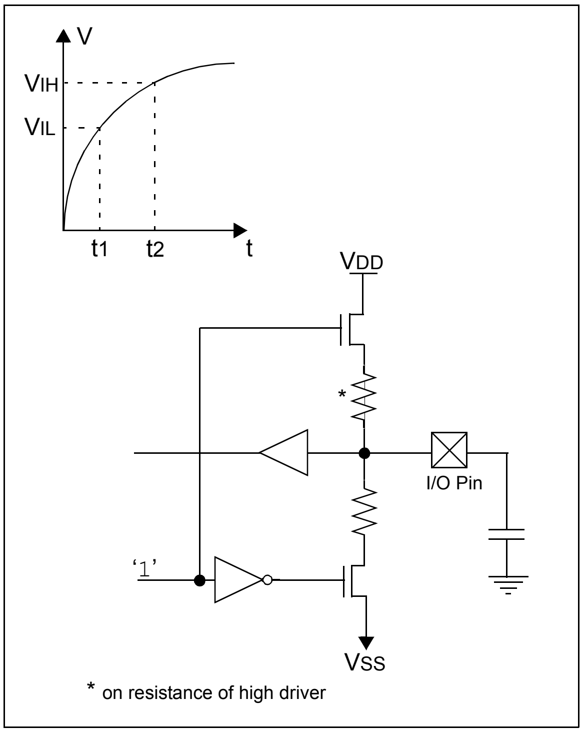
Using a bit operation on a PORT register as an example, there is a read of the register and the byte read is passed in to the processor core where the bit specified is modified. Then, the byte is written back to the register. This all happens in a single instruction and is known as a read-modify-write instruction.

In the base-line and mid-range core, a read of the PORT register is always a read of the input buffers, regardless of whether the pins are configured as inputs or outputs. Capacitive loads and other circuitry on an output may slow the rise and fall times of voltages on the pin such that the pin may not be driven to the logic level specified before a following read-modify-write operation, as can be seen in Figure 1. In this case, the following read-modify-write operation will read the pin as having the previous logic level. This bit is then passed into the processor core as part of the byte read where it is modified, depending on the instruction, and written back to the PORT register, essentially undoing the earlier operation on the port.

Depending on rise and fall times, and speed of operation, this issue may not be apparent when clocking the device at lower frequencies, or single stepping with an emulator or in-circuit debugger. This issue may only appear when executing at higher speeds, where there is insufficient time for the output to charge/discharge.

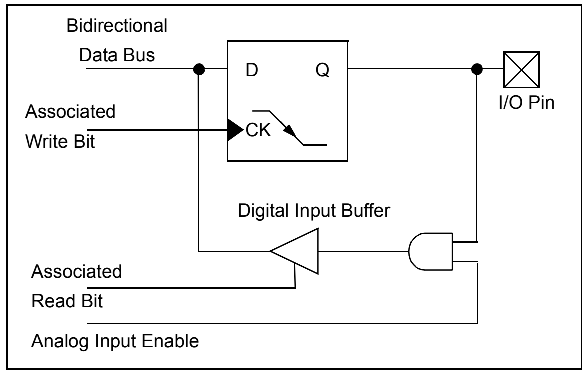
Note:	Many newer devices have output latches for each port, which should be written to when using the output drivers. A read of the PORTx latch register LATx returns the settings of the output drivers, while a read of the PORTx register returns the logic levels seen on the pins. Thus, read-modify-write issues can be avoided in newer devices by ensuring all read-modify-write instructions use the latch registers.

FIGURE 1: RISE TIME OF VOLTAGE ON PIN



Developers may also encounter this issue when a pin configured as an analog input or configured for use with certain peripherals, where its digital input buffer will be disconnected. With the input buffer being disconnected, the associated bit in the PORT register will always read as a logical low. Thus, any read-modify-write operation on any bit in the PORT register will enable the low output driver on this pin, which, typically, would not be the desired operation.

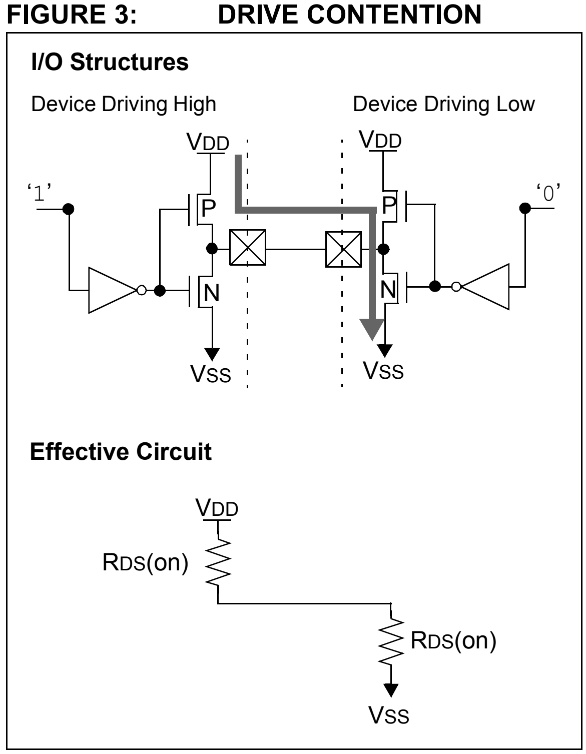
FIGURE 2: SIMPLIFIED FORM OF DIGITAL I/O PIN CIRCUITRY



DRIVE CONTENTION

Two outputs should never attempt to drive the same line, except in an open-collector configuration where both outputs can only pull the line low and the line is externally pulled high by a pull-up resistor. The potential issue of two outputs driving the line is that one output may drive high, while the other is driving low. In this case, the stronger drive should win in this conflict. If both output drives are PIC microcontroller outputs, then they may have a similar strength causing the line to assume a voltage between the two drive levels. Microcontrollers are designed to have as strong drive capability as possible for their technology, with low R_{DS}(on) values, thus, drive contention can cause excessive current draw and can damage or significantly reduce the life span of a device.

FIGURE 3: DRIVE CONTENTION

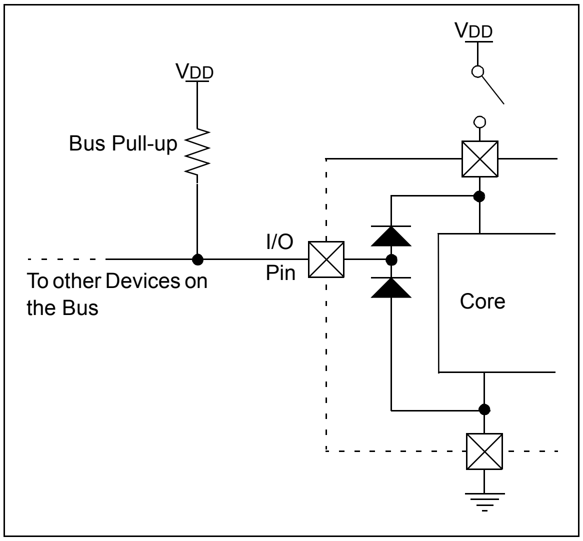


UN-POWERED DEVICE ON THE LINE

The microcontroller may clamp the voltage on a line if it is not powered. On nearly all I/O pins there is a path for current through the ESD protection diodes to the VDD bus inside of the device, where the device would then be powered through the I/O pin. The voltage the line is clamped to is dependent on the resistance of the pull-up or high side driver on the line. However, the ESD protection diode requires a forward voltage of approximately 0.6V to begin passing current, thus the line should be clamped to some voltage above this level. If a line to the microcontroller is clamped on power-up, check to ensure that the microcontroller is powered on all VDD power pins.

Note:	Passing currents through the ESD protection diodes is outside of the operating conditions of the part and the device may not function as expected.

FIGURE 4: CLAMPING LINE THROUGH ESD DIODES



IN-CIRCUIT DEBUGGING

In-circuit debug requires use of the MCLR pin and two I/O for the communications link. For low pin count devices, Microchip provides debug headers for use in place of an actual device with adapters to match the header to the socket or to the surface mount pads of a regular device. The header has a special device with additional pins, which prevents the in-circuit debug I/O requirement from impacting the functionality of the device. For devices without a debug header option, the In-Circuit Serial Programming pins (PGC/ICSPCLK and PGD/ICSPDAT) are dedicated to a serial link to the debugger tool and are not usable by the applications software. Also, MCLR must be configured for External mode and cannot be used as a digital input.

IN-CIRCUIT SERIAL PROGRAMMING™

When using In-Circuit Serial Programming for development or reprogramming of devices, users should ensure that if their programmer releases the MCLR line to allow the device to run, that he also releases the programming clock and data lines (PGC/ICSPCLK and PGD/ICSPDAT). Otherwise, users may encounter drive contention. The programmer usually has greater drive strength than the microcontroller, which can make it appear that a digital output of the microcontroller is not being driven. Programmers may also have internal pull-up or pull-down resistors on the programming lines that may interfere with correct operation of the circuit.

PASSING CURRENTS THROUGH ESD PROTECTION DIODES

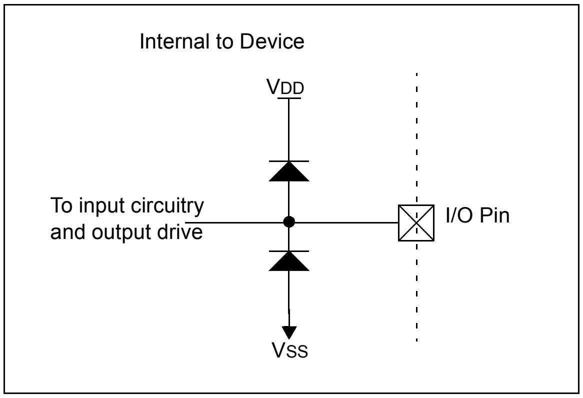
When passing currents through the ESD protection diodes of the device, the internal voltages may be affected causing inputs to be read incorrectly, A/D conversions in process to be disturbed and other unexpected behavior. Common causes of passing sustained currents through the ESD protection diodes are:

- mains “zero cross” circuits which rely on a large series resistor and the protection diodes to clamp the line
- circuits which have an I/O pin driven or pulled up to greater than VDD of the device.

For high noise environments or when a signal needs to be clamped to within the power rails, adding external clamp diodes gives increased current capability and should prevent the device from exceeding operating conditions.

Note:	Passing current through the ESD protection diodes of the device is outside of the operating conditions of the device causing potentially shortened device life span and incorrect functionality

FIGURE 5: ESD DIODE STRUCTURE



MANUFACTURING ERROR

Accidents happen during board design, PCB manufacturing and populating.

To rule out the possibility of cold/dry joints, it is best to check voltages directly on the pins of the device, in some cases desoldering a pin and lifting it to isolate it from the board. By isolating the pin it is easy to determine if the microcontroller is driving the pin and if the expected signals are reaching the pin. It is possible that boards get populated with incorrect value components or of components being left off.

Solder bridges happen while populating the board, especially with fine-pitch devices. However, these often manifest themselves as pins being driven when not expected and pins permanently being low. Measuring the resistance between pins can identify shorts, though inspection will be required to identify the short location.

Flux, if not completely removed from the board, may have a low enough resistance to affect operation of the board, as can moisture improperly applied conformal coatings and potting compounds especially with sensitive analog circuits.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/02/08