Understanding Reset Events On The PIC10F20X

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INTRODUCTION

The PIC10F20X family of microcontrollers utilizes the baseline 12-bit microcontroller core from Microchip. Because this core does not support interrupts, wake-up from Sleep is accomplished by a variety of Reset events within the microcontroller. This technical brief describes how to enable the different sources of Reset and the process of identifying the cause of a Reset.

The possible sources of Reset that can be used to wake the microcontroller from Sleep are shown in Table 1.

TABLE 1: SOURCES OF RESET

Source of Reset	Microcontroller
Power-on Reset	PIC10F200/202/204/206
Watchdog Timer	PIC10F200/202/204/206
$\overline{\text{MCLR}}$ Input	PIC10F200/202/204/206
Change-on-Port Pin GP0/1/3	PIC10F200/202/204/206
Comparator Output Change[1]	PIC10F204/206

Note 1: The Comparator Output Change Reset is limited to the PIC10F204/206. The PIC10F200/202 do not have the comparator.

The following sections outline the process of enabling each source of Reset and the process of identifying the Reset.

POWER-ON RESET (POR)

Condition of Reset: A POR is generated when the device transitions from a power-down condition (VDD < 0.6 VDC typical) to a power-up condition (VDD > 2.0 VDC).

Setup: No programming or configuration bits are needed to enable the POR, it is always enabled.

Testing: A POR condition is determined by testing the $\overline{\text{PD}}$ bit in the Status register. If the $\overline{\text{PD}}$ bit is set, the last Reset was the result of a power-up condition.

Note:	Executing a CLRWDT instruction will also set the $\overline{\text{PD}}$ bit, resulting in a false POR indication. To determine the occurrence of an actual POR condition, the bit must be tested prior to the execution of a CLRWDT instruction or a load of the Option register.

Clearing the Reset: The $\overline{\text{PD}}$ bit is cleared by executing a SLEEP instruction.

WATCHDOG TIMER OR WDT

Condition of Reset: A WDT Reset is generated when the WDT circuit is enabled in the configuration word and the WDT circuit is allowed to time out.

Setup: The WDT circuit must be enabled by setting the WDTE bit in the configuration word. An optional prescaler for the WDT circuit is selected by setting the PSA bit in the Option register. Setting bits PS<2:0> in the Option register sets the prescaler ratio.

Testing: A WDT condition is determined by testing the $\overline{\text{TO}}$ bit in the Status register. If the $\overline{\text{TO}}$ bit is cleared, the last Reset was the result of a WDT time-out. Executing a CLRWDT instruction sets the $\overline{\text{TO}}$ bit, removing the indication of a WDT time-out. To correctly detect an actual time-out condition, the $\overline{\text{TO}}$ bit must be tested prior to the execution of a CLRWDT instruction or a load of the Option register.

Note:	Loading the Option register clears the WDT.

Clearing the Reset: Executing a CLRWDT or SLEEP instruction will set the $\overline{\text{TO}}$ bit.

CHANGE-ON-PORT PIN

Condition of Reset: The logic state of GP0, GP1 or GP3 has changed since the last read and the pin experiencing the logic state change is configured as a digital input.

Setup: The Change-on-Port Reset is enabled by clearing the $\overline{\text{GPWU}}$ bit in the Option register and configuring GP0, GP1 and/or GP3 as inputs.

Note:	While POR, $\overline{\text{MCLR}}$ and WDT can generate a Reset when the microcontroller is running, the Change-on-Port Reset will only cause a Reset if the microcontroller is in Sleep mode.

Testing: A Change-on-Port Reset condition is determined by testing the GPWUF bit in the Status register. If the GPWUF bit is set, the last Reset was the result of a change on the GP0, GP1 or GP3 pins. The GPWUF flag is only available if the $\overline{\text{GPWU}}$ bit has been cleared in the Option register, so the Option register must be configured before a Change-on-Port Reset condition can be tested. However, configuring the Option register generates an automatic clear Watchdog event, which clears both the $\overline{\text{PD}}$ and $\overline{\text{TO}}$ bits. Therefore, it is necessary to test for POR and WDT Reset conditions before testing for a Change-on-Port Reset condition.

Clearing the Reset: To clear a Wake-up Reset caused by a Change-on-Port pin, read the GPIO register and clear the GPWUF bit in the Status register.

COMPARATOR OUTPUT CHANGE

Condition of Reset: The comparator is present, enabled, configured to generate a Reset, and the output state of voltage comparator has changed.

Setup: The Comparator Output Change Reset is enabled by setting the CMPON bit and clearing the $\overline{\text{CWU}}$ bits in the CMCON0 register.

Note 1:	While POR, $\overline{\text{MCLR}}$ and WDT can generate a Reset when the microcontroller is running, the Comparator Output Change Reset will only cause a Reset if the microcontroller is in Sleep mode.
2:	Reset available in PIC10F204/206 only.

Testing: A Comparator Output Change Reset condition is determined by testing the CWUF bit in the Status register. If the CWUF bit is set, the last Reset was the result of a change in the state of the comparator output. The CWUF bit is only available if the CMPON bit is set and the $\overline{\text{CWU}}$ bit cleared in the CMCON0 register, so the CMCON0 register must be configured before a Change-on-Port Reset condition can be tested.

Clearing a Comparator Output Change Reset: To clear this Reset, read the CMCON0 register and clear the CWUF flag in the Status register.

MASTER CLEAR OR $\overline{\text{MCLR}}$

Condition of Reset: The MCLRE bit in the configuration word is set and GP3 has been pulled low.

Setup: The $\overline{\text{MCLR}}$ input is enabled by setting the MCLRE bit in the configuration word.

Testing: There is no bit available to determine a $\overline{\text{MCLR}}$ Reset event. Testing is done by a process of elimination. If a Reset condition occurs and it is not the result of any other Reset source, then the Reset was caused by the $\overline{\text{MCLR}}$ input, provided that the $\overline{\text{MCLR}}$ input has been enabled in the configuration word.

Clearing a $\overline{\text{MCLR}}$ Reset: No action required.

EXAMPLE FIRMWARE

The enclosed example firmware is an example program which can determine and display the source of up to 5 sources of Reset. POR is generated when the circuit is first powered up. The WDT generates a continuous stream of Reset following the POR, unless another Reset is generated.

Note:	The lack of WDT Reset is due to the inclusion of `CLRWDT` instructions in the response programs for the other Resets, not due to a hardware lockout of the WDT Reset.

Three push buttons are used to generate $\overline{\text{MCLR}}$ (SW3), Comparator Output Change (SW1) and Port Change Reset (SW2) conditions. The firmware then indicates the source of the Reset by driving the red and green LEDs. The schematic of the test circuit is provided in Figure 1.

FIGURE 1: TEST CIRCUIT FOR THE EXAMPLE FIRMWARE
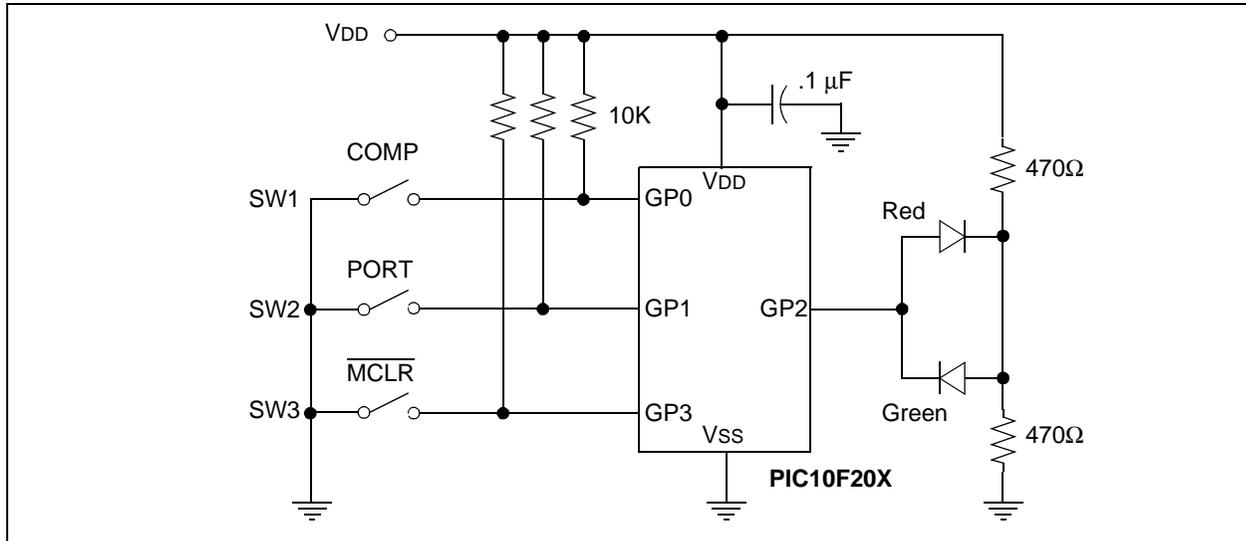
In response to a POR Reset, the firmware lights first the red LED (for 1 second) and then the green LED (for 1 second). Following the LED drive, the firmware executes a SLEEP instruction.

In response to the repeated WDT Resets, the microcontroller toggles the LED drive line resulting in the alternating lighting of the red and green LEDs. After each change in the LED drive line, the firmware executes a SLEEP instruction.

Pressing SW1 grounds the non-inverting input to the comparator causing a change in the comparator output and a Comparator Output Change Reset. In response to the Reset condition, the red LED is turned on for 1 second. The firmware then executes a SLEEP instruction.

> **Note:** During the 1 second red LED time, the WDT is held clear.

Pressing SW2 grounds the GP1 input generating a Port Change Reset condition. In response to the Reset condition, the firmware drives the green LED on for 1 second, before executing a SLEEP instruction.

> **Note:** During the 1 second green LED time, the WDT is held clear.

Pressing SW3 grounds the $\overline{MCLR}$ input generating a $\overline{MCLR}$ Reset condition. In response to the Reset condition, the firmware blanks both LEDs for 1 second before executing a SLEEP instruction.

> **Note:** During the 1 second LED blank time, the WDT is held clear.

The attached listing shows the firmware which implements this operation. It demonstrates enabling and identifying the various Reset conditions. It also provides a template for new applications using these features.

The initial code executed following Reset performs the required testing for each of the five potential Reset causes. If one of more of the Reset conditions are not needed, the appropriate bit test and GOTO instructions can be eliminated from this section.

Following the initial code, sections for each of the Reset conditions are presented.

> **Note 1:** The LED drive portions of these routines are bracketed by comments for the easy substitution of new code.
>
> **2:** The bit set and clear instructions needed to clear the Reset conditions appear after the bracketed LED drive code.
>
> **3:** The only subroutine is the initialization code for the Option, CMCON0 and TRIS registers.

A macro is also included in the listing to generate the needed 1 second delay. This routine may be removed without affecting the operation of the Reset identification and response routines.

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CONCLUSION

The multiple Reset conditions within the PIC10F20X family of microcontrollers provide a wide variety of wake-up from Sleep options. However, careful testing is required to successfully determine the specific Reset condition. The firmware in this technical brief provides an example of how the Reset conditions can be tested, as well as a useful template for new designs incorporating the wake-up from Reset features.

Note 1:	Flash memory usage for the example program is 121 words. The RAM usage is 3 bytes.
2:	The design assumes a PIC10F206 microcontroller.

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08/24/04