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FLASH Memory Technology: Considerations for Application Design

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INTRODUCTION

Many times, choosing a FLASH memory device is driven by which manufacturer has the cheapest offering. Regardless of its use as a stand-alone device or as the program memory of a microcontroller, what is often overlooked are the many key design parameters, or the features that the memory may offer to the application. Endurance, data retention, temperature, operating voltage and frequency, and programming time all play significant roles in the reliability of the device. Selections based on cost alone may be penny-wise but dollar-foolish; the application may be the cheapest on the market but its overall quality can negatively impact the customer's perception and therefore, their future purchases. Carefully balancing these factors can make the difference between an application that's a long term superstar or a one hit wonder.

This technical brief will review the basic operation of Non-Volatile Memory (NVM) cells and the key factors of memory performance that should be considered in the decision making process. We will use these factors to show why Microchip's FLASH technology is such a strong contender in the world of embedded control design.

BASICS OF NVM OPERATION

The reliability of an NVM cell is determined by the technology and process used in its design. Many designs exist because one design cannot satisfy all requirements. Each cell has its own benefits and limitations that are based heavily on the needs of the applications.

All NVM memories use some type of floating gate topology, where the gate is completely encased in an insulator such as oxide. Electrons are moved across the oxide boundary, either on to the gate for programming or off of the gate during an erase. The transistor with the floating gate becomes the bit of memory. Early designs used two transistors for each memory bit, with one transistor being used as the data bit and the other used to select the data transistor. Advances in cell design and process have reduced the memory to a single transistor; this provides a smaller die area but may sacrifice other features.

Program and erase operations are primarily accomplished by two methods. Programming can use either *Channel Hot Electrons* (CHE) or *Fowler-Nordheim tunneling* (FN). Erase operations can use either FN tunneling or *Emission*. CHE uses a combination of gate, drain and source voltages to create sufficient energy for electrons to jump very rapidly from the channel to the floating gate. FN tunneling applies a high voltage to the gate and 0V to the drain, to tunnel electrons onto the floating gate for programming; the voltage potentials are reversed to remove electrons from the floating gate during an erase. Emission is an erase operation only; it occurs on a specially formed area (i.e., a high stress region) in the cell structure where electrons move off the floating gate.

CHE is the primary programming mechanism and is found on most EPROM and FLASH devices. FN tunneling is the primary program and erase method for EEPROMs, and the erase method for some FLASH devices. FN operations tend to produce less stress on the gate insulator than CHE or Emission, and usually result in much higher cell reliability. Table 1 summarizes the various benefits and side effects of each combination

CHE/Emission is predominantly used; while it provides faster programming time and smaller cell areas, it is much more susceptible to both endurance and retention failures. The CHE/FN combination provides an extremely small die area and programming time (in microseconds) but also sacrifices endurance and retention. It also is more susceptible to disturb conditions and therefore, requires additional circuitry to minimize all these effects.

FN/FN solutions provide extremely good performance and reliability but suffer from longer programming times (milliseconds vs. microseconds) and larger die area for array sizes greater than 64 Kbytes. Since over 95% of all 8-bit microcontroller applications run on devices with less than 64 Kbytes, the advantage of a small die area for the CHE/FN design is only useful when tens to hundreds of megabytes of memory space are required. Long programming times can be minimized by implementing block write and block erase operations. Slower programming also tends to decrease the chance of a corruption or write disturb event when compared to cells with ultra-fast programming times; this benefits the overall device reliability.

TABLE 1: COMPARISON OF PERFORMANCE CRITERIA FOR VARIOUS NVM TECHNOLOGIES

Program/Erase Technology / Criteria	FN/FN	CHE/FN	CHE/Emission
Endurance	+++	++	+
Retention	+++	++	+
Disturb	+++	++	+
Cell Area	+	+++	+++
Optimal for arrays < 64 Kbytes	+++	++	++
Manufacturability	+++	+++	+
Cell TPROG	+	+++	+++
Cell TERA	+++	+++	+
Cell Program IDD	+++	+	+
Cell Erase IDD	+++	+++	++

Legend: FN = Fowler/Nordheim, CHE = Channel Hot Electrons, + = acceptable, ++ = better, +++ = optimal

CONSIDERATIONS IN SELECTING AN NVM MEMORY

Endurance

Endurance is the number of erase/write operations that the memory will complete and continue to operate as specified in the data sheet. For NVM cells, endurance is closely tied to both data retention and reliability. This is because the same design features and support circuitry that enhance retention and reliability will also enhance memory endurance. Most manufacturers provide only a single memory, shared by program instructions and data, with an endurance of 100 to 10,000 erase/write cycles and retention of 15 to 25 years. While this may exceed your application's requirements, you have to think about how reliable this NVM cell will perform over time, temperature, and other factors. A memory with greater overall endurance tends to deal with these other factors much better over time.

One side benefit of high endurance, such as that offered with Microchip's PEEC cell, is that infant mortality screening is much more effective. Several thousand erase/write cycles are performed on each device before it leaves the factory. Coupled with a high temperature retention bake, this screening significantly reduces the fallout once the device is populated with the end application.

A parallel concern is how individual bit memories are implemented. Many manufacturers use RAM latches for these, which are then used to implement things like device configuration bits. These tend to be highly susceptible to noise and ESD; should they be corrupted, the device may not be able to recover.

Temperature

Operating temperature has the single greatest impact on the endurance of NVM cells. Devices based on CHE or FN will have worse results when the temperature is hot while Emission devices will show the worst results at cold temperatures. Most manufacturers of 8-bit microcontrollers only specify endurance or retention at 25°C. While this shows the best numbers for the device, it doesn't accurately describe how the device will operate over its entire temperature range. All designers should check the device data sheet to understand how the device will perform at the application's expected temperature range.

Operating Voltage and Frequency

Operating voltage and frequency are closely tied together. Typically, manufacturers will specify bands of operation based on frequency and voltage. Some will even show extended ranges of voltage or frequency for core device operation but limit the availability of certain features (such as the A/D converter or NVM self-writing) to specific ranges of voltage or frequency. In an extreme example, the ability to self-write NVM may be limited to specific and narrow voltage and frequency ranges because of the limited regulation capacity of the on-chip programming charge pump.

Self-Programmability

Besides the ability to generate the programming voltage on-chip, another important feature of self-programming is that the control circuitry provides the proper margin on the cell to read correctly over all specified operating parameters for the device. Some microcontrollers provide the added “benefit” of being able to control the time that high voltage is applied to the memory during erase or program operations. While this may appear to be an advantage, it also requires very careful control of the programming or erase timing. If the time is too short, the NVM cell will not be properly margined and therefore, will not read correctly. If the time is too long, on the other hand, the cell can be over erased or permanently damaged. Over erasure occurs when an excessive erase time has reduced the gate threshold below the applied control gate voltage for an unselected cell, resulting in excessive source-to-drain leakage. The only way to recover from this event is to use a special programming algorithm that raises the threshold of the NVM cell; the manufacturer may or may not implement this.

Programming Time

When NVM technology was first introduced, its use in microcontrollers was limited to prototyping – but only because of its relatively long programming time. While this time was still shorter than the erase interval for UV-EPROM parts (about 15 minutes), it was still too long for high volume production. Advances in technology have reduced programming times close to the same magnitude as earlier EPROM technologies.

ADVANTAGES OF MICROCHIP’S PEEC TECHNOLOGY

The ideal NVM cell design for the embedded control market has at least the following characteristics:

- Provides best in class reliability over the widest operating range
- Implements fast programming times
- Can be used to create arrays of various sizes (single bits to multiple kilobytes) in a cost effective manner

When Microchip began developing its NVM technology, it was interesting to find out that no one else was developing a NVM cell to address these needs. As a result, Microchip can now offer the 0.5µ P-channel Electrically Erasable Cell (PEEC) for both microcontrollers and serial EEPROMs. The Microchip PEEC cell offers these advantages:

- FN program and erase for ultra reliable operation
- Single transistor design for small die area arrays or bits
- Capable of true EEPROM operation (single byte erase and program)
- No change in tunnel oxide from previous processes
- Higher coupling ratio resulting in lower programming voltages and times
- Individual bits for configuration and calibration, removing the need for RAM-based latches
- Charge pump regulation controlled by dedicated on-chip circuitry
- High voltage application to NVM cells timed by on-chip circuitry
- Best in class endurance and reliability

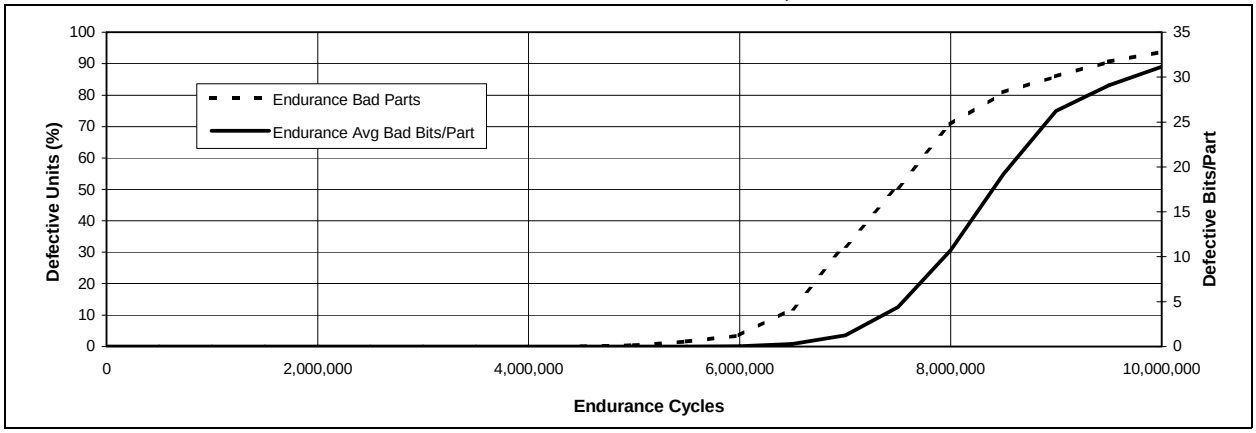
Referring to your own memory architecture as “best in class” may sound like bragging but the characterization data for the 0.5µ NVM cell backs up the claim time and time again. Microchip continuously monitors the performance of the FLASH memory by constantly sampling lots over the course of any given year, averaging about 100 lots per year. Key performance indicators that are monitored are Endurance, Accelerated Retention, and Failure-In-Time (FIT) rates.

Endurance

Endurance (the number of erase/write operations that the memory will complete before failing) encompasses both cell failures and disturb conditions. *Disturb* is a reliability issue, where adjacent cells in other rows and columns combinations of the array are exercised during multiple erase/write cycles. The high voltage applied to the non-selected rows and columns will slowly strip away charge from the non-selected cells, resulting in a bit that changes from a ‘0’ to a ‘1’. Disturb conditions are exhibited in some NVM cells, primarily those using CHE/FN and CHE/Emission technologies.

Figure 1 shows the results of endurance testing for one lot of Microchip’s 24XX256 serial EEPROMs using the 0.5µ PEEC cell. In this test, one row was exercised 10 million times at a temperature of 85°C. The first bit failure in this test was detected at approximately 5 million cycles. In a similar test at 25°C, the first bit failure does not occur until the 8 to 10 million cycle range. What this figure doesn’t show is that none of the bit failures occurred in non-selected rows which would indicate disturb related failures. These results are far superior to any NVM memory offered on an 8-bit microcontroller.

FIGURE 1: ENDURANCE RESULTS FOR MICROCHIP 0.5µ PEEC EEPROMS

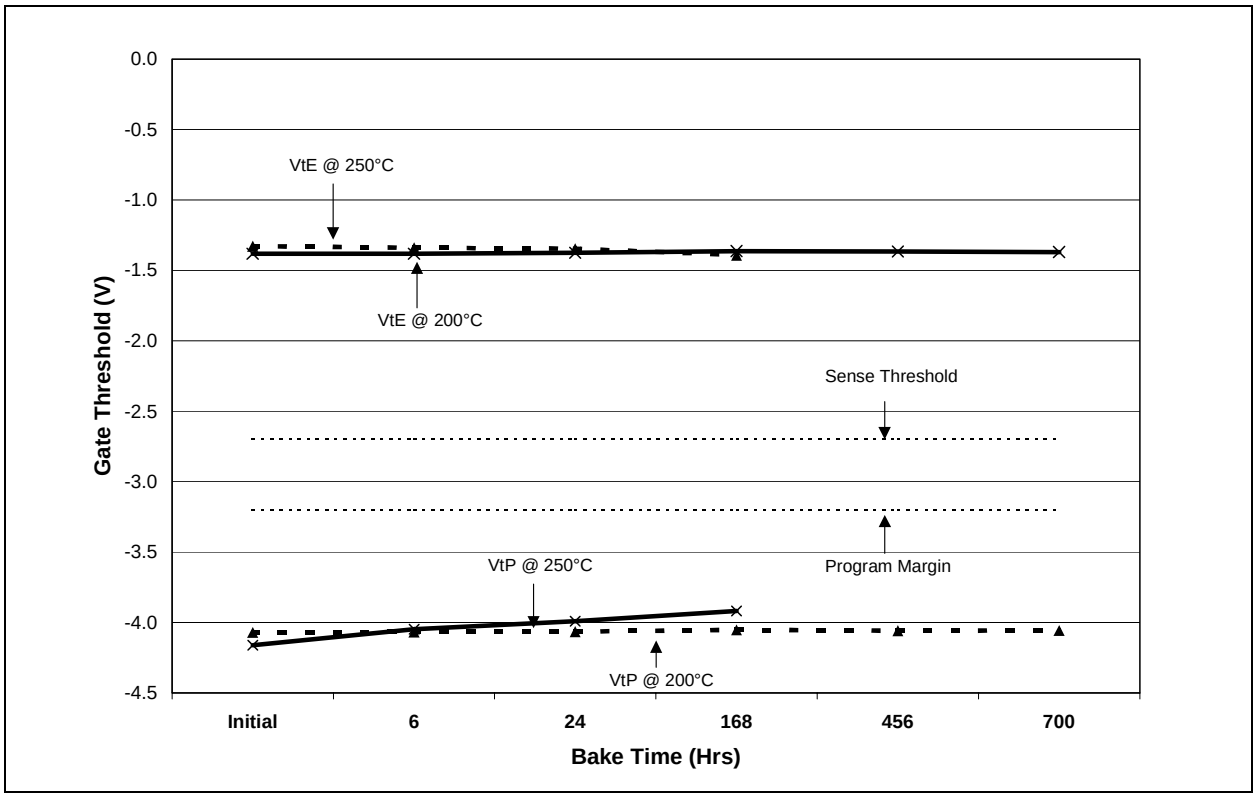


Retention

Retention refers to how long a bit retains its originally programmed value. Retention testing takes place at elevated temperatures of 200°C and 250°C on unbiased devices. At several points in time, the threshold voltage on the data bit transistor is measured.

The results are shown in Figure 2. The upper lines represent "VtE", the threshold voltages for cells in an erased state (no charge is present on the floating gate). The bottom lines represent "VtP", the threshold voltage for cells in a programmed state (charge present on the floating gate). The lines in the middle represent the sense amplifier trip point, where a voltage that drops below the line represents a state change for that particular bit, and the program margin. As the graph shows, very little charge loss occurs over the bake time. The lifetime calculations from the data for this test translate to well over 100 years of retention. Again, the results are far superior to any other 8-bit microcontroller manufacturer.

FIGURE 2: DATA RETENTION AS A FUNCTION OF WAFER LEVEL CHARGE LOSS OVER TIME



FIT Rates

The last of the testing performed by Microchip is the Dynamic Life Testing (DLT) and Data Retention Reliability. This testing takes place on random lots throughout the year. The data is shown as *Failures in Time*, or FITs. One FIT represents a single failure in 1 billion device hours of operation. To put this another way, 1000 FITs is equivalent to a failure rate of 0.1% per 1000 hours of operation.

Figure 3 shows typical data for a one year period for the 0.5µ NVM cell. A user could experience 8 fails per every 1 billion device hours of operation. These failures are due to random fab defects, and are not related to the core technology. The retention FIT rate is best in class with no failures at all. This data indicates that failures in the device usually occur outside of the program memory area before there is a retention failure. One thing to note is that retention testing is performed after a device has been exercised for the specified erase/write cycles. This represents the worst case scenario, and is used to create weak cells that are more susceptible to retention issues.

Microchip specifies endurance and retention over the entire operating temperature range of the device. Most specifications include a typical number at 25°C, a minimum number of cycles for the entire industrial temperature range (-40°C to +85°C), and a minimum specification for the extended temperature range (+85°C to +125°C). The specifications are also separated by memory usage (i.e., program memory and data EEPROM).

FIGURE 3: SUMMARY OF FIT TESTING FOR MEMORY (MARCH 2001 THROUGH APRIL 2002)

Dynamic Life Testing:

- 125°C @ 0.7 eV
- Temperature derated to 55°C
- 60% Confidence Level
- Total Device Hours: 16,000,000 (samples from 113 lots)
- FIT Rate: 8

Bake Retention after Endurance Testing:

- 150°C @ 1.2 eV
- Temperature derated to 55°C
- 60% Confidence Level
- Device Hours: 8,200,000 (samples from 117 lots)
- FIT Rate: 0

TABLE 2: ENDURANCE AND RETENTION FIGURES FOR MICROCHIP FLASH NVM

Temperature (°C)	Endurance (E/W Cycles)		Data Retention (Yrs)
	Program Memory	Data Memory	
25°C	100,000	1,000,000	100
-40°C to +85°C	10,000	100,000	40
+85°C to +125°C	1,000	10,000	40

The complete endurance/retention matrix is shown in Table 2. At 25°C, the PEEC cell can be expected to have 1 million erase/write cycles on data EEPROM and 100,000 erase/write cycles on program memory. At the same time, it can be expected to retain its contents for a minimum of 100 years. No other manufacturer of 8-bit microcontrollers can offer these specifications.

The outcome of endurance testing on the PEEC cell design used in Microchip's 8-bit microcontrollers is shown in Figure 4 (for data EEPROM) and Figure 5 (for program memory). In both graphs, note that the typical number of erase/write cycles before failure exceeds the published endurance specification. So even as significant as the published endurance specifications are, they are conservative in comparison to what actual testing suggests.

FIGURE 4: TYPICAL AND SPECIFIED ENDURANCE FOR 0.5µ PEEC DATA EEPROM

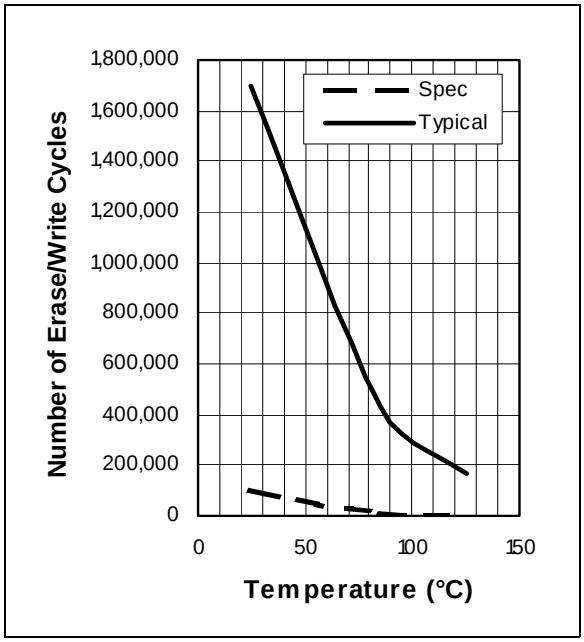
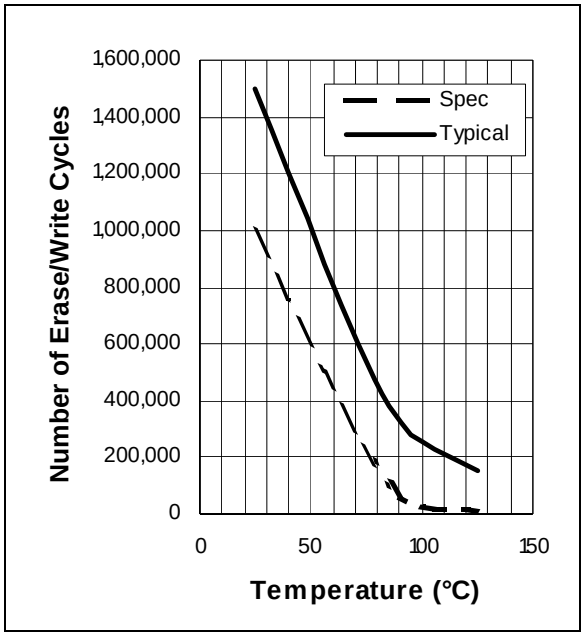


FIGURE 5: TYPICAL AND SPECIFIED ENDURANCE FOR 0.5µ PEEC PROGRAM MEMORY



ADVANTAGES FOR APPLICATIONS

Endurance

As we've already noted, most other manufacturers provide memory with an endurance of 100 to 10,000 cycles and retention of 15 to 25 years. Microchip's PEEC cells are capable of over 100 years of data retention with 1 million erase/write cycles for data EEPROM and 100,000 erase/write cycles for program memory. With these unprecedented numbers, the PEEC cell far surpasses most other manufacturers of 8-bit microcontrollers and in fact allows program memory to be used to store non-static data.

For single bit memories such as device configuration bits, the PEEC cell provides a noise insensitive and reliable method for storing configuration data. This helps to prevent noise from impacting device operation, and enhances reliability even more.

The endurance of the PEEC cell provides designers with a sense of security – and one less thing to worry about when using NVM in their application.

Temperature

While most manufacturers of 8-bit microcontrollers only specify endurance or retention at 25°C, the operation of the PEEC cell is specified over the entire operating temperature range of the microcontroller (-40°C to +125°C). The numbers provided do not reflect just optimal conditions but actual expected performance in all specified conditions.

Operating Voltage and Frequency

For Microchip devices, the V/F characterization graph in each device data sheet (see the example in Figure 6) shows where the device is fully functional; that means *all* parts of the microcontroller are functional to the specifications in the data sheet. Other manufacturers show extended ranges of voltage or frequency but limit the operation of certain features, such as self-writes to NVM. These exceptions are usually called out in footnotes.

The ability for Microchip PEEC cells to operate across the entire operating range is due to the design of the on-chip charge pump for high voltage generation. It not only self-regulates over the entire operating voltage range of the device (2.0V to 5.5V), but includes its own clock source to program and erase cells regardless of the clock frequency, supply voltage or temperature. This provides reliable programming without imposing any limitations on the application.

Self-Programmability

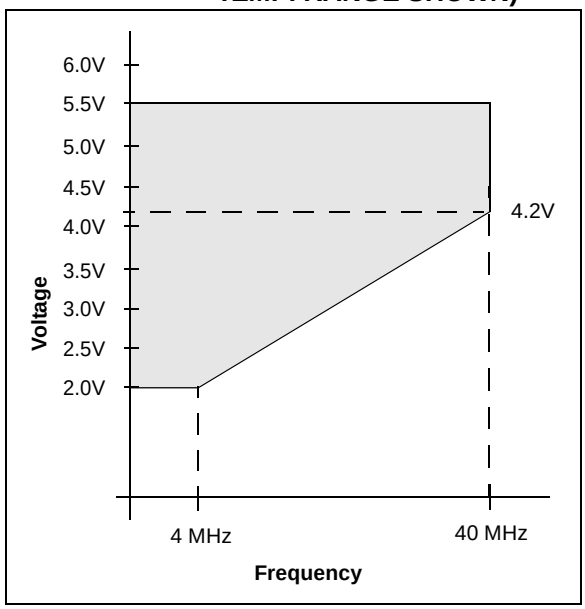
As we said earlier, an important feature of self-programming is providing the proper margin on the cell to read correctly over the specified operating range for the device. As noted above, Microchip devices embed the timing source into the charge pump circuitry itself. The user simply executes a sequence of instructions to activate the self-programming circuitry which develops the regulated high voltage and applies it precisely to ensure proper cell margins. An internal state machine controls the entire process.

Programming Time

The PEEC cell has a limitation of slower programming time when compared to other technologies. Microchip overcomes this limitation by carefully designing the structure of the array to provide a programming time of one second for all PEEC FLASH devices, from 512 bytes to 128 Kbytes. This is achieved by decreasing the single byte programming time to 1 ms and implementing parallel block programming.

Although programming still takes longer than the other technologies, the limitation in a high volume manufacturing environment is usually not the device to be programmed. Very often, it's the tester which also functions as a programmer. The best program/test cycle times for these systems are typically 5 to 7 seconds, which are well above the programming time for Microchip devices. This means that even with today's best current assembly line technology, programming a PICmicro® FLASH device will most likely not be the rate limiting step.

FIGURE 6: TYPICAL V/F GRAPH FOR A PICmicro DEVICE (PIC18LF4320, INDUSTRIAL TEMP. RANGE SHOWN)



CONCLUSION

It's possible that providing the best memory performance over the widest possible range of conditions is not important to your application. However, reliability is always an important factor. The 0.5µ PEEC cell from Microchip provides an alternative to other 8-bit microcontrollers that is reliable, extremely flexible and cost effective, and all without sacrificing performance.

REFERENCES

IEEE 1005-1998. *IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays*. New York: The Institute of Electrical and Electronics Engineers, Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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