TB033

Using the PIC16F877 To Develop Code For PIC16CXXX Devices

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INTRODUCTION

With the release of the FLASH-based PIC16F87X family, Microchip Technology has completed the circle on product technology. Microchip is now in the unique position of offering FLASH, OTP or ROM-based versions of devices with similar feature sets. Customers now have the most flexible position to select their choice of technology and easily migrate from one technology to another, reaping the benefits and cost structures which best suit their needs.

The PIC16F877 FLASH-based PICmicro® introduced by Microchip has the unique distinction of being a superset part with reprogrammable program memory for most PIC16CXXX products. The FLASH program memory, coupled with a built-in, In-Circuit Debugger (ICD), allows the development of a simple, low-cost emulator or ROMulator for most of the PIC16CXXX products.

A typical design scenario starts with the customer developing the initial prototype using a FLASH product. A limited production run using FLASH allows the customer to verify the operation of the production line without sacrificing product. Full production then starts with either FLASH or OTP, depending on how well the software has been validated. When the software has a proven track record of robustness, the customer can migrate to a lower cost ROM. This technical brief will highlight the design considerations associated with such a strategy.

The original goal of the PIC16F87X devices was to maintain compatibility with the existing PIC16C6X/7X devices, such that any code written for a PIC16C6X/7X device will run on a PIC16F87X without any modifications. It is so compatible that any HEX file generated for a PIC16C6X/7X device can be programmed into the PIC16F87X device, as long as the configuration bits are set correctly. Developing an application for an OTP or ROM device using the PIC16F87X requires some care and minor device differences must be taken into account.

The PIC16F87X devices have some features that are not available or modified from the PIC16CXXX devices. When developing code, use the data sheet for the target device and refer to the exceptions listed in the next section for each device. Following these suggestions should minimize the number of problems that arise. The features not found on the OTP/ROM PIC16CXXX microcontrollers are:

- FLASH Program Memory with read and write capabilities
- EEPROM Data Memory
- Master SSP (MSSP)

The peripherals on the PIC16F87X devices that are modified versions of the PIC16CXXX device, but code compatible, are:

- 10-bit A/D converter
- 9-bit Addressable USART

Certain resources are consumed when the MPLAB™-ICD In-Circuit Debugger is used to develop code. These resources are released when the debugger is not used. The resources include:

- Last 256 words of program memory: IF00h to IFFh
- Program memory location 0000h must be a `NOP` instruction
- Pins RB6 and RB7: CLK and Data for ICD
- $\overline{\text{MCLR}}$/V_{PP} used for programming @ 13V
- Data memory locations 70h, 1EBh – 1EFh
- 1 Level of stack

PART-TO-PART DIFFERENCES

When using the PIC16F87X device to develop code for an application that will eventually use a ROM or OTP device, the designer should not only keep in mind the discrepancies between the devices, but also the errata for both devices. A limitation on one or both devices may require the designer to use different workarounds to make the application work. All device errata can be found on the Microchip website (www.microchip.com).

The following paragraphs explain the differences or what's missing on the target device when compared to the PIC16F87X device. Some differences, such as program and data memory sizes, need to be monitored as development progresses to ensure that the limits are not exceeded for the target device. Obviously, none of the advanced features of the PIC16F87X should be used, such as Data EEPROM memory or Master Mode I^2C™. Appendix A shows tables comparing the OTP/ROM PIC16CXXX to the FLASH equivalent.

Data Memory

All of the PIC16CXXX devices, except the PIC16C66/67/76/77, have only two banks of data memory. The method of switching between the two banks is to clear the RP0 bit (STATUS<5>) to access registers in Bank 0 and set the bit to access registers in Bank 1. Any indirect addressing uses only the FSR special function register (SFR) to access any register in Bank 0 or Bank 1. However, the PIC16F87X devices and the PIC16C66/67/76/77 all have four banks of data memory. The RP1:RP0 bits (STATUS<5,6>) now select the bank for direct data memory addressing operations. When performing indirect data memory accesses on a device with four banks, the IRP bit (STATUS<7>) is used to indicate the upper or lower two banks. Since the FSR can access 256 registers or one register in either the two lower or upper banks, only one additional bit is required to indicate which set of registers to operate on. The following table shows the bank decoding of RP1 and RP0

TABLE 1: BANK CONTROL

		RPO	
		0	1
RP1	0	Bank 0	Bank 1
	1	Bank 2	Bank 3

When writing code on the PIC16F87X devices for a target PIC16CXXX device, simply maintain the IRP and RP1 bits as '0's. This requirement follows the recommendations in the target data sheet to maintain these bits clear for devices that have only two banks of data memory.

SSP Module

The next difference is the SSP Module that contains the SPI™ and I^2C peripherals. There are several variations of the SSP Module. Microchip currently has three versions of the SSP Module:

- BSSP
  - 2-mode SPI
  - Slave I^2C with Start & Stop bit detection
- SSP
  - 4-mode SPI with Microwire®
  - Slave I^2C with Start & Stop bit detection
- MSSP
  - 4-mode SPI with Microwire
  - Slave I^2C
  - Master Mode I^2C

Of all the differences between the three modules, the revision of the 2-mode SPI module to 4-modes is the biggest backward compatibility issue. These changes include redefining the functionality of the CKP (SSPCON<4>), adding the CKE bit (SSPSTAT<6>) and adding the SMP bit (SSPSTAT<7>). In the BSSP module, the CKP bit controlled both the idle state of the clock and the clock edge that data is transmitted on as shown below:

- Idle state for clock is high, transmit happens on falling edge, receive on rising edge
- Idle state for clock is low, transmit happens on rising edge, receive on falling edge

In the new 4-mode SPI module, the CKP bit controls the idle state of the clock, the CKE bit controls the edge that data is transmitted and the SMP bit controls where the incoming data is sampled (middle or end of bit time). The SMP bit sets the SPI module for regular SPI operation or Microwire operation. The table below shows this graphically.

TABLE 2: SPI CONFIGURATION

		CKE	
		0	1
CKP	0	low, falling	low, rising
	1	high, rising	high, falling

To properly configure the PIC16F87X devices to be compatible with the non-FLASH devices, you must set the bits to the following states:

- For BSSP operation when CKP = '0', set CKP = '0', CKE = '1', SMP = '0'
- For BSSP operation when CKP = '1', set CKP = '1', CKE = '1', SMP = '0'

Even though the PIC16F87X devices add Master Mode I^2C to the SSP module, problems will not be encountered as long as code is written using the target device data sheet. This part of the SSP module was designed to be 100% compatible with the existing BSSP and SSP modules.

A/D Module

Although the 10-bit A/D converter is 100% compatible to the 8-bit A/D, it does have a 10-bit result. These 10 bits are spread across the two registers, ADRESH and ADRESL, either left or right justified. Any code written for the PIC16F87X 10-bit A/D converter will be compatible as long as the result is left justified (default state) and the code uses ADRESH as the 8-bit result. The ADRESH register is in the same place in the Data Memory map as the ADRES register of the 8-bit A/D. When changing over to the target OTP or ROM device, you simply need to change ADRESH to ADRES.

USART

The addressable USART also has only one additional bit, ADDEN (RCSTA<3>). The default state of this bit is 0, which turns off 9-bit addressing and therefore remains 100% compatible to the non-addressable USART. Here again, problems should not be encountered as long as the target data sheet is used to write code.

Brown-out Reset

On a device that has Brown-out Reset, only the BOR bit (PCON<0>) was added. In most cases, this bit is not used and can be ignored. The main consideration when writing code on the PIC16F87X device for a device that does not have Brown-out Reset is to make sure that this function is disabled in the configuration bits.

Extra SFRs

The PIC16F87X devices will have some SFRs that are not present in other devices. The code should refrain from using these locations, otherwise unexpected results may occur. As long as the code is written using the target device data sheet, problems should not be encountered.

CONCLUSION

The MPLAB-ICD In-Circuit Debugger makes an ideal low-cost development tool for not only the PIC16F87X devices but also for the PIC16C6X/7X devices as well. Using the guidelines presented in this technical brief, a designer should be able to design/debug an application using the FLASH devices and then switch to the lower cost ROM or OTP equivalents for production.

Comparison tables by device family follow for review of feature differences.

APPENDIX A: DEVICE COMPARISON TABLES

PIC16C62A/62B/CR62: 2KW, 28-pin, Without Analog					FLASH Equivalent
Device		**PIC16C62A**	**PIC16C62B**	**PIC16CR62**	**PIC16F873**
Program Memory		2KW	2KW	2KW	4KW
Data Memory	**Bytes**	128	128	128	192
	Banks	0,1	0,1	0,1	0,1,2,3
	Shared	—	—	—	16 bytes (F0h-FFh)
Data EEPROM		128	128	128	128
Additional Features		—	—	—	10-bit A/D Addressable RT CCP2
Additional SFRs		—	—	—	PIR2, PIE2, CCPR2L, CCPR2H, CCP2CON, RXSTA, TXSTA, SPBRG, ADCON0, ADCON1, ADRESH, ADRESL, SSPCON2, TXREG, RCREG
Bit Differences	**IRP**	Reserved	Reserved	Reserved	Selects upper/lower bank
	RP1	Reserved	Reserved	Reserved	Selects upper/lower bank
	SMP	—	Yes	—	Microwire/slew rate control
	CKE	—	Yes	—	Clock edge/levels select
	CKP	Yes	Yes	Yes	Clock idle/stretching control

PIC16C63A/CR63: 4KW, 28-pin, Without Analog				FLASH Equivalent
Device		**PIC16C63A**	**PIC16CR63**	**PIC16F873**
Program Memory		4KW	4KW	4KW
Data Memory	**Bytes**	192	192	192
	Banks	0,1	0,1	0,1,2,3
	Shared	—	—	16 bytes (F0h-FFh)
Data EEPROM		—	—	128
Additional Features		Brown-out Reset	Brown-out Reset	10-bit A/D Brown-out Reset
Additional SFRs		—	—	ADCON0, ADCON1, ADRESH, ADRESL, SSPCON2
Bit Differences	**IRP**	Reserved	Reserved	Selects upper/lower bank
	RP1	Reserved	Reserved	Selects upper/lower bank
	SMP	Yes	—	Microwire/slew rate control
	CKE	Yes	—	Clock edge/levels select
	CKP	Yes	Yes	Clock idle/stretching control
	BOR	Yes	Yes	Brown-out Reset status
	ADDEN	—	—	Selects 9-bit addressing

PIC16C64A/CR64: 2KW, 40-pin, Without Analog				FLASH Equivalent
Device		**PIC16C64A**	**PIC16CR64**	**PIC16F874**
Program Memory		2KW	2KW	4KW
Data Memory	**Bytes**	128	128	192
	Banks	0,1	0,1	0,1,2,3
	Shared	—	—	16 bytes (F0h-FFh)
Data EEPROM		—	128	128
Additional Features		Brown-out Reset	—	10-bit A/D Addressable USART CCP2 Brown-out Reset
Additional SFRs		—	—	PIR2, PIE2, CCPR2L, CCPR2H, CCP2CON, RXSTA, TXSTA, SPBRG, ADCON0, ADCON1, ADRESH, ADRESL, SSPCON2, TXREG, RCREG
Bit Differences	**IRP**	Reserved	Reserved	Selects upper/lower bank
	RP1	Reserved	Reserved	Selects upper/lower bank
	SMP	—	—	Microwire/slew rate control
	CKE	—	—	Clock edge/levels select
	CKP	Yes	Yes	Clock idle/stretching control
	BOR	Yes	Yes	Brown-out Reset status

PIC16C65A/65B/CR65: 4KW, 40-pin, Without Analog					FLASH Equivalent
Device		**PIC16C65A**	**PIC16C65B**	**PIC16CR65**	**PIC16F874**
Program Memory		4KW	4KW	4KW	4KW
Data Memory	**Bytes**	192	192	192	192
	Banks	0,1	0,1	0,1	0,1,2,3
	Shared	—	—	—	16 bytes (F0h-FFh)
Data EEPROM		—	—	128	128
Additional Features		Brown-out Reset	Brown-out Reset	Brown-out Reset	Brown-out Reset
Additional SFRs		—	—	—	ADCON0, ADCON1, ADRESH, ADRESL, SSPCON2
Bit Differences	**IRP**	Reserved	Reserved	Reserved	Selects upper/lower bank
	RP1	Reserved	Reserved	Reserved	Selects upper/lower bank
	SMP	Yes	Yes	—	Microwire/slew rate
	CKE	Yes	Yes	—	Clock edge/levels select
	CKP	Yes	Yes	Yes	Clock idle/stretching
	BOR	Yes	Yes	Yes	Brown-out Reset status
	ADDEN	—	—	—	Selects 9-bit addressing

PIC16C66/67: 8KW, 28/40-pin, Without Analog				FLASH Equivalent
Device		**PIC16C66**	**PIC16C67**	**PIC16F876/877**
Program Memory		8KW	8KW	8KW
Data Memory	**Bytes**	368	368	368
	Banks	0,1,2,3	0,1,2,3	0,1,2,3
	Shared	16 bytes (F0h-FFh)	16 bytes (F0h-FFh)	16 bytes (F0h-FFh)
Data EEPROM		—	—	128
Additional Features		—	—	10-bit A/D
Additional SFRs		—	—	ADCON0, ADCON1, ADRESH, ADRESL, SSPCON2
Bit Differences	**ADDEN**	ADDEN	—	Selects 9-bit addressing

PIC16C72/72A/CR72: 2KW, 28-pin, With Analog					FLASH Equivalent
Device		**PIC16C72**	**PIC16C72A**	**PIC16CR72**	**PIC16F873**
Program Memory		2KW	2KW	2KW	4KW
Data Memory	**Bytes**	128	128	128	192
	Banks	0,1	0,1	0,1	0,1,2,3
	Shared	—	—	—	16 bytes (F0h-FFh)
Data EEPROM		—	—	—	128
Additional Features		—	—	—	Addressable USART CCP2
Additional SFRs		—	—	—	PIR2, PIE2, CCPR2L, CCPR2H, CCP2CON, RXSTA, TXSTA, SPBRG, SSPCON2, TXREG, RCREG, ADRESL
Bit Differences	**IRP**	Reserved	Reserved	Reserved	Selects upper/lower bank
	RP1	Reserved	Reserved	Reserved	Selects upper/lower bank
	SMP	—	Yes	Yes	Microwire/slew rate control
	CKE	—	Yes	Yes	Clock edge/levels select
	CKP	Yes	Yes	Yes	Clock idle/stretching control
Register Names	**ADRESH**	ADRESH	ADRES	ADRES	ADRESH in F873 same as ADRES

PIC16C73A/73B: 4KW, 28-pin, With Analog				FLASH Equivalent
Device		**PIC16C73A**	**PIC16C73B**	**PIC16F873**
Program Memory		4KW	4KW	4KW
Data Memory	**Bytes**	192	192	192
	Banks	0,1	0,1	0,1,2,3
	Shared	—	—	16 bytes (F0h-FFh)
Data EEPROM		—	—	128
Additional Features		Brown-out Reset	Brown-out Reset	Brown-out Reset
Additional SFRs		—	—	ADRESL,SSPCON2
Bit Differences	**IRP**	Reserved	Reserved	Selects upper/lower bank
	RP1	Reserved	Reserved	Selects upper/lower bank
	SMP	Yes	Yes	Microwire/slew rate control
	CKE	Yes	Yes	Clock edge/levels select
	CKP	Yes	Yes	Clock idle/stretching control
	BOR	Yes	Yes	Brown-out Reset status
	ADDEN	—	—	Selects 9-bit addressing
Register Names	**ADRESH**	ADRES	ADRES	ADRESH in F873 same as ADRES

PIC16C74A/74B: 4KW, 40-pin, With Analog				FLASH Equivalent
Device		**PIC16C74A**	**PIC16C74B**	**PIC16F874**
Program Memory		4KW	4KW	4KW
Data Memory	**Bytes**	192	192	192
	Banks	0,1	0,1	0,1,2,3
	Shared	—	—	16 bytes (F0h-FFh)
Data EEPROM		—	—	128
Additional Features		Brown-out Reset	Brown-out Reset	Brown-out Reset
Additional SFRs		—	—	ADRESL,SSPCON2
Bit Differences	**IRP**	Reserved	Reserved	Selects upper/lower bank
	RP1	Reserved	Reserved	Selects upper/lower bank
	SMP	Yes	Yes	Microwire/slew rate control
	CKE	Yes	Yes	Clock edge/levels select
	CKP	Yes	Yes	Clock idle/stretching control
	BOR	Yes	Yes	Brown-out Reset status
	ADDEN	—	—	Selects 9-bit addressing
Register Names	**ADRESH**	ADRES	ADRES	ADRESH in F874 same as ADRES

PIC16C76/77: 8KW, 28/40-pin, Without Analog				FLASH Equivalent
Device		**PIC16C76**	**PIC16C77**	**PIC16F876/877**
Program Memory		8KW	8KW	8KW
Data Memory	**Bytes**	368	368	368
	Banks	0,1,2,3	0,1,2,3	0,1,2,3
	Shared	16 bytes (F0h-FFh)	16 bytes (F0h-FFh)	16 bytes (F0h-FFh)
Data EEPROM		—	—	128
Additional Features		—	—	10-bit A/D
Additional SFRs		—	—	ADRESL, SSPCON2
Bit Differences	**ADDEN**	—	—	Selects 9-bit addressing
Register Names	**ADRESH**	ADRES	ADRES	ADRESH in F876/77 same as ADRES

NOTES:

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