TB020

PIC12C67X Emulation Using PIC16C72 PICMASTER™ Emulator Probe

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This technical brief describes how to use the PIC16C72 PICMASTER™ emulator probe for PIC12C67X emulation.

Overview

Many simple PIC12C67X applications can be developed using the MPLAB™ simulator (Version 3.31 or higher), for complex applications real-time emulation may be required. Since the PIC16C72 shares the same upward expanded memory map and similar pin functions as the PIC12C67X, the PICMASTER® emulator probe 16J (AC165009) can be used to emulate most PIC12C67X functions. The PIC16C710, PIC16C711 or PIC16C715 emulator probes are not recommended for PIC12C67X emulation due to only 5 bits in the PORTA (address 05 hex) register map versus the 6 bits for the PIC12C67X.

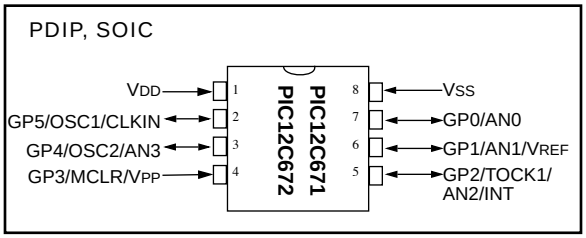
A custom bond-out chip is being designed specifically for emulation of the PIC12C67X (scheduled for completion in Q3 1998) and this will eliminate the need for this technical brief.

Hardware Emulation Recommendations

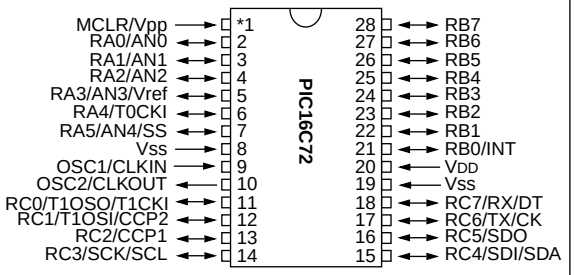
Your target PCB will accept the 8 pin PDIP or SOIC pin out of the PIC12C67X. An adapter socket must be constructed to interface from your 8 pin target to the 28 pin DIP socket on the emulator probe (see pin outs in Figure #1).

FIGURE 1:

PDIP, SOIC



SDIP, SOIC, Windowed Side Brazed Ceramic



Building the adapter socket

Many PIC12C67X functions are multiplexed into a single pin. For example, the GP2/T0CK1/AN2/INT pin, can be configured as a digital I/O, Timer 0 counter input, A/D input, or external interrupt pin. This highly multiplexed PIC12C67X pin does not exactly match a corresponding PIC16C72 pin, however most applications will use this pin in only one of it's four configurations. Therefore, a single PIC12C67X pin function can be mapped into the corresponding pin on PORTA or PORTB of the PIC16C72.

If any A/D channels are enabled then it is necessary to map all PIC12C67X GPIO (Digital I/O's) to PORTB of the PIC16C72. Using PORTB will enable emulation of the external interrupt, programmable pull-up resistors, and will simplify changes to the ADCON1 register.

Your adapter socket pin out must be customized for your specific application. The following tables show the pin out for six common applications.

TABLE 1 6 DIGITAL I/O'S

PIC12C67X Pin Function		Equivalent PIC16C72 Function	
Name	**#**	**Name**	**#**
VDD	1	VDD	20
GP5/OSC1/CLKIN	2	RA5/AN4	7
GP4/OSC2/AN3/CLKOUT	3	RA4/TOCK1	6
GP3/MCLR/Vpp	4	RA3/AN3/Vref	5
GP2/TOCK1/AN2/INT	5	RA2/AN2	4
GP1/AN1/Vref	6	RA1/AN1	3
GP0/AN0	7	RA0/AN0	2
VSS	8	VSS	8,19

Note 1: If you plan to use the GPIO pull-up resistors then map to PORTB.

TABLE 2 4 ANALOG AND 2 DIGITAL I/O'S

PIC12C67X Pin Function		Equivalent PIC16C72 Function	
Name	**#**	**Name**	**#**
VDD	1	VDD	20
GP5/OSC1/CLKIN	2	RB5	26
GP4/OSC2/AN3/CLKOUT	3	RA3/AN3/Vref	5
GP3/MCLR/Vpp	4	RB3	24
GP2/TOCK1/AN2/INT	5	RA2/AN2	4
GP1/AN1/Vref	6	RA1/AN1	3
GP0/AN0	7	RA0/AN0	2
VSS	8	VSS	8,19

TABLE 3 3 ANALOG AND 3 DIGITAL I/O'S

PIC12C67X Pin Function		Equivalent PIC16C72 Function	
Name	**#**	**Name**	**#**
VDD	1	VDD	20
GP5/OSC1/CLKIN	2	RB5	26
GP4/OSC2/AN3/CLKOUT	3	RB4	25
GP3/MCLR/Vpp	4	RB3	24
GP2/TOCK1/AN2/INT	5	RA3/AN3/Vref	5
GP1/AN1/Vref	6	RA1/AN1	3
GP0/AN0	7	RA0/AN0	2
VSS	8	VSS	8,19

TABLE 4 2 ANALOG AND 4 DIGITAL I/O'S

PIC12C67X Pin Function		Equivalent PIC16C72 Function	
Name	**#**	**Name**	**#**
VDD	1	VDD	20
GP5/OSC1/CLKIN	2	RB5	26
GP4/OSC2/AN3/CLKOUT	3	RB4	25
GP3/MCLR/Vpp	4	RB3	24
GP2/TOCK1/AN2/INT	5	RB2	23
GP1/AN1/Vref	6	RA1/AN1	3
GP0/AN0	7	RA0/AN0	2
VSS	8	VSS	8,19

TABLE 5 1 ANALOG AND 5 DIGITAL I/O'S

PIC12C67X Pin Function		Equivalent PIC16C72 Function	
Name	**#**	**Name**	**#**
VDD	1	VDD	20
GP5/OSC1/CLKIN	2	RB5	26
GP4/OSC2/AN3/CLKOUT	3	RB4	25
GP3/MCLR/Vpp	4	RB3	24
GP2/TOCK1/AN2/INT	5	RB2	23
GP1/AN1/Vref	6	RB1	22
GP0/AN0	7	RA0/AN0	2
VSS	8	VSS	8,19

Note 1: If you plan to use the GPIO pull-up resistors then map to PORTB.

TABLE 6 2 ANALOG, 3 DIGITAL I/O'S AND 1 EDGE TRIGGERED INTERRUPT

PIC12C67X Pin Function		Equivalent PIC16C72 Function	
Name	**#**	**Name**	**#**
VDD	1	VDD	20
GP5/OSC1/CLKIN	2	RB5	26
GP4/OSC2/AN3/CLKOUT	3	RB4	25
GP3/MCLR/Vpp	4	RB3	24
GP2/TOCK1/AN2/INT	5	RB0/INT	21
GP1/AN1/Vref	6	RA1/AN1	3
GP0/AN0	7	RA0/AN0	2
VSS	8	VSS	8,19

Hardware differences and work-arounds

The PIC12C67X has more flexibility in selecting A/D versus digital I/O pins (see table 2, ADCON1 register). To work around this difference, enable more A/D channels on PORTA of the PIC16C72 and map all digital I/O's to PORTB of the PIC16C72 (and ignore the extra 16C72 A/D channels).

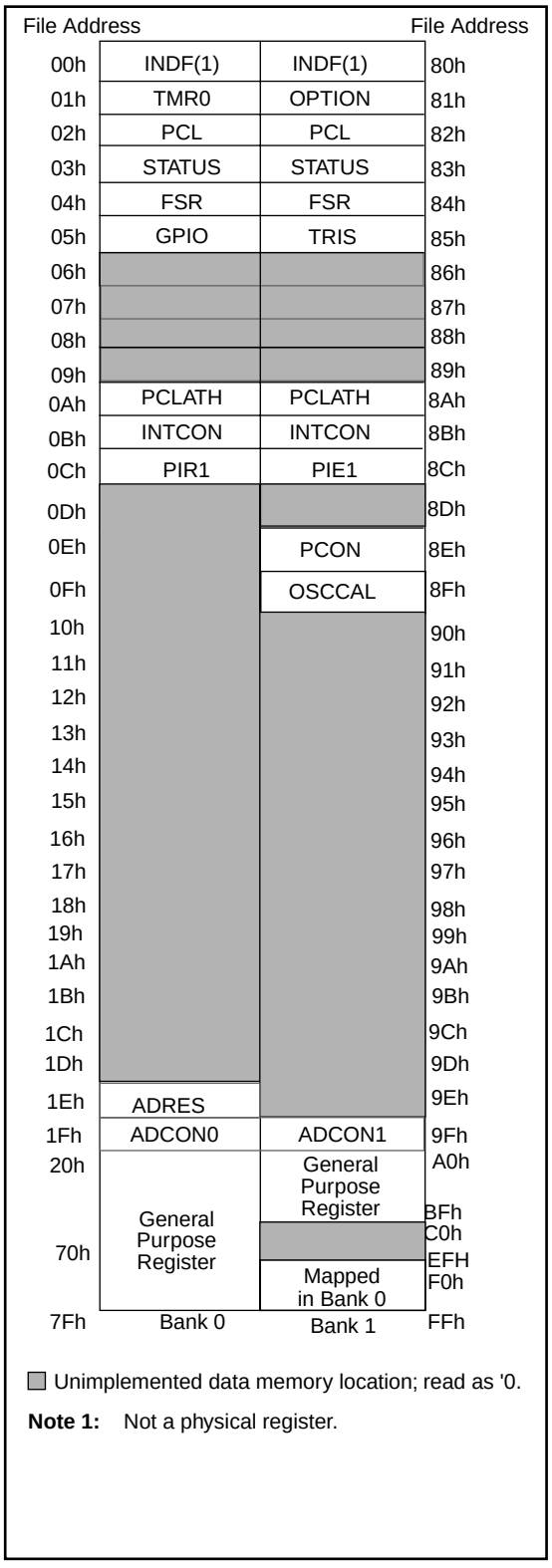
The PIC12C67X also has an on chip oscillator with the ability to output it's clock (to CLKOUT pin). The internal oscillator option can be emulated with the PIC16C72 by using a 4Mhz 'canned' clock oscillator, with the probe jumper set to "INT CLK".

The RA4/T0CK1 pin of the PIC16C72 when configured as an output is open drain, and therefore will need a pull-up resistor to emulate the GP4 PIC12C67X pin output.

Software Emulation Recommendations

The PIC12C67X and PIC16C72 both have 2K words of program memory and 128 bytes of RAM. As is indicated by the following register file map, the PIC12C67X is a sub-set of the PIC16C72. The 'extra' registers of the PIC16C72 can be ignored while emulating.

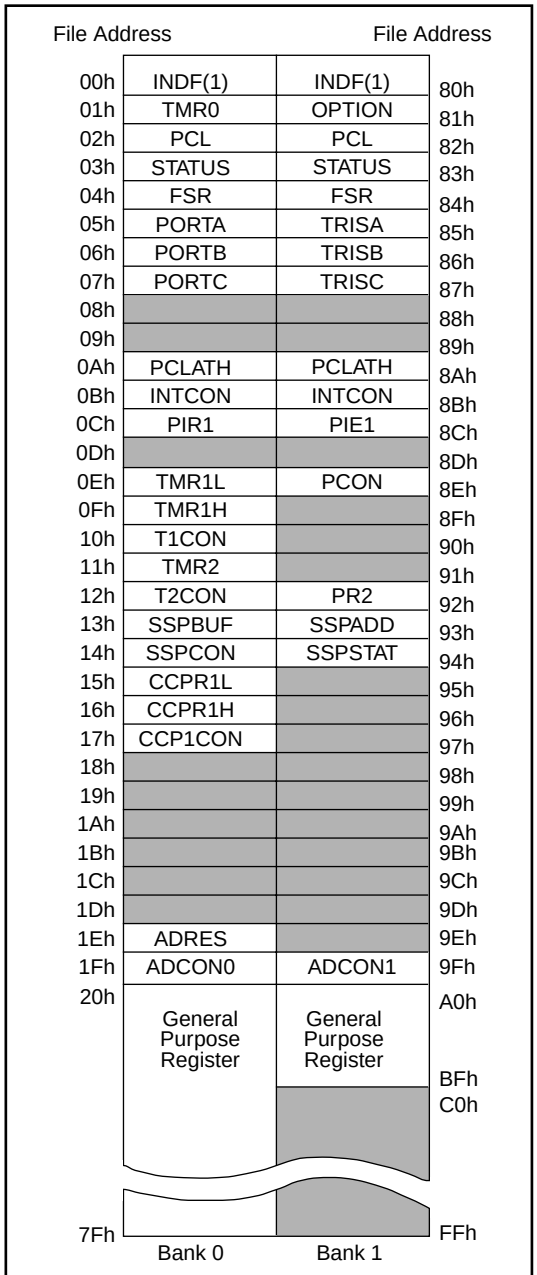
FIGURE 2: PIC12C67X REGISTER FILE MAP



Unimplemented data memory location; read as '0.

Note 1: Not a physical register.

FIGURE 3: PIC16C72 REGISTER FILE MAP



Unimplemented data memory location; read as '0.

Note 1: Not a physical register.

SPECIAL FUNCTION REGISTER SUMMARY (BANK 0)

PIC12C67X

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0									
00h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)							
01h	TMR0	Timer0 module's register							
02h(1)	PCL	Program Counter's (PC) Least Significant Byte							
03h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04h(1)	FSR	Indirect data memory address pointer							
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0
06h	—	Unimplemented							
07h	—	Unimplemented							
08h	—	Unimplemented							
09h	—	Unimplemented							
0Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter				
0Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	**GPIE**	T0IF	INTF	**GBIF**
0Ch	PIR1	—	ADIF	—	—	—	—	—	—
0Dh	—	Unimplemented							
0Eh	—	Unimplemented							
0Fh	—	Unimplemented							
10h	—	Unimplemented							
11h	—	Unimplemented							
12h	—	Unimplemented							
13h	—	Unimplemented							
14h	—	Unimplemented							
15h	—	Unimplemented							
16h	—	Unimplemented							
17h	—	Unimplemented							
18h	—	Unimplemented							
19h	—	Unimplemented							
1Ah	—	Unimplemented							
1Bh	—	Unimplemented							
1Ch	—	Unimplemented							
1Dh	—	Unimplemented							
1Eh	ADRES	A/D Result Register							
1Fh	ADCON0	ADCS1	ADCS0	r	CHS1	CHS0	GO/$\overline{DONE}$	r	ADON

(1) The PIC12C67X bit names are different than the corresponding PIC16C72 names, but the functions are the same.

PIC16C72

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)							
TMR0	Timer0 module's register							
PCL	Program Counter's (PC) Least Significant Byte							
STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
FSR	Indirect data memory address pointer							
PORTA	—	—	PORTA Data Latch when written: PORTA pins when read					
PORTB	PORTB Data Latch when written: PORTB pins when read							
PORTC	PORTC Data Latch when written: PORTC pins when read							
—	Unimplemented							
—	Unimplemented							
PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter				
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF
—	Unimplemented							
TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register							
TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register							
T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON
TMR2	Timer2 module's register							
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register							
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
CCPR1L	Capture/Compare/PWM Register (LSB)							
CCPR1H	Capture/Compare/PWM Register (MSB)							
CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
ADRES	A/D Result Register							
ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON

SPECIAL FUNCTION REGISTER SUMMARY (BANK 1)

PIC12C67X

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Bank 1							
80h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)							
81h	OPTION	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
82h(1)	PCL	Program Counter's (PC) Least Significant Byte							
83h(1)	STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
84h(1)	FSR	Indirect data memory address pointer							
85h	TRIS	—	—	GPIO Data Direction Register					
86h	—	Unimplemented							
87h	—	Unimplemented							
88h	—	Unimplemented							
89h	—	Unimplemented							
8Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the PC				
8Bh(1)	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF
8Ch	PIE1	—	ADIE	—	—	—	—	—	—
8Dh	—	Unimplemented							
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	—
8Fh	OSCCAL	CAL3	CAL2	CAL1	CAL0	CALFST	CALSLW	—	—
90h	—	Unimplemented							
91h	—	Unimplemented							
92h	—	Unimplemented							
93h	—	Unimplemented							
94h	—	Unimplemented							
95h	—	Unimplemented							
96h	—	Unimplemented							
97h	—	Unimplemented							
98h	—	Unimplemented							
99h	—	Unimplemented							
9Ah	—	Unimplemented							
9Bh	—	Unimplemented							
9Ch	—	Unimplemented							
9Dh	—	Unimplemented							
9Eh	—	Unimplemented							
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0

(1) The PIC12C67X bit names are different than the corresponding PIC16C72 names, but the functions are the same.

(2) The OSCCAL register is unimplemented in the PIC16C72.

PIC16C72

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)							
OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
PCL	Program Counter's (PC) Least Significant Byte							
STATUS	IRP(4)	RP1(4)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
FSR	Indirect data memory address pointer							
TRISA	—	—	PORTA Data Direction Register					
TRISB	PORTB Data Direction Register							
TRISC	PORTC Data Direction Register							
—	Unimplemented							
—	Unimplemented							
PCLATH	—	—	—	Write Buffer for the upper 5 bits of the PC				
INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE
—	Unimplemented							
PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
PR2	Timer2 Period Register							
SSPADD	Synchronous Serial Port (I^2C mode) Address Register							
SSPSTAT	—	—	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
—	Unimplemented							
ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0

Your application software can be written with the MPASM conditional assembly feature. When emulating, assemble for the PIC16C72, when programming, re-assemble for the PIC12C67X. The attached source code (AtoD.asm) has been written to show a conditional assembly example and re-mapping of the registers.

Software Emulation Differences and work arounds:

Both devices have an ADCON1 register with 3 bits of control (PCFG0, 1, &2), however the PIC12C67X has much finer control over it's individual A/D pins. Therefore, if only one PIC12C67X A/D channel is needed (ADCON1 = xxxx x110), the PIC16C72 emulator will be configured as three A/D channels enabled (ADCON1= xxxx x100). Only one channel will be connected from the emulator to the PIC12C67X and the other two channels will be ignored.

The ADCON1 register differences are:

Table 2a:

PIC16C72 PCFG2:PCFG0 A/D Control bits

PCFG2 : PCFG0	RA5	RA3	RA2	RA1	RA0	Vref
000	A	A	A	A	A	VDD
001	A	Vref	A	A	A	RA3
010	A	A	A	A	A	VDD
011	A	Vref	A	A	A	RA3
100	D	A	D	A	A	VDD
101	D	Vref	D	A	A	RA3
110	D	D	D	D	D	-----
111	D	D	D	D	D	-----

Table 2b:

PIC12C67X PCFG2:PCFG0 A/D Control bits

PCFG2 : PCFG0	GP4	GP2	GP1	GP0	Vref
000	A	A	A	A	VDD
001	A	A	Vref	A	GP1
010	D	A	A	A	VDD
011	D	A	Vref	A	GP1
100	D	D	A	A	VDD
101	D	D	Vref	A	GP1
110	D	D	D	A	VDD
111	D	D	D	D	-----

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