INTRODUCTION

The early revision of Microchip’s 25xx080 and 25xx160 devices (revision A and B) require a software work around for proper write operation in mode 1,1. Mode 0,0 does NOT require a work around. This issue does not exist in 25xx080 and 25xx160 revision C silicon. The revision number can be found on the outside of a packaged part. It is the middle letter of the three letter string following the package type.

Mode 0,0 and 1,1 indicate that an SPI slave device latches serial data in on the rising edge of clock and out after the falling edge of clock. Mode 0,1 and 1,0 SPI devices would latch data in on the falling edge of clock and out after the rising edge of clock.

Reading a 25xx080 or 25xx160 devices do not require any software adjustments whether it is read in mode 0,0 or 1,1. However, for revision A or B silicon to properly initiate a write, the clock line must be low, when raising chip select (CS) for the write cycle to begin. In mode 0,0 the polarity of the clock is defined as low, and the clock idles low when not shifting data in or out. In mode 1,1, the polarity of the clock is defined as high, and the clock idles high when not shifting data in or out.

*Figure 1* depicts a write timing diagram. It can be seen that for mode 0,0 operation, the clock line is low when CS is brought high to start the write cycle timer. The write will be completed successfully in this case.

The dashed lines in *Figure 1* also depict the state of the clock in mode 1,1. The drawing shows that the clock line will be high when CS is raised. This will not start the write cycle timer, and the part will not write successfully.

*Figure 2* shows the timing necessary for proper implementation of mode 1,1 writes. The following steps should be taken to write properly in mode 1,1:

1. Load and send the write instruction.
2. Load and send the address.
3. Load and send the data.
4. **Lower the clock line.**
5. Raise chip select to start a write.
6. **Raise the clock line.**

The **bold** indicates the extra steps necessary to properly implement mode 1,1 operation on revision A or B silicon. The write cycle timer will begin when the chip select line is raised.

**FIGURE 1: NORMAL WRITE OPERATION**
FIGURE 2: MODIFIED WRITE OPERATION

SCK must be low when CS is raised for the write cycle to begin.

CS

SCK

Mode 0.0

Mode 1.1

SI

SO

high impedance

instruction

address bytes

data byte

SCK Low