Section 45. High-Speed Analog Comparator

HIGHLIGHTS

This section of the manual contains the following major topics:

Note:	This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices. Please consult the note at the beginning of the **"High-Speed Analog Comparator"** chapter in the current device data sheet to check whether this document supports the device you are using. Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

45.1 INTRODUCTION

The High-Speed Analog Comparator module in Switch Mode Power Supply (SMPS) and Digital Power Conversion devices provides a way to monitor voltage and current in a power conversion application. The analog comparator provides the user with the ability to implement Current Mode Control (CMC) in power conversion applications.

The High-Speed Analog Comparator module contains up to four high-speed analog comparators with dedicated 10-bit Digital-to-Analog Converters (DACs), which provide a programmable reference voltage to one input of the comparator.

The High-Speed Analog Comparator module consists of the following key features:

- Up to four analog comparators
- Dedicated 10-bit DAC for each analog comparator
- Programmable output polarity
- Interrupt generation capability
- Up to 16 selectable input sources
- Control for comparator hysteresis
- Comparator pulse stretcher
- Digital filter for comparator output
- DAC output to device pin
- Multiple voltage references for the DAC:
  - $AV_{DD}/2$
  - Internal Reference 1.2V ±1%
  - External Reference < (AV_{DD} - 1.6V)
- Interrupt generation capability
- Functional support for High-Speed Pulse-Width Modulation (PWM) module, which includes:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

45.2 MODULE DESCRIPTION

Depending on the device variant, SMPS dsPIC® devices feature either a standard or enhanced High-Speed Analog Comparator module, as illustrated in Figure 45-1 and Figure 45-2, respectively. Refer to the **"High-Speed Analog Comparator"** chapter in the specific device data sheet, to determine which Comparator module applies to your device.

The High-Speed Analog Comparator module provides high-speed operation with a typical delay of 20 ns with a typical offset voltage of ±5 mV. The negative input of the comparator is always connected to the DAC circuit. The positive input of the comparator is connected to an analog multiplexer that selects the desired source pin.

The analog comparator input pins are typically shared with pins used by the Analog-to-Digital Converter (ADC) module. Both the comparator and the ADC can use the same pins at the same time. This capability enables a user to measure an input voltage with the ADC module and detect voltage transients with the High-Speed Analog Comparator module.

Figure 45-1: Standard High-Speed Analog Comparator Module Block Diagram

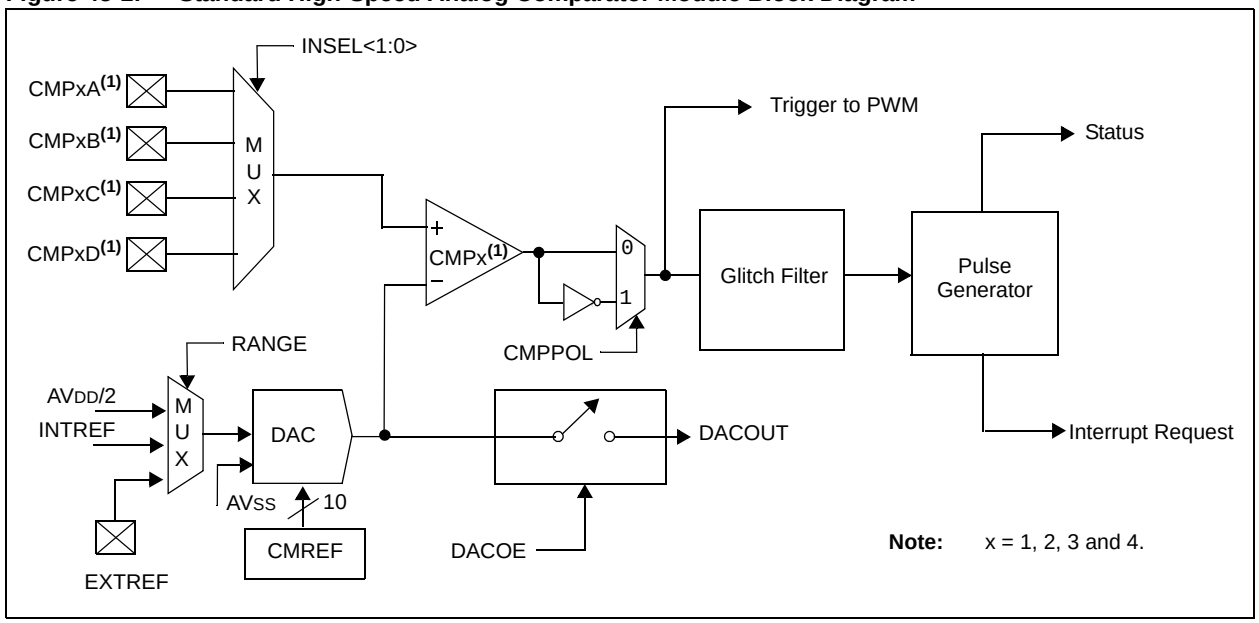
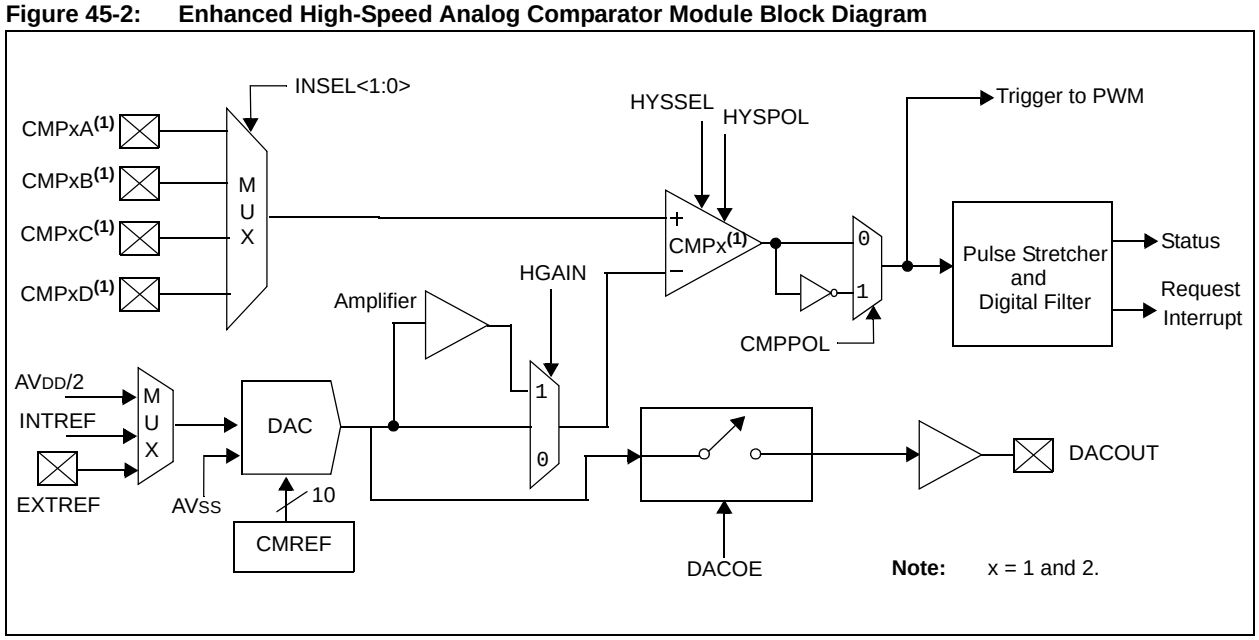


Figure 45-2: Enhanced High-Speed Analog Comparator Module Block Diagram



45.3 CONTROL REGISTERS

The following registers are used to configure the High-Speed Analog Comparator module:

- **CMPCONx: Comparator x Control Register**

  This register is used to configure the comparator voltage reference source, input pin and output polarity. Depending on the device variant, there are up to four individual registers (CMPCON1 to CMPCON4), which correspond to the respective comparator.

- **CMPDACx: Comparator x DAC Control Register**

  The contents of this register determine the threshold voltage for the comparator. Depending on the device variant, there are up to four individual registers (CMPDAC1 to CMPDAC4), which correspond to the respective comparator.

Register 45-1: CMPCONx: Comparator x Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPON	—	CMPSIDL	HYSSEL<1:0>		FLTREN	FCLKSEL	DACOE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
INSEL<1:0>		EXTREF	HYSPOL	CMPSTAT	HGAIN	CMPPOL	RANGE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMPON:** Comparator A/D Operating Mode bit
1 = Comparator module is enabled
0 = Comparator module is disabled (reduces power consumption)

bit 14 **Unimplemented:** Read as '0'

bit 13 **CMPSIDL:** Comparator Stop in Idle Mode bit
1 = The comparator clocks will be stopped and the bias current will be disabled. The comparators will not recover from Idle mode.
0 = No operational changes for the comparators from normal mode. The comparators will recover from Idle mode.
If a device has multiple comparators, any CMPSIDL bit set to '1' will disable all comparators while in Idle mode.

bit 12-11 **HYSSEL<1:0>:** Comparator Hysteresis Select bits
11 = 45 mV hysteresis
10 = 30 mV hysteresis
01 = 15 mV hysteresis
00 = No hysteresis selected

bit 10 **FLTREN:** Digital Filter Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled

bit 9 **FCLKSEL:** Digital Filter and Pulse Stretcher Clock Select bit
1 = Digital Filter and Pulse Stretcher operates with PWM clock
0 = Digital Filter and Pulse Stretcher operates with system clock

bit 8 **DACOE:** DAC Output Enable bit(1)
1 = DAC analog voltage is output to DACOUT pin(2)
0 = DAC analog voltage is not connected to DACOUT pin

bit 7-6 **INSEL<1:0>:** Comparator Input Source Select bits
11 = Select CMPxD input pin
10 = Select CMPxC input pin
01 = Select CMPxB input pin
00 = Select CMPxA input pin

bit 5 **EXTREF:** External Reference Enable bit
1 = External source provides reference to DAC (maximum DAC voltage determined by external voltage source)
0 = Internal reference sources provide reference to DAC (maximum DAC voltage determined by RANGE bit setting)

Note 1: The DACOE bit is not implemented in the dsPIC33FJ06GS001 device.
2: At any given time, DACOUT can only be associated with a single comparator.

Register 45-1: CMPCONx: Comparator x Control Register (Continued)

bit 4 **HYSPOL:** Comparator Hysteresis Polarity Select bit
1 = Hysteresis is applied to falling edge of the comparator output
0 = Hysteresis is applied to rising edge of the comparator output

bit 3 **CMPSTAT:** Current state of comparator output including CMPPOL selection

bit 2 **HGAIN:** DAC High Gain Enable bit
1 = Reference DAC output to comparator is scaled to 1.8 times
0 = Reference DAC output to comparator is scaled to 1.0 times

bit 1 **CMPPOL:** Comparator Output Polarity Control bit
1 = Output is inverted
0 = Output is not inverted

bit 0 **RANGE:** DAC Output Voltage Range bit
1 = High range: Maximum DAC value = AV_{DD}/2 (1.65V at 3.3V AV_{DD})
0 = Low range: Maximum DAC value = INTREF (1.2V ±1%)

Note 1: The DACOE bit is not implemented in the dsPIC33FJ06GS001 device.
2: At any given time, DACOUT can only be associated with a single comparator.

Register 45-2: CMPDACx: Comparator x DAC Control Register

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CMREF<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMREF<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **CMREF<9:0>:** Comparator Reference Voltage Select bits

1111111111 = (CMREF * INTREF/1024) or [CMREF * (AVDD/2)/1024] volts depending on RANGE bit, or (CMREF * EXTREF/1024) if the EXTREF bit is set

•

•

•

0000000000 = 0.0V

Note 1: When using an external reference source, the output voltage of the DAC is lower than the set value due to the presence of an internal Electrostatic Discharge (ESD) protection resistor. For a typical device with an internal ESD resistor of approximately 300Ω and EXTREF of 1.8V, the difference in output voltage of the DAC varies from 7 mV (for CMREF = 0x000) to 97 mV (for CMREF = 0x3FF).

2: The ESD resistor has no effect when using INTREF or AVDD/2 as the DAC reference source.

45.4 CONFIGURING THE HIGH-SPEED ANALOG COMPARATOR

The High-Speed Analog Comparator module is configured using the Comparator x Control (CMPCONx) register. The Comparator Input Source Select bits, INSEL<1:0> (CMPCONx<7:6>) are used to select the comparator input pin. The signal to be monitored must be connected to this pin.

The External Reference Enable bit, EXTREF (CMPCONx<5>), selects between an external reference source or the internal reference source. If the EXTREF bit is set (CMPCONx<5> = 1), the voltage applied to the EXTREF pin provides the comparator reference voltage.

If the EXTREF bit is cleared (CMPCONx<5> = 0), the DAC Output Voltage Range bit, RANGE (CMPCONx<0>), determines the comparator reference voltage. If low range is selected (CMPCONx<0> = 0), the internal band gap reference (INTREF) provides the comparator reference voltage. If high range is selected (CMPCONx<0> = 1), AVDD/2 provides the comparator reference voltage. The polarity of the analog comparator is selected by configuring the Comparator Output Polarity Control bit, CMPPOL (CMPCONx<1>).

45.4.1 10-Bit DAC

Each analog comparator in the High-Speed Analog Comparator module has a dedicated 10-bit DAC that is used to program the comparator threshold voltage.

Each DAC has an output enable bit in the DAC Output Enable bit, DACOE (CMPCONx<8>), that enables the DAC reference voltage to be an output on the device (DACOUT). The DACOUT can only be associated with a single comparator at any given time. When more than one DACOE bit (CMPCONx<8>) is set, the DACOUT pin will reflect the DAC output of the comparator with the highest priority. The comparator priority is based on the comparator number, with Comparator 1 having the highest priority.

The full range of the DAC (AVDD/2) will typically be used when the chosen input source pin is shared with an ADC input.

The reduced range option (INTREF) is typically used when monitoring currents through a current sense shunt resistor. Generally, the measured voltages in such applications are small (< 1.25V); therefore, the option of using a reduced reference range for the comparator extends the available DAC resolution in these applications. The use of an external reference enables the user to connect to a reference that better suits their application.

45.4.2 DAC Buffer Gain

The output of the DAC is amplified through the DAC buffer. The amplifier functions as a 1x gain amplifier, or as a 1.8x gain amplifier. The gain is selected by configuring the DAC High Gain Enable bit, HGAIN (CMPCONx<2>).

Using the 1.8x gain option will increase the reference voltage of the analog comparator up to a maximum of 3.0V. Selecting a higher reference voltage for the analog comparator can improve the signal-to-noise ratio in SMPS and motor control applications.

45.4.3 Pulse Stretcher

The analog comparator can respond to a very fast transient signals. To avoid a comparator malfunction, after choosing the comparator output polarity using the CMPPOL bit (CMPCONx<1>), the signal is passed to a pulse stretching circuit.

For reliable operation, the pulse stretcher waits for the comparator output to be in a high state or low state for at least three times the selected clock cycles or three PWM cycles. The digital filter and pulse stretcher clock are selected by configuring the Digital Filter and Pulse Stretcher Clock Select bit, FCLKSEL (CMPCONx<9>).

45.4.4 Digital Filter

The digital filter processes the comparator signal from the pulse stretcher circuit. The digital filter is enabled by the Digital Filter Enable bit, FLTREN (CMPCONx<10>). The digital filter operates with the clock selected by the FCLKSEL bit (CMPCONx<9>). The comparator signal must be stable either in a high state or low state for at least three times the selected clock cycles or three PWM cycles for it to pass through the digital filter.

45.4.5 Comparator Outputs

The selected output polarity, pulse stretched and digital filtered comparator signal are made available to the PWM module as a current-limit and/or Fault signal. The stretched and filtered comparator signal is then used as a status signal, and to generate interrupt request signals. The comparator signal to the PWM module is directly generated from the comparator output and is not filtered by the digital filter and pulse stretcher.

Note 1:	Some of the devices support four virtual RPn pins and these pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example the output of the analog comparator can be connected to RP26. This configuration allows the analog comparator output on RP26.
2:	Refer to the **"I/O Ports"** chapter in the specific device data sheet for the availability of Virtual pins.

Example 45-1: Remapping of Analog Comparator Output on the Virtual Pin

```
/* Remapping of  comparator output on the virtual pin*/
/* RP26 tied to Analog Comparator Output 2 */
   RPOR13bits.RP26R= 0b101000;
```

45.4.6 Interaction with Digital I/O Pin Buffers

When the High-Speed Analog Comparator module is enabled, and a pin is selected as the source for the comparator, the digital input buffer associated with that pin will be disabled. This is done to prevent excessive current in the digital buffer due to analog input voltages.

45.4.7 Glitch Filter

In many motor and power control applications, the analog comparator input signals can be corrupted by the large electromagnetic fields generated by the associated external switching power transistors. Corruption of the analog input signals to the comparator can cause unwanted comparator output transitions. The programmable digital output filter can minimize the effects of the input signal corruption.

The digital filter requires three consecutive input samples to be similar before the output of the filter can change state. Assuming the current state is '0', an input string of '001010110111' will only yield an output state of '1' at the end of the example sequence after the three consecutive '1's. Similarly, a sequence of three consecutive '0's are required before the output will change to a '0' state.

Because of the requirement of three similar consecutive states for the filter, the selected digital filter clock period must be one-third or less than the maximum desired comparator response time.

In Sleep mode or Idle mode, the glitch filter is bypassed to enable an asynchronous signal from the comparator to the interrupt controller. This asynchronous signal can be used to wake-up the processor from Sleep mode or Idle mode.

45.4.8 Analog Comparator Interrupt

The analog comparator interrupt can be used to service the comparator switching event and can be enabled or disabled from the interrupt controller. The analog comparator interrupt, if enabled, generates the comparator interrupt signal on the rising edge of the comparator output following the polarity processing through the CMPPOL bit (CMPCONx<1>), and the subsequent processing by the pulse stretcher and the digital filter logic.

It is very important that the interrupt be generated only on the selected rising edge and not on the subsequent falling edge. If the CMPPOL bit (CMPCONx<1>) is changed during operation, the CMPPOL bit (CMPCONx<1>) change will not cause an interrupt. Only the selected edge of an actual change of the comparator output status will initiate an interrupt.

Note:	To guarantee an interrupt request to pass through the glitch filter, the comparator output must remain active for at least three instruction cycles. The comparator signal to the PWM module is directly generated from the comparator output and does not get filtered by the digital filter and pulse stretcher.

45.4.9 Comparator Hysteresis Control

The Comparator Hysteresis Select bits, HYSSEL<1:0> (CMPCONx<12:11>), specify the amount of hysteresis for the analog comparator. The Comparator Hysteresis Polarity Select bit, HYSPOL (CMPCONx<4>), specifies whether hysteresis is applied to the rising edge or falling edge of the signal.

Configuration of hysteresis (see Example 45-2) helps the comparator to avoid oscillation (that is, toggling of the comparator output), which could be caused by noise in the non-inverting input.

Example 45-2: Configuration of Hysteresis Control

```
// Select comparator hysteresis
CMPCON1bits.HYSSEL = 3;    /* 45 mV hysteresis selected */
CMPCON1bits.HYSPOL = 0;    /* Hysteresis is applied to rising edge of the */
                           /* comparator output */
```

45.4.10 Operation in Sleep and Idle Modes

The comparator can be disabled while in Idle mode by setting the Comparator Stop in Idle Mode bit, CMPSIDL (CMPCONx<13>), to '1'. Setting the CMPSIDL bit (CMPCONx<13>) for any one of the comparators causes the entire High-Speed Analog Comparator module to be disabled while in Idle mode.

If the High-Speed Analog Comparator module is disabled (CMPCONx<15> = 0), all of the analog comparators and the DACs are disabled to reduce power consumption.

45.5 APPLICATION INFORMATION

The High-Speed Analog Comparator module provides comparators that can be used in many power conversion applications. The outputs of the High-Speed Analog Comparator module can be used to perform the following functions:

- Generate an interrupt
- Trigger an ADC sample and convert process
- Truncate the PWM signal (current-limit)
- Truncate the PWM period (current reset)
- Disable the PWM outputs (Fault latch)

The output of the High-Speed Analog Comparator module can be used in multiple modes at the same time. For example, comparator output can be used to generate an interrupt, have the ADC take a sample and convert it, and truncate the PWM output, all in response to a voltage being detected beyond its expected value.

The High-Speed Analog Comparator module can also be used to wake-up the system from Sleep mode or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

The potential applications of the High-Speed Analog Comparator module are numerous and varied. The following section describes some typical applications in power conversion circuits.

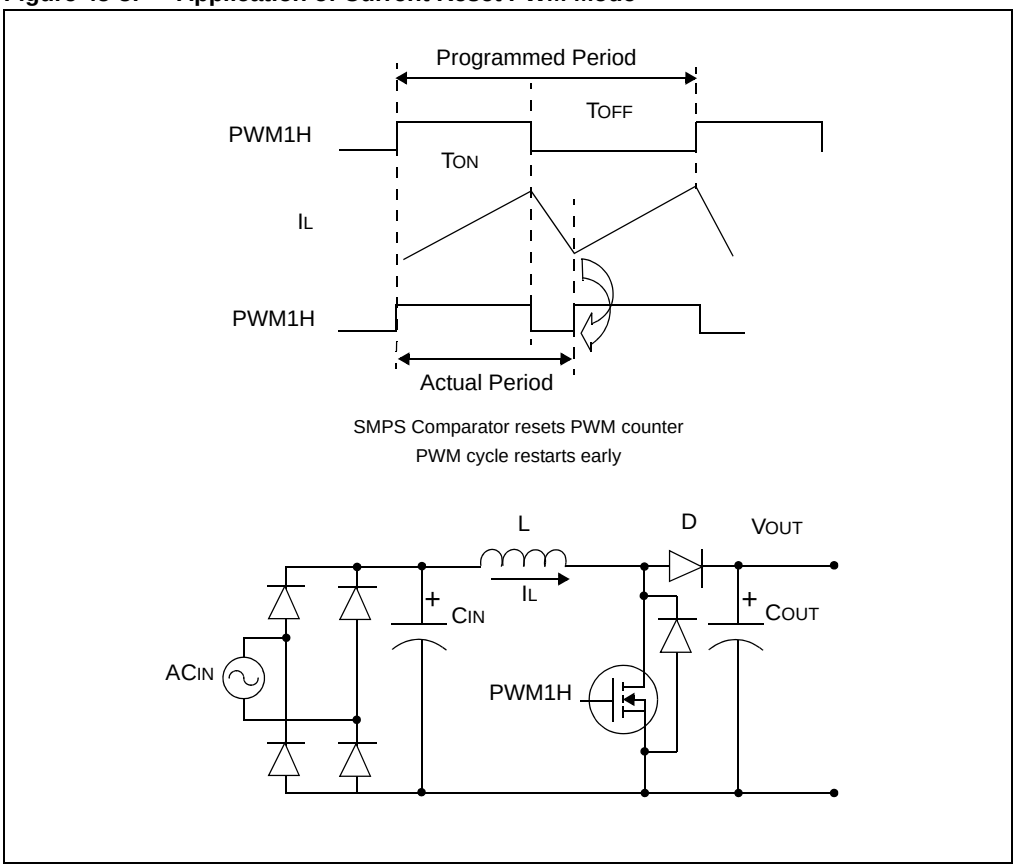
45.5.1 Power Factor Correction (PFC) Boost Converter: PWM Reset Using the High-Speed Analog Comparator

Analog comparators are widely used in PFC boost converter applications as illustrated in Figure 45-3. The High-Speed Analog Comparator module can be utilized for this application instead of adding expensive circuitry. The High-Speed Analog Comparator is used in conjunction with the High-Speed Power Supply PWM module to generate the Current Reset mode PWM signal. For more information on this PWM mode of operation, refer to **Section 43. "High-Speed PWM"** (DS70323).

The High-Speed Analog Comparator is configured to reset the PWM module when the measured current through the inductor falls below the minimum acceptable current level. This minimum current level is determined by the application.

Initially, the power semiconductor switch is turned ON. After a constant ON time, the switch is turned OFF and the PWM module waits for the current to decay below the comparator threshold. When the current falls below the threshold, the comparator resets the PWM module, turning the power semiconductor switch back ON, and thereby energizing the inductor.

Figure 45-3: Application of Current Reset PWM Mode



45.6 HIGH-SPEED ANALOG COMPARATOR LIMITATIONS

45.6.1 Comparator Input Range

The High-Speed Analog Comparator has a limitation for the input Common Mode Range (CMR) to not exceed (AVDD - 1.5V). The HGAIN bit (CMPCONx <2>) is enabled, and the High-Speed Analog Comparator input Common Mode Range (CMR) can be extended to 3V. This means that both inputs to the comparator (the selected CMPx input pin and the selected reference source) should be within this range. As long as one of the inputs is within the CMR, the comparator output will be correct. However, any input exceeding the CMR limitation will cause the comparator input to be saturated. If both inputs exceed the CMR, the comparator output will be indeterminate.

45.6.2 DAC Input Range

The maximum reference voltage input to the DAC should not exceed (AVDD - 1.6V). If the external reference voltage input exceeds this value, the DAC output will become indeterminate.

45.6.3 EXTREF Range

If EXTREF is selected as the comparator reference source, the voltage at the EXTREF pin should not exceed (AVDD - 1.5V). If the voltage at EXTREF pin exceeds this value, the comparator output may become unpredictable.

45.7 REGISTER MAP

A summary of the registers associated with the High-Speed Analog Comparator module is provided in Table 45-1.

Table 45-1: Analog Comparator Control Register Map(1)

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMPCONx	CMPON	—	CMPSIDL	HYSSEL<1:0>		FLTREN	FCLKSEL	DACOE	INSEL<1:0>		EXTREF	HYSPOL	CMPSTAT	HGAIN	CMPPOL	RANGE	0000
CMPDACx	—	—	—	—	—	—	CMREF<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Not all bits are available on all dsPIC33F/PIC24H devices. Refer to the specific device data sheet for more information.

45.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the High-Speed Analog Comparator module are:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33F/PIC24H device family.

45.9 REVISION HISTORY

Revision A (August 2007)

This is the initial released version of the document

Revision B (December 2010)

This revision includes the following updates:

- Added a note at the beginning of the section, which provides information on complementary documentation
- Updated the dsPIC33F references in the entire document as dsPIC33F/PIC24H
- Added **Figure 45-1: High-Speed Analog Comparator Equivalent Circuit**
- Updated the CMPSIDL bit definition in Register 45-1
- Added a note after Register 45-2
- Added **45.4.8 “Analog Comparator Interrupt”**
- Added **“If the High-Speed Analog Comparator module is disabled (CMPCONx<15> = 0), all of the analog comparators and the DACs are disabled to reduce power consumption.”**
- Changes to text and formatting were incorporated throughout the document

Revision C (June 2011)

This revision includes the following updates:

- Examples:
  - Added Example 45-2
- Figures:
  - Removed **Figure 45-1: High-Speed Analog Comparator Equivalent Circuit**
  - Added Figure 45-2
- Notes:
  - Removed Note 1 in Register 45-1
  - Added Note 2 in Register 45-1 and Register 45-2
  - Removed Note 3 in Register 45-2
  - Updated the Note in **45.4.8 “Analog Comparator Interrupt”**
  - Added Note 1 in Table 45-1
- Registers:
  - Updated Register 45-1
- Sections:
  - Updated **45.1 “Introduction”**
  - Updated the **CMPDACx: Comparator x DAC Control Register** description in **45.3 “Control Registers”**
  - Updated the third paragraph in **45.4 “Configuring the High-Speed Analog Comparator”**
  - Added the following sub sections: **45.4.2 “DAC Buffer Gain”**, **45.4.3 “Pulse Stretcher”**, **45.4.4 “Digital Filter”** and **45.4.5 “Comparator Outputs”**
  - Removed **45.4.6 “Programmable Hysteresis Band”**
  - Updated **45.4.7 “Glitch Filter”**
  - Updated **45.4.8 “Analog Comparator Interrupt”**
  - Added **45.4.10 “Operation in Sleep and Idle Modes”**
- Tables:
  - Updated Table 45-1
- Updated all dsPIC33F references to dsPIC33F/PIC24H
- Changes to text and formatting were incorporated throughout the document

Revision D (August 2012)

This revision incorporates the following updates:

- Examples:
  - Added Example 45-1 in **45.4.5 “Comparator Outputs”**
- Notes:
  - Added a note in **45.4.5 “Comparator Outputs”**
- Changes to text and formatting were incorporated throughout the document

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Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
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ASIA/PACIFIC

India - Bangalore
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Fax: 91-80-3090-4123

India - New Delhi
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Fax: 91-11-4160-8632

India - Pune
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Japan - Osaka
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Fax: 81-66-152-9310

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
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Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
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Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
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Taiwan - Hsin Chu
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Fax: 886-3-5770-955

Taiwan - Kaohsiung
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Taiwan - Taipei
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