Section 42. Oscillator (Part IV)

HIGHLIGHTS

This section of the manual contains the following major topics:

> **Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.
>
> Please consult the note at the beginning of the **"Oscillator Configuration"** chapter in the current device data sheet to check whether this document supports the device you are using.
>
> Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

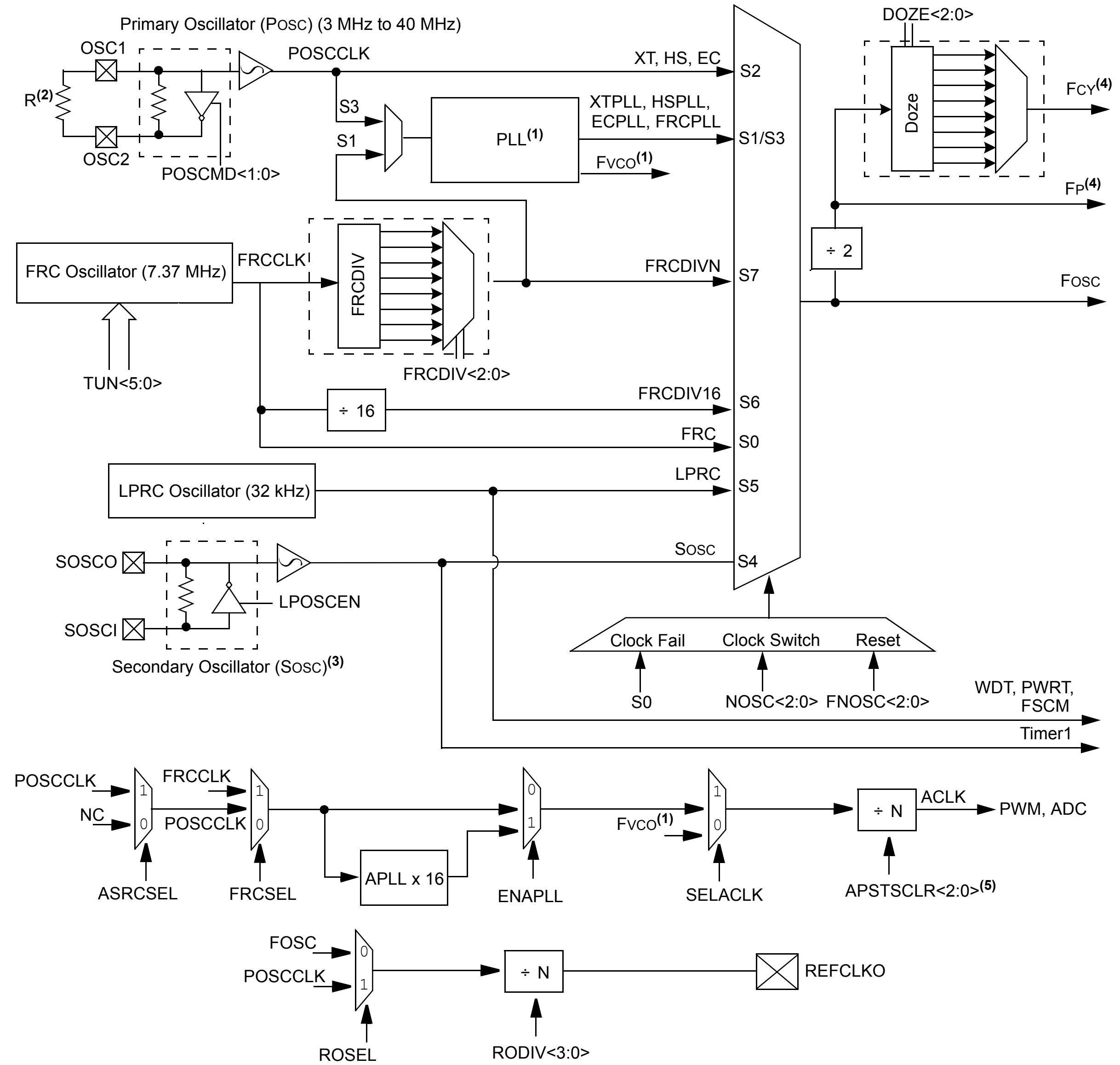
42.1 INTRODUCTION

The dsPIC33F/PIC24H oscillator system includes the following characteristics:

- External and internal oscillator options
- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on selected internal and external oscillator sources
- On-chip Auxiliary PLL to boost the internal operating frequency of the PWM and ADC
- On-the-fly clock switching between various clock sources
- Doze mode for system power-savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Nonvolatile Configuration bits for clock source selection
- Pseudo-random generator to trim the Fast RC (FRC) Oscillator

A block diagram of the dsPIC33F/PIC24H oscillator system is illustrated in Figure 42-1.

Figure 42-1: Oscillator System Block Diagram



Note 1: FVCO = 120 MHz only with a maximum 30 MIPS CPU operation. Refer to **42.7 "Phase-Locked Loop (PLL)"** for FVCO values.

2: If the oscillator is used with XT or HS modes, an external parallel resistor with the value of 1 MΩ must be connected.

3: The SOSC and its associated pins may not be available on all devices. Refer to the specific device data sheet for more information.

4: The term FP refers to the clock source for all the peripherals, while FCY refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used in any ratio other than 1:1, which is the default.

5: The auxiliary clock postscaler must be configured to Divide-by-1 (APSTSCLR<2:0> = `111`) for proper operation of the PWM module.

42.2 CPU CLOCKING

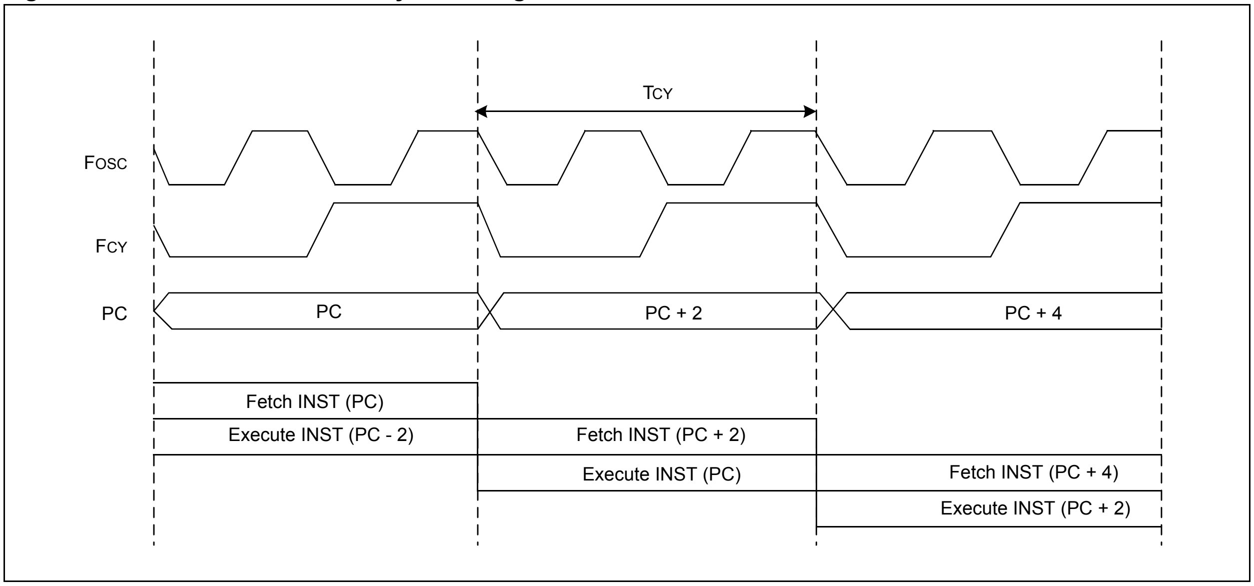
The system clock (FOSC) source can be provided by one of the following options:

- Primary Oscillator (POSC) on the OSC1 and OSC2 pins
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO pins
- Internal FRC Oscillator with optional clock divider
- Internal Low-Power RC (LPRC) Oscillator
- POSC with PLL
- Internal FRC Oscillator with PLL

The FOSC source is divided by two to produce the internal instruction cycle clock. In this document, the instruction cycle clock is denoted by FCY. The timing diagram in Figure 42-2, illustrates the relationship between the system clock (FOSC), the instruction cycle (FCY) and the Program Counter (PC).

The internal instruction cycle clock (FCY) can be output on the OSC2 I/O pin, if Primary Oscillator mode or High Speed Oscillator (HS) mode is not selected as the clock source. For more information about the POSC, refer to **42.5 "Primary Oscillator (POSC)"**.

Figure 42-2: Clock/Instruction Cycle Timing



42.3 OSCILLATOR CONFIGURATION REGISTERS

The Oscillator Configuration registers are located in the program memory space, and are not Special Function Registers (SFRs). These two registers are mapped into program memory space and are programmed at the time of device programming.

- **FOSCSEL: Oscillator Source Selection Register**

  FOSCSEL selects the initial oscillator source and start-up option. FOSCSEL contains the following Configuration bits:

  - Initial Oscillator Source Selection Configuration bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) determine the clock source that is used at a Power-on Reset (POR). Thereafter, the clock source can be changed between permissible clock sources with clock switching.

  The Internal FRC Oscillator with postscaler (FRCDIVN) is the default (unprogrammed) selection.

- **FOSC: Oscillator Configuration Register**

  FOSC configures Primary Oscillator mode, OSC2 pin function, peripheral pin select, and the fail-safe and clock switching modes. FOSC contains the following Configuration bits:

  - Primary Oscillator Mode Selection Configuration bits (POSCMD<1:0>) in the Oscillator Configuration register (FOSC<1:0>) select the operation mode of the POSC
  - OSC2 Pin Function Configuration bit (OSCIOFNC) in the Oscillator Configuration register (FOSC<2>) selects the OSC2 pin function, except in HS or Medium-Speed Oscillator (XT) mode:
    - If the OSCIOFNC bit is unprogrammed ('1'), the FCY clock is output on the OSC2 pin
    - If the OSCIOFNC bit is programmed ('0'), the OSC2 pin becomes a general purpose I/O pin

Table 42-1 lists the configuration settings that select the device oscillator source and operating mode at a POR.

Table 42-1: Configuration Bit Values for Clock Selection

Oscillator Source	Oscillator Mode	FNOSC Value	POSCMD Value	See Note
S0	Fast RC Oscillator (FRC)	000	xx	**1**
S1	Fast RC Oscillator with PLL (FRCPLL)	001	xx	**1**
S2	Primary Oscillator (EC)	010	00	**1**
S2	Primary Oscillator (XT)	010	01	—
S2	Primary Oscillator (HS)	010	10	—
S3	Primary Oscillator with PLL (ECPLL)	011	00	**1**
S3	Primary Oscillator with PLL (XTPLL)	011	01	—
S3	Primary Oscillator with PLL (HSPLL)	011	10	—
S4	Secondary Oscillator (SOSC)	100	xx	**3**
S5	Low-Power RC Oscillator (LPRC)	101	xx	**1**
S6	Fast RC Oscillator with /16 divider (FRCDIV16)	110	xx	**1**
S7	Fast RC Oscillator with /N divider (FRCDIVN)	111	xx	**1, 2**

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: Default Oscillator mode for an unprogrammed (erased) device.

3: The SOSC may not be available on all devices. Refer to the specific device data sheet for more information.

4: In some devices, Fuses are not implemented and functionality is supported through the configuration words. Refer to the specific device data sheet for more information.

Register 42-1: FOSCSEL: Oscillator Source Selection Register

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	U-1	U-1	U-1	U-1	R/P	R/P	R/P
IESO	—	—	—	—	FNOSC<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unused bits, program to Logic ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘1’

bit 7 **IESO:** Internal External Start-up Option bit

1 = Start-up device with the Internal FRC Oscillator, then automatically switch to the user-selected oscillator source when ready
0 = Start device with user-selected oscillator source

bit 6-3 **Unimplemented:** Read as ‘1’

bit 2-0 **FNOSC<2:0>:** Initial Oscillator Source Selection bits
111 = Fast RC Oscillator (FRC) with Divide-by-N (FRCDIVN)
110 = Fast RC Oscillator (FRC) with Divide-by-16 (FRCDIV16)
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)(1)
011 = Primary Oscillator with PLL (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

Note 1: This setting is not available on all devices. Refer to the specific device data sheet for more information.

Register 42-2: FOSC: Oscillator Configuration Register

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

R/P	R/P	R/P	U-1	U-1	R/P	R/P	R/P
FCKSM<1:0>		IOL1WAY(1)	—	—	OSCIOFNC	POSCMD<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unused bits, program to Logic ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘1’

bit 7-6 **FCKSM<1:0>:** Clock Switching Mode bits
1x = Clock switching is disabled, FSCM is disabled
01 = Clock switching is enabled, FSCM is disabled
00 = Clock switching is enabled, FSCM is enabled

bit 5 **IOL1WAY:** Peripheral Pin Select Configuration bit(1)
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 4-3 **Unimplemented:** Read as ‘1’

bit 2 **OSCIOFNC:** OSC2 Pin Function bit (except in XT and HS modes)
1 = OSC2 is clock output and instruction cycle (FCY) clock is output on OSC2 pin
0 = OSC2 is a general purpose digital I/O pin

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Mode Selection bits
11 = Primary Oscillator disabled
10 = HS (High-Speed) Crystal Oscillator mode
01 = XT (Crystal) Oscillator mode
00 = EC (External Clock) mode

Note 1: The IOL1WAY bit is not available on all devices. Refer to the specific device data sheet for more information.

42.4 SPECIAL FUNCTION REGISTERS (SFRs)

The following SFRs provide run-time control and status of the oscillator system:

- **OSCCON: Oscillator Control Register[1,3]**

  This register controls the clock switching and provides status information that allows the current clock source, PLL lock and clock fail conditions to be monitored.

- **CLKDIV: Clock Divisor Register[3]**

  This register controls the Doze mode and selects the PLL prescaler, PLL postscaler and FRC postscaler.

- **PLLFBD: PLL Feedback Divisor Register[1]**

  This register selects the PLL feedback divisor.

- **OSCTUN: FRC Oscillator Tuning Register[1]**

  This register is used to tune the internal FRC oscillator frequency in the application software. It allows the FRC oscillator frequency to be adjusted over a range of ±12%.

- **ACLKCON: Auxiliary Clock Control Register[1]**

  This register controls the auxiliary PLL mode and the auxiliary PLL clock divider.

- **REFOCON: Reference Oscillator Control Register**

  This register controls the reference oscillator output.

- **LFSR: Linear Feedback Shift Register**

  This register provides a pseudo-random FRC trim value.

Note:	The Oscillator SFRs (OSCCON, CLKDIV, PLLFBD, OSCTUN and ACLKCON) are reset only on a POR.

Register 42-3: OSCCON: Oscillator Control Register(1,3)

U-0	R-y	R-y	R-y	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0>(4)		
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	R/W-0	R/W-0
CLKLOCK	IOLOCK(5)	LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

Legend:	y = Value set from Configuration bits on POR		C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)(2)
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with PLL
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(4)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)(2)
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with PLL
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
If clock switching is enabled and FSCM is disabled, (FCKSM bit, FOSC<7:6> = '0b01)
1 = Clock switching is disabled. System clock source is locked
0 = Clock switching is enabled. System clock source can be modified by clock switching

bit 6 **IOLOCK:** Peripheral Pin Select Lock bit
1 = Peripherial Pin Select is locked. Write to Peripherial Pin Select registers not allowed
0 = Peripherial Pin Select is out of lock. Write to Peripherial Pin Select registers allowed

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock, or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1: Writes to this register require an unlock sequence. For more information and examples, refer to **42.12 “Clock Switching”**.
2: This setting is not available on all devices. Refer to the specific device data sheet for more information.
3: The OSCCON register can be reset only on a POR.
4: Direct clock switches between any primary oscillator mode with PLL and FRC PLL mode are not permitted. This applies to the clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
5: The IOLOCK bit is not available on all dsPIC33F/PIC24H devices. Refer to the specific device data sheet for more information.

Register 42-3: OSCCON: Oscillator Control Register(1,3) (Continued)

bit 4	**Unimplemented:** Read as '0'
bit 3	**CF:** Clock Fail Detect bit (read/clear by application) 1 = FSCM has detected clock failure 0 = FSCM has not detected clock failure
bit 2	**Unimplemented:** Read as '0'
bit 1	**LPOSCEN:** 32 kHz Secondary (LP) Oscillator Enable bit 1 = Enable Secondary Oscillator 0 = Disable Secondary Oscillator
bit 0	**OSWEN:** Oscillator Switch Enable bit 1 = Request oscillator switch to selection specified by NOSC<2:0> bits 0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. For more information and examples, refer to **42.12 "Clock Switching"**.

2: This setting is not available on all devices. Refer to the specific device data sheet for more information.

3: The OSCCON register can be reset only on a POR.

4: Direct clock switches between any primary oscillator mode with PLL and FRC PLL mode are not permitted. This applies to the clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

5: The IOLOCK bit is not available on all dsPIC33F/PIC24H devices. Refer to the specific device data sheet for more information.

Register 42-4: CLKDIV: Clock Divisor Register[3]

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE<2:0>[2]			DOZEN[1]	FRCDIV<2:0>		
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST<1:0>		—	PLLPRE<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit

1 = Interrupts will clear the DOZEN bit and the processor clock/peripheral clock ratio is set to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits[2]

111 = FCY/128
110 = FCY/64
101 = FCY/32
100 = FCY/16
011 = FCY/8 (default)
010 = FCY/4
001 = FCY/2
000 = FCY/1

bit 11 **DOZEN:** Doze Mode Enable bit[1]

1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock/peripheral clock ratio forced to 1:1

bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits

111 = FRC/256
110 = FRC/64
101 = FRC/32
100 = FRC/16
011 = FRC/8
010 = FRC/4
001 = FRC/2
000 = FRC/1 (default)

bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as ‘N2’, PLL postscaler)

11 = Output/8
10 = Reserved
01 = Output/4 (default)
00 = Output/2

bit 5 **Unimplemented:** Read as ‘0’

bit 4-0 **PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as ‘N1’, PLL prescaler)

11111 = Input/33
•
•
•
00001 = Input/3
00000 = Input/2 (default)

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.
2: For more information on Doze mode, refer to **Section 9. “Watchdog Timer (WDT) and Power-Saving Modes”** (DS70196).
3: The CLKDIV register can be reset only on a POR.

Register 42-5: PLLFBD: PLL Feedback Divisor Register(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as ‘M’, PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
000000010 = 4
000000001 = 3
000000000 = 2

Note 1: The PLLFBD register can be reset only on a POR.

Register 42-6: OSCTUN: FRC Oscillator Tuning Register(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits

111111 = Center frequency - 0.375% (7.345 MHz)
100001 = Center frequency - 11.625% (6.52 MHz)
100000 = Center frequency - 12% (6.49 MHz)
•
•
•
011111 = Center frequency + 11.625% (8.23 MHz)
011110 = Center frequency + 11.25% (8.20 MHz)
000001 = Center frequency + 0.375% (7.40 MHz)
000000 = Center frequency (7.37 MHz nominal)

Note 1: The OSCTUN register can be reset only on a POR.

Register 42-7: ACLKCON: Auxiliary Clock Control Register(1)

R/W-0	R-0	R/W-1	U-0	U-0	R/W-1	R/W-1	R/W-1
ENAPLL	APLLCK	SELACLK	—	—	APSTSCLR<2:0>		
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
ASRCSEL	FRCSEL	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ENAPLL:** Auxiliary PLL Enable bit
1 = Auxiliary PLL is enabled
0 = Auxiliary PLL is disabled

bit 14 **APLLCK:** Auxiliary PLL Locked Status bit (read-only)
1 = Auxiliary PLL is in lock
0 = Auxiliary PLL is not in lock

bit 13 **SELACLK:** Select Clock Source for Auxiliary Clock Divider bit
1 = Auxiliary PLL or FRC or POSC provides the source clock for the auxiliary clock divider
0 = PLL output (FVCO) provides the source clock for the auxiliary clock divider

bit 12-11 **Unimplemented:** Read as ‘0’

bit 10-8 **APSTSCLR<2:0>:** Auxiliary Clock Output Divider bits
111 = Divided by 1
110 = Divided by 2
101 = Divided by 4
100 = Divided by 8
011 = Divided by 16
010 = Divided by 32
001 = Divided by 64
000 = Divided by 256 (default)

bit 7 **ASRCSEL:** Select Reference Clock Source for Auxiliary Clock bit
1 = Primary Oscillator is the clock source
0 = No clock input is selected

bit 6 **FRCSEL:** Select Reference Clock Source for Auxiliary Clock bit
1 = Select FRC clock for clock source
0 = Input clock source is determined by ASRCSEL bit setting

bit 5-0 **Unimplemented:** Read as ‘0’

Note 1: The ACLKCON register can be reset only on a POR.

Register 42-8: REFOCON: Reference Oscillator Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV<3:0>(1)			
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference Oscillator output enabled on the REFCLKO pin
0 = Reference Oscillator output disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference Oscillator output continues to run in Sleep mode
0 = Reference Oscillator output is disabled in Sleep mode

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal used as the reference clock
0 = System clock used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits(1)
1111 = Divided by 32,768
1110 = Divided by 16,384
1101 = Divided by 8,192
1100 = Divided by 4,096
1011 = Divided by 2,048
1010 = Divided by 1,024
1001 = Divided by 512
1000 = Divided by 256
0111 = Divided by 128
0110 = Divided by 64
0101 = Divided by 32
0100 = Divided by 16
0011 = Divided by 8
0010 = Divided by 4
0001 = Divided by 2
0000 = Reference Oscillator source

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: The Reference Oscillator module must be disabled (ROON = 0) before writing to these bits.

Register 42-9: LFSR: Linear Feedback Shift Register

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	LFSR<14:8>						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LFSR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **LFSR<14:8>:** Most Significant 7 bits of the LFSR Register

bit 7-0 **LFSR<7:0>:** Least Significant 8 bits of the LFSR Register

42.5 PRIMARY OSCILLATOR (Posc)

The Primary Oscillator (POSC) is available on the OSC1 and OSC2 pins of the dsPIC33F/PIC24H device families. This connection enables an external crystal (or ceramic resonator) to provide the clock to the device. Optionally, the internal PLL can be used to boost the system frequency (FOSC) to 80 MHz for 40 MIPS execution. The POSC provides the following modes of operation:

- **Medium-Speed (XT Mode)**

  XT mode is a medium-gain, medium-frequency mode used to work with crystal frequencies of 3 MHz to 10 MHz.

- **High-Speed Oscillator (HS Mode)**

  HS mode is a high-gain, high-frequency mode used to work with crystal frequencies of 10 MHz to 40 MHz.

- **External Clock Source Operation (EC Mode)**

  If the on-chip oscillator is not used, EC mode allows the internal oscillator to be bypassed. The device clocks are generated from an external source (0.8 MHz to 64 MHz) and input on the OSC1 pin.

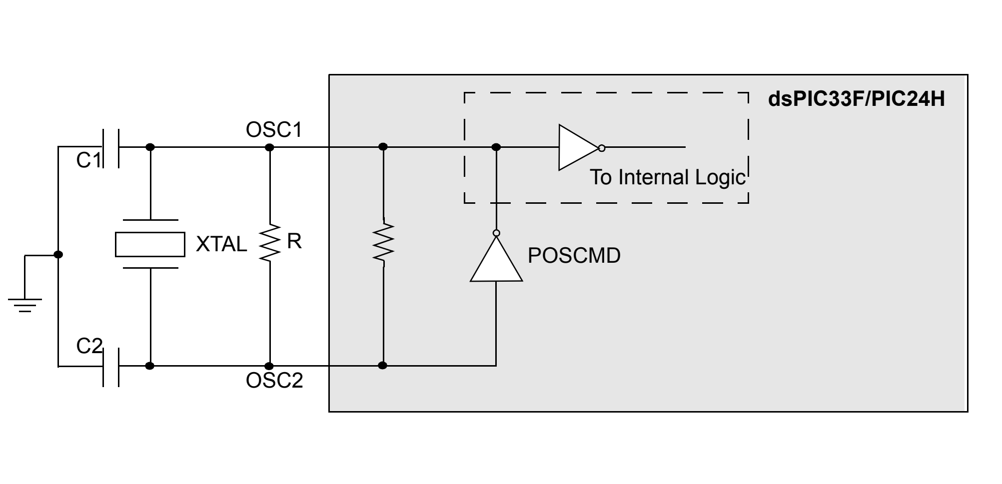
The FNOSC<2:0> Configuration bits in the Oscillator Source Selection register (FOSCSEL<2:0>) specify the POSC clock source at POR. The POSCMD<1:0> Configuration bits in the Oscillator Configuration register (FOSC<1:0>) specify the Primary Oscillator mode. Table 42-2 provides the options selected by specific bit configurations, which are programmed at the time of device programming.

Table 42-2: Primary Oscillator Clock Source Options

FNOSC Value	POSCMD	Primary Oscillator Source/Mode
011	00	Primary Oscillator with PLL: External Clock Mode (ECPLL)
011	01	Primary Oscillator with PLL: Crystal Oscillator with PLL Mode (XTPLL)
011	10	Primary Oscillator with PLL: High-Speed Oscillator with PLL Mode (HSPLL)
010	00	Primary Oscillator: External Clock Mode (EC)
010	01	Primary Oscillator: Crystal Oscillator Mode (XT)
010	10	Primary Oscillator: High-Speed Mode (HS)

A recommended crystal oscillator circuit diagram for the dsPIC33F/PIC24H devices is illustrated in Figure 42-3. Capacitors, C1 and C2, form the load capacitance for the crystal.

Figure 42-3: Crystal or Ceramic Resonator Operation (XT or HS Oscillator Mode)



42 Oscillator (Part IV)

The optimum load capacitance (C_L) for a given crystal is specified by the crystal manufacturer. Load capacitance can be calculated as shown in Equation 42-1.

Equation 42-1: Crystal Load Capacitance

$$C_L = C_S + \frac{C1 \times C2}{C1 + C2}$$

Where,

C_S = Stray capacitance

Assuming $C1 = C2$, Equation 42-2 gives the capacitor value (C1, C2) for a given load and stray capacitance.

Equation 42-2: External Capacitor for Crystal

$$C1 = C2 = 2(C_L - C_S)$$

For more information on crystal oscillators and their operation, refer to **42.6 "Internal FRC Oscillator"**.

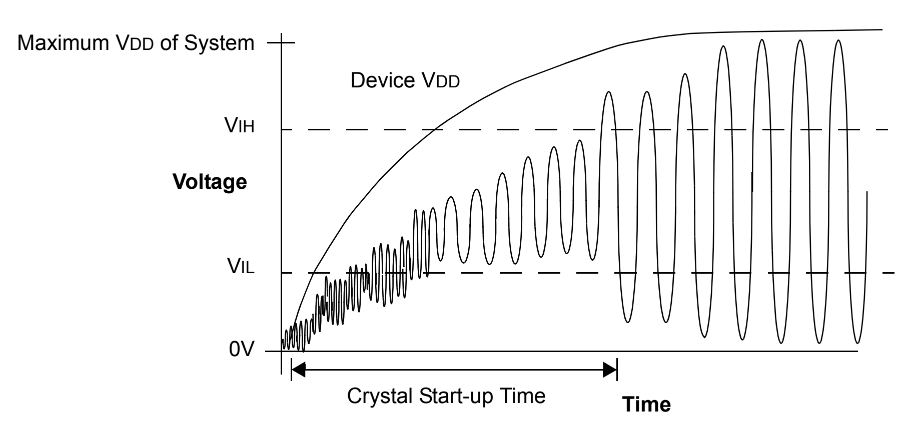
42.5.1 Oscillator Start-up Time

The oscillator starts oscillating as the device voltage increases from VSS. The time required for the oscillator to start oscillating depends on the following factors:

- Crystal and resonator frequency
- Capacitor values used (C1 and C2 in Figure 42-3)
- Device VDD rise time
- System temperature
- Series resistor value and type, if used
- Oscillator mode selection of device (selects the gain of the internal oscillator inverter)
- Crystal quality
- Oscillator circuit layout
- System noise

A graph of the typical oscillator/resonator start-up is illustrated in Figure 42-4.

Figure 42-4: Example of Oscillator/Resonator Start-up Characteristics



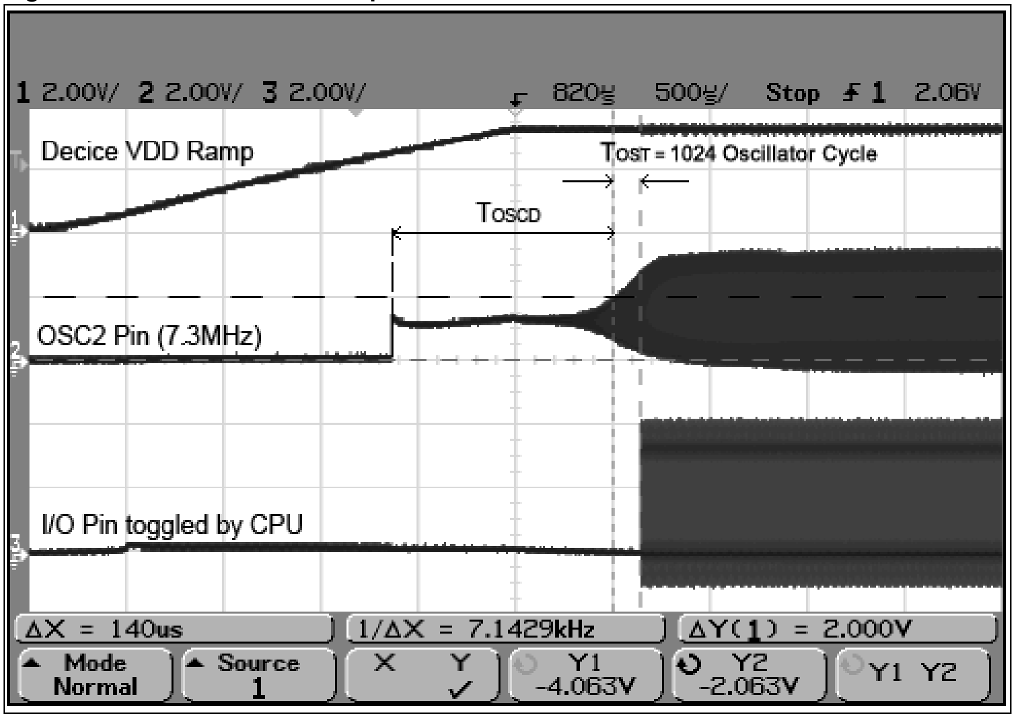
To ensure that a crystal oscillator (or ceramic resonator) has started and stabilized, an Oscillator Start-up Timer (OST) is provided with the POSC and SOSC. The OST is a simple 10-bit counter that counts 1024 cycles before releasing the oscillator clock to the rest of the system. This time-out period is denoted as TOST.

The amplitude of the oscillator signal must reach the VIL and VIH thresholds for the oscillator pins before the OST can begin to count cycles. The TOST interval is required every time the oscillator restarts (that is, on POR, BOR and wake-up from Sleep mode).

After the POSC is enabled, it takes a finite amount of time to start oscillating. This delay is denoted as TOSCD. After TOSCD, the OST timer takes 1024 clock cycles (TOST) to release the clock. The total delay for the clock to be ready is TOSCD + TOST. If the PLL is used, an additional delay is required for the PLL to lock (see **42.7 "Phase-Locked Loop (PLL)"**).

The POSC start-up behavior is illustrated in Figure 42-5, where the CPU starts toggling an I/O pin when it starts execution after the TOSCD + TOST interval.

Figure 42-5: Oscillator Start-up Characteristics



42.5.2 Primary Oscillator Pin Functionality

The Primary Oscillator pins (OSC1/OSC2) can be used for other functions when the oscillator is not being used.

The POSCMD Configuration bits in the Oscillator Configuration register (FOSC<1:0>) determine the oscillator pin function.

The OSCIOFNC bit (FOSC<2>) determines the OSC2 pin function. When FOSC<2> is '0', OSC2 is a general purpose digital I/O pin (see Figure 42-6). When FOSC<2> is '1', OSC2 is a clock output and the instruction cycle (FCY) clock is output on the OSC2 pin (see Figure 42-7).

The oscillator pin functions are shown in Table 42-3.

Table 42-3: Clock Pin Function Selection

Oscillator Source	OSCIOFNC<2> Value	POSCMD<1:0> Value	OSC1(1) Pin Function	OSC2(2) Pin Function
POSC Disabled	1	11	Digital I/O	Clock Output (FCY)
POSC Disabled	0	11	Digital I/O	Digital I/O
HS (High-Speed)	x	10	OSC1	OSC2
XT (Crystal)	x	01	OSC1	OSC2
EC (External Clock)	1	00	OSC1	Clock Output (FCY)
EC (External Clock)	0	00	OSC1	Digital I/O

Note 1: The OSC1 pin function is determined by the Primary Oscillator Mode Configuration bits (POSCMD<1:0>).

2: The OSC2 pin function is determined by the Primary Oscillator Mode Configuration bits (POSCMD<1:0>) and the OSC2 Pin Function Configuration bits (OSCIOFNC<2>).

Figure 42-6: OSC2 Pin for Digital I/O (in EC Mode), FOSC<2> = 0

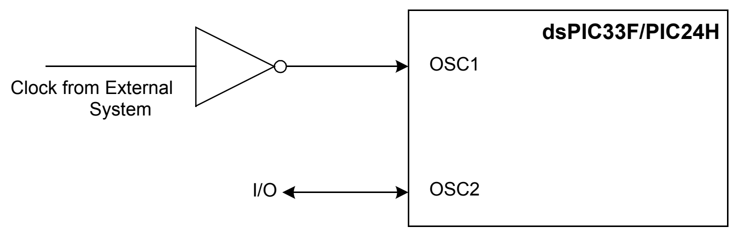
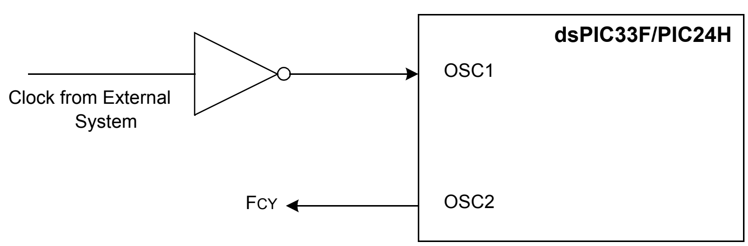


Figure 42-7: OSC2 Pin for Clock Output (in EC Mode), FOSC<2> = 1



42.6 INTERNAL FRC OSCILLATOR

The Internal FRC Oscillator provides a nominal 7.37 MHz clock without requiring an external crystal or ceramic resonator, which results in system cost savings for applications that do not require a precise clock reference.

The application software can tune the frequency of the oscillator from -12% to +11.625% (30 kHz steps) of the nominal frequency value using the FRC Oscillator Tuning bits (TUN<5:0>) in the FRC Oscillator Tuning register (OSCTUN<5:0>). The nominal or tuned frequency of the FRC Oscillator is expected to remain within ±2% of the tuned value over temperature and voltage variations of a particular device.

> **Note 1:** Refer to the specific device data sheet for the accuracy of the FRC clock frequency over temperature and voltage variations.
>
> **2:** The FRC Oscillator Tuning bits (TUN<5:0>) should not be changed dynamically when operating in internal FRC with PLL.
>
> To change the FRC Oscillator Tuning bits:
>
> a) Switch the clock to a non-PLL mode (for example, Internal FRC).
>
> b) Make the necessary changes.
>
> c) Switch the clock back to the PLL mode.

The Internal FRC Oscillator starts up immediately. Unlike a crystal oscillator, which can take several milliseconds to begin oscillation, the Internal FRC starts oscillating immediately.

The Initial Oscillator Source Selection Configuration bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) select the FRC clock source. The FRC clock source options at the time of a POR are provided in Table 42-4. The Configuration bits are programmed at the time of device programming.

Table 42-4: FRC Clock Source Options

FNOSC<2:0> Value	Primary Oscillator Source/Mode
111	FRC Oscillator: Postscaler Divide-by-N (FRCDIVN)
110	FRC Oscillator: Postscaler Divide-by-16 (FRCDIV16)
001	FRC Oscillator with PLL (FRCPLL)
000	FRC Oscillator (FRC)

42.6.1 FRC Postscaler Mode (FRCDIVN)

In FRC Postscaler mode, a variable postscaler divides the FRC clock output and allows a lower frequency to be chosen. The postscaler is controlled by the Internal FRC Oscillator Postscaler bits (FRCDIV<2:0>) in the Clock Divisor register (CLKDIV<10:8>). These bits allow for eight settings, from 1:1 to 1:256, as shown in Table 42-5.

Table 42-5: Internal Fast RC Oscillator Postscaler Settings

FRCDIV<2:0> Value	Internal FRC Oscillator Setting
111	FRC Divide-by-256
110	FRC Divide-by-64
101	FRC Divide-by-32
100	FRC Divide-by-16
011	FRC Divide-by-8
010	FRC Divide-by-4
001	FRC Divide-by-2
000	FRC Divide-by-1 (default)

Optionally, the FRC postscaler output can be used with the internal PLL to boost the system frequency (FOSC) to 80 MHz for 40 MIPS instruction cycle execution speed.

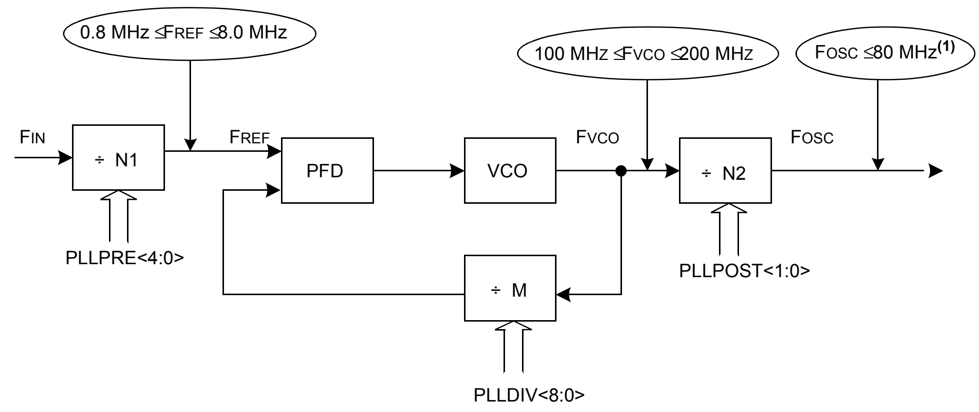
Note: The FRC divider should not be changed dynamically when operating in internal FRC with PLL. To change the FRC divider:

1. Switch the clock to non-PLL mode (for example, Internal FRC).
2. Make the necessary changes.
3. Switch the clock back to PLL mode.

42.7 PHASE-LOCKED LOOP (PLL)

The POSC and Internal FRC Oscillator sources can also be used with an on-chip PLL to obtain higher operating speeds. A block diagram of the PLL module is illustrated in Figure 42-8.

Figure 42-8: dsPIC33F/PIC24H PLL Block Diagram



Note 1: This specification is temperature dependent. Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for the exact value.

For proper PLL operation, the Phase Frequency Detector (PFD) input frequency and Voltage Controlled Oscillator (VCO) output frequency must meet the following requirements:

- The PFD input frequency (FREF) must be in the range of 0.8 MHz to 8.0 MHz
- The VCO output frequency (FVCO) must be in the range of 100 MHz to 200 MHz

The PLL Phase Detector Input Divider Select bits (PLLPRE<4:0>) in the Clock Divisor register (CLKDIV<4:0>) specify the input divider ratio (N1), which is used to scale down the input clock (FIN) to meet the PFD input frequency range of 0.8 MHz to 8 MHz.

The PLL Feedback Divisor bits (PLLDIV<8:0>) in the PLL Feedback Divisor register (PLLFBD<8:0>) specify the divider ratio (M), which scales down the VCO frequency (FVCO) for feedback to the PFD. The VCO frequency (FVCO) is 'M' times the input reference clock (FREF).

The PLL VCO Output Divider Select bits (PLLPOST<1:0>) in the Clock Divisor register (CLKDIV<7:6>) specify the divider ratio (N2) to limit the system clock frequency (FOSC) to 80 MHz.

Equation 42-3 provides the relation between the input frequency (FIN) and the output frequency (FOSC).

Equation 42-3: Fosc Calculation

$$F_{OSC} = F_{IN}\left(\frac{M}{N1 \times N2}\right) = F_{IN}\left(\frac{PLLDIV + 2}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where,

$N1 = PLLPRE + 2$

$N2 = 2 \times (PLLPOST + 1)$

$M = PLLDIV + 2$

Equation 42-4 provides the relation between the input frequency (FIN) and the VCO frequency (FVCO).

Equation 42-4: Fvco Calculation

$$F_{VCO} = F_{IN}\left(\frac{M}{N1}\right) = F_{IN}\left(\frac{PLLDIV + 2}{PLLPRE + 2}\right)$$

42.7.1 Input Clock Limitation at Start-up for PLL Mode

Table 42-6 provides the default values of the PLL Prescaler, PLL Postscaler and PLL Feedback Divisor Configuration bits at a POR.

Table 42-6: PLL Mode Defaults

Register	Bit Field	Value at POR Reset	PLL Divider Ratio
CLKDIV<4:0>	PLLPRE<4:0>	00	N1 = 2
CLKDIV<7:6>	PLLPOST<1:0>	01	N2 = 4
PLLFBD<8:0>	PLLDIV<8:0>	000110000	M = 50

Given these Reset values, Equation 42-5, Equation 42-6 and Equation 42-7 provide the relationship between the input frequency (FIN) and PFD input frequency (FREF), and the VCO frequency (FVCO) and system clock frequency (FOSC) at a POR.

Equation 42-5: FREF at POR

$$F_{REF} = FIN\left(\frac{1}{M}\right) = 0.5 \times F_{IN}$$

Equation 42-6: FVCO at POR

$$F_{VCO} = FIN\left(\frac{M}{N1}\right) = FIN\left(\frac{50}{2}\right) = 25(FIN)$$

Equation 42-7: FOSC at POR

$$FOSC = FIN\left(\frac{\mathrm{M}}{\mathrm{N1} \cdot \mathrm{N2}}\right) = 6.25(FIN)$$

Given the preceding equations at POR, the input frequency (FIN) to the PLL module must be limited to 4 MHz < FIN < 8 MHz to comply with the VCO output frequency requirement (100M < FVCO < 200M), if the default values of PLLPRE, PLLPOST and PLLDIV are used.

The POSC can support the following input frequency ranges, which are not within the frequency limit required (4 MHz < FIN < 8 MHz) at a POR:

- POSC in XT mode supports: 3.5 MHz to 10 MHz crystal
- POSC in HS mode supports: 10 MHz to 40 MHz crystal
- POSC in EC mode supports: 0.8 MHz to 64 MHz input

To use the PLL when the input frequency is not within the 4 MHz to 8 MHz range, follow the process given below:

1. Power-up the device with Internal FRC or POSC, without a PLL.
2. Change the PLLDIV, PLLPRE and PLLPOST bit values, based on the input frequency, to meet these PLL requirements:
   - The FREF must be in the range of 0.8 MHz to 8.0 MHz
   - The FVCO must be in the range of 100 MHz to 200 MHz
3. Switch the clock to the PLL mode in the user-assigned software.

42.7.2 PLL Lock Status

Whenever the PLL input frequency, the PLL prescaler or the PLL feedback divisor, is changed, the PLL requires a finite amount of time (TLOCK) to synchronize to the new settings.

TLOCK is applied when the PLL is selected as the clock source at POR, or during a clock switching operation. The value of TLOCK is relative to the time at which the clock is available to the PLL input. For example, with the POSC, TLOCK starts after the OST delay. For more information about start-up delay, refer to **42.5.1 "Oscillator Start-up Time"**. Refer to the specific device data sheet for information about typical TLOCK values.

The PLL Lock Status bit (LOCK) in the Oscillator Control register (OSCCON<5>) is a read-only bit that indicates the Lock status of the PLL. The LOCK bit is cleared at POR and on a clock-switch operation, when the PLL is selected as the destination clock source. It remains clear when any clock source not using the PLL is selected. It is a good practice to wait for the LOCK bit to be set before executing code after a clock switch event in which the PLL is enabled.

Note:	The PLL Prescaler bit (PLLPRE) and the PLL Feedback Divisor bit (PLLDIV) should not be changed when operating in PLL mode. You must clock switch to a non-PLL mode (for example, Internal FRC), to make the necessary changes, and then clock switch back to PLL mode

42.7.2.1 SETUP FOR USING PLL WITH THE POSC

The following process can be used to set up the PLL to operate the device at 40 MIPS with a 10 MHz external crystal:

1. To execute instructions at 40 MHz, ensure that the required system clock frequency is FOSC = 2 * FCY = 80 MHz.
2. Ensure that the default Reset values of PLLPRE, PLLPOST and PLLDIV meet PLL and user requirements.
3. If the PLL and user requirements are met, directly configure the FNOSC bits (FOSCSEL<2:0>) to select the Primary Oscillator with PLL at POR.

   If the PLL and user requirements are not met, follow these steps:

   a) Select the PLL postscaler to meet the VCO output frequency requirement (100 < FVCO < 200 MHz).
   b) Select the PLL prescaler to meet the PFD input frequency requirement (0.8 < FREF < 8 MHz).
   c) Select the PLL feedback divisor to generate the required VCO output frequency based on the PFD input frequency.
   d) Configure the FNOSC bits (FOSCSEL<2:0>) to select a clock source without the PLL (for example, Internal FRC) at POR.
   e) In the main program, change the PLL prescaler, PLL postscaler and PLL feedback divisor values to the values obtained in the previous steps, and then perform a clock switch to PLL mode.

Example 42-1 illustrates the code for using PLL with the POSC. For the clock switching code example, refer to **42.12 "Clock Switching"**.

Example 42-1: Code Example for Using PLL with 10 MHz Posc Crystal

```
_FOSCSEL(FNOSC_FRC & IESO_OFF);   // Internal FRC start-up without PLL,
                                  // no Two Speed Start-up
_FOSC(FCKSM_CSECMD & OSCIOFNC_OFF & POSCMD_XT);  // Clock switch enabled,
                                                 // Primarly Oscillator XT
_FWDT(FWDTEN_OFF);                // Watchdog Timer disabled
_FPOR(PPWRT_PWR128);              // Power-up Timer enabled 128 ms
_FICD(JTAGEN_OFF);                // Disable JTAG

int main()
{

// Configure PLL prescaler, PLL postscaler, PLL divisor
PLLFBD=30;            // M = 32
CLKDIVbits.PLLPOST=0; // N2 = 2
CLKDIVbits.PLLPRE=0;  // N1 = 2

// Initiate Clock Switch to Primary Oscillator with PLL (NOSC = 0b011)
__builtin_write_OSCCONH(0x03);
__builtin_write_OSCCONL(OSCCON | 0x01);

// Wait for Clock switch to occur
while (OSCCONbits.COSC != 0b011);

// Wait for PLL to lock
while(OSCCONbits.LOCK!=1) {};

}
```

42.7.2.2 SETUP FOR USING PLL WITH 7.37 MHz INTERNAL FRC

The following process is used to set up the PLL to operate the device at 40 MIPS with a 7.37 MHz Internal FRC.

1. To execute instructions at 40 MHz, ensure that the system clock frequency is $F_{OSC} = 2 * F_{CY} = 80$ MHz.
2. Ensure that the default Reset values of PLLPRE, PLLPOST and PLLDIV meet PLL and user requirements:
3. If the PLL and user requirements are met, directly configure the FNOSC bits (FOSCSEL<2:0>) to select the POSC with PLL at a POR.

   If the PLL and user requirements are not met, follow these steps:

   a) Select the PLL postscaler to meet the VCO output frequency requirement ($100 < F_{VCO} < 200$ MHz).
   b) Select the PLL prescaler to meet the PFD input frequency requirement ($0.8 < F_{REF} < 8$ MHz).
   c) Select the PLL feedback divisor to generate the required VCO output frequency based on the PFD input frequency.
   d) Configure the FNOSC bits (FOSCSEL<2:0>) to select a clock source without the PLL (for example, Internal FRC Oscillator) at POR.
   e) In the main program, change the PLL prescaler, PLL postscaler and PLL feedback divisor to meet the PLL and user requirements, and then perform a clock switch to PLL mode.

Example 42-2 illustrates the code for using PLL with a 7.37 MHz Internal FRC. For the clock switching code example, refer to **42.12 "Clock Switching"**.

Example 42-2: Code Example for Using the PLL with 7.37 MHz Internal FRC Oscillator

```
_FOSCSEL(FNOSC_FRC & IESO_OFF);   // Internal FRC start-up without PLL,
                                  // no Two Speed Start-up
_FOSC(FCKSM_CSECMD & OSCIOFNC_OFF & POSCMD_XT);  // Clock switch enabled,
                                                 // Primarly Oscillator XT
_FWDT(FWDTEN_OFF);                // Watchdog Timer disabled
_FPOR(PPWRT_PWR128);              // Power-up Timer enabled 128 ms
_FICD(JTAGEN_OFF);                // Disable JTAG

int main()
{

// Configure PLL prescaler, PLL postscaler, PLL divisor
PLLFBD = 63;           // M = 65
CLKDIVbits.PLLPOST=0;  // N2 = 2
CLKDIVbits.PLLPRE=1;   // N1 = 3

// Initiate Clock Switch to Internal FRC with PLL (NOSC = 0b001)
__builtin_write_OSCCONH(0x01);
__builtin_write_OSCCONL(OSCCON | 0x01);

// Wait for Clock switch to occur
while (OSCCONbits.COSC != 0b001);

// Wait for PLL to lock
while(OSCCONbits.LOCK!=1) {};

}
```

42.8 SECONDARY OSCILLATOR (SOSC)

The Secondary Oscillator (SOSC) enables a 32.768 kHz crystal oscillator to be attached to the dsPIC33F/PIC24H device as a secondary crystal clock source for low-power operation. It uses the SOSCI and SOSCO pins. The SOSC can also drive Timer1 for Real-Time Clock (RTC) applications.

> **Note 1:** The SOSC is sometimes referred to as the Low-Power Secondary Oscillator due to its low-power capabilities. However, this oscillator should not be confused with the Low-Power RC (LPRC) Oscillator.
>
> **2:** In addition, this oscillator is not available on all devices. Refer to the specific device data sheet for more information.

42.8.1 SOSC for System Clock

The SOSC is enabled as the system clock when:

- The Initial Oscillator Source Selection Configuration bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) are appropriately set to select the SOSC at a POR
- The user-assigned software initiates a clock switch to the SOSC for low-power operation

When the SOSC is not being used to provide the system clock, or the device enters Sleep mode, the SOSC is disabled to save power.

42.8.2 SOSC Start-up Delay

When the SOSC is enabled, it takes a finite amount of time to start oscillating. For more information, refer to **42.5.1 "Oscillator Start-up Time"**.

42.8.3 Continuous SOSC Operation

Optionally, you can leave the SOSC running continuously. The SOSC is always enabled if the Secondary Oscillator Enable bit (LPOSCEN) is set in the Oscillator Control register (OSCCON<1>).

There are two reasons to leave the SOSC running:

- Keeping the SOSC always ON allows a fast switch to the 32 kHz system clock for lower-power operation, since returning to the faster main oscillator still requires an oscillator start-up time, if it is a crystal type source. For more information, refer to **42.5.1 "Oscillator Start-up Time"**.
- The oscillator should remain on continuously when Timer1 is used as an RTC.

> **Note:** In Sleep mode, all clock sources (the POSC, Internal FRC Oscillator and LPRC Oscillator) are shut down, with the exception of the SOSC and LPRC under certain conditions. If the Watchdog Timer is enabled, LPRC is always active, even during Sleep mode. The SOSC can be active in Sleep mode, if the Secondary Oscillator Enable bit (LPOSCEN) is set in the Oscillator Control register (OSCCON<1>).

42.9 LOW-POWER RC (LPRC) OSCILLATOR

The Low-Power RC (LPRC) Oscillator provides a nominal clock frequency of 32 kHz. The LPRC Oscillator is the clock source for the Power-Up Timer (PWRT), Watchdog Timer (WDT) and FSCM circuits. It can also be used to provide a low-frequency clock source option for the device in those applications where power consumption is critical and timing accuracy is not required.

Note:	The clock frequency of the LPRC Oscillator will vary depending on the device voltage and operating temperature. Refer to the **“Electrical Characteristics”** section in the specific device data sheet for more information.

42.9.1 LPRC Oscillator for System Clock

The LPRC Oscillator is selected as the system clock in the following conditions:

- The Initial Oscillator Source Selection bits (FNOSC<2:0>) in the Oscillator Source Selection register (FOSCSEL<2:0>) are appropriately set to select the LPRC Oscillator at a POR
- The user-assigned software initiates a clock switch to the LPRC Oscillator for low-power operation

42.9.2 Enabling the LPRC Oscillator

The LPRC Oscillator is the clock source for the PWRT, WDT and FSCM. The LPRC Oscillator is enabled on a POR, and if the Power-on Reset Timer Value Select bits (FPWRT) in the POR Configuration Fuse register (FPOR<2:0>) are set.

The LPRC Oscillator remains enabled under these conditions:

- The FSCM is enabled
- The WDT is enabled
- The LPRC oscillator is selected as the system clock

If none of these conditions is true, the LPRC Oscillator shuts off after the PWRT expires. The LPRC Oscillator is shut off in Sleep mode.

Note:	The LPRC Oscillator runs in Sleep mode only if the WDT is enabled. Under all other conditions, the LPRC Oscillator is disabled in Sleep mode.

42.9.3 LPRC Oscillator Start-up Delay

The LPRC Oscillator starts up immediately, unlike a crystal oscillator, which can take several milliseconds to begin oscillation.

42.10 AUXILIARY PLL MODULE FOR ADC AND PWM SYSTEM CLOCK

The Auxiliary PLL can be used to provide a high-speed clock to peripherals such as the PWM and the ADC. The ACLKCON register selects the reference clock and output dividers for obtaining the necessary auxiliary clock for the PWM and ADC modules. The auxiliary clock for the PWM and ADC can be either:

- Internal FRC Oscillator (7.37 MHz nominal)
- Primary Oscillator
- Internal FRC Oscillator with PLL
- Primary Oscillator with PLL
- Auxiliary PLL

42.10.1 Enabling the Auxiliary PLL

To enable the Auxiliary PLL, the following steps must be performed:

1. Select the reference clock for the Auxiliary PLL by setting the ASRCSEL bit (ACLKCON<7>) for the POSC, or by setting the FRCSEL bit (ACLKCON<6>) for the Internal FRC Oscillator.
2. Enable the Auxiliary PLL by setting the ENAPLL bit (ACLKCON<15>).
3. Select the clock source for the auxiliary clock output divider by setting the SELACLK bit (ACLKCON<13>).
4. Select the appropriate clock divider by setting the APSTSCLR<2:0> bits (ACLKCON<10:8>).
5. Ensure that the Auxiliary PLL has locked and is ready for operation. This is done by polling the APLLCK bit (ACLKCON<14>).

Example 42-3 illustrates a code example to set up the Auxiliary PLL for 120 MHz, using the Internal FRC Oscillator as a clock reference.

Example 42-3: Enabling the Auxiliary PLL

```
ACLKCONbits.FRCSEL = 1;    /* Internal FRC is clock source for auxiliary PLL */
ACLKCONbits.ENAPLL = 1;    /* APLL is enabled */
ACLKCONbits.SELACLK = 1;   /* Auxiliary PLL provides the source clock for the */
                           /* clock divider */
ACLKCONbits.APSTSCLR = 7;  /* Auxiliary Clock Output Divider is Divide-by-1 */

while(ACLKCONbits.APLLCK != 1){}; /* Wait for Auxiliary PLL to Lock */

/* Given a 7.5MHz input from the FRC the Auxiliary Clock for the ADC and PWM */
/* modules are 7.5MHz * 16 = 120MHz */
```

Note 1: If the Primary PLL is used as a source for the auxiliary clock, then the Primary PLL should be configured up to a maximum operation of 30 MIPS or less.

2: To achieve 1.04 ns PWM resolution, the auxiliary clock must use the x16 Auxiliary PLL and be set up for 120 MHz. All other clock sources will have a minimum PWM resolution of 8 ns.

3: By using various combinations of clock inputs and PLL settings, it is possible to configure the oscillator out of specification. The user-assigned software must ensure that the Auxiliary Clock is configured to be within the electrical specification range of 112 MHz to 120 MHz.

42.10.2 Auxiliary Clock Divider

The Auxiliary Clock Output Divider bits (APSTSCLR<2:0>) in the Auxiliary Clock Control register (ACLKCON<10:8>) divide the auxiliary clock, which allow a lower frequency to be chosen. These bits allow for eight postscaler settings, from 1:1 to 1:256, as shown in Table 42-7.

The auxiliary clock postscaler must be configured to Divide-by-1 (APSTSCLR<2:0> = `111`) for proper operation of the PWM module.

Table 42-7: Auxiliary Clock Output Divider Settings

APSTSCLR<2:0> Bit Value	Auxiliary Oscillator Setting
111	Divide-by-1
110	Divide-by-2
101	Divide-by-4
100	Divide-by-8
011	Divide-by-16
010	Divide-by-32
001	Divide-by-64
000	Divide-by-256 (default setting)

42.10.3 Linear Feedback Shift Register (LFSR)

The pseudo-random number generator is incremented every PWM cycle. The Least Significant bits (LSbs) can be used to add to the period, and to dither the PWM edges (for EMI).

42.11 FAIL-SAFE CLOCK MONITOR (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate in the event of an oscillator failure. The FSCM function is enabled by programming the Clock Switching Mode Configuration bits (FCKSM<1:0>) in the Oscillator Configuration register (FOSC<7:6>) at the time of device programming. When the FSCM is enabled (FCKSM = `00`), the LPRC internal oscillator will run at all times except during Sleep mode.

The FSCM monitors the system clock. If it does not detect a system clock within a specific period of time (typically 2 ms, maximum 4 ms), it generates a clock failure trap and switches the system clock to the FRC oscillator. The user-assigned software then has the option to either attempt to restart the oscillator or execute a controlled shutdown.

> **Note:** The FSCM does not wake-up the device, if the clock fails while the device is in Sleep mode.

The FSCM takes the following actions when it switches to the FRC oscillator:

- The Current Oscillator Selection bits, COSC<2:0> (OSCCON<14:12>), are loaded with '`000`' (Internal FRC)
- The Clock Fail Detect bit, CF (OSCCON<3>), is set to indicate the clock failure
- The Oscillator Switch Enable control bit, OSWEN (OSCCON<0>), is cleared to cancel any pending clock switches
- The Interrupt Status bit, OSCFAIL (INTCON1<1>), is set and must be cleared by user software
- An oscillator fail trap interrupt is taken

42.11.1 FSCM Delay

The FSCM monitors the system clock for activity after the system clock is ready and the nominal delay (TFSCM) has elapsed.

The FSCM delay (TFSCM) is applied when the FSCM is enabled and the POSC or SOSC is selected as the system clock. For more information, refer to **Section 8. "Reset"** (DS70192).

> **Note:** Refer to the **"Electrical Characteristics"** section of the specific device data sheet for TOSC values.

42.11.2 FSCM and WDT

The FSCM and WDT use the LPRC oscillator as their time base. In the event of a clock failure, the WDT is unaffected and continues to run on the LPRC.

42.12 CLOCK SWITCHING

Clock switching can be initiated as a result of a hardware event or a software request. Typical scenarios include:

- Two-Speed Start-up sequence on a POR, which initially uses the internal FRC oscillator for quick start-up, and then automatically switches to the selected clock source when the clock is ready
- The FSCM automatically switches to Internal FRC Oscillator on a clock failure
- The user-assigned software requests clock switching by setting the OSWEN bit (OSCCON<0>), causing the hardware to switch to the clock source selected by the NOSC bits (OSCCON<10:8>) when the clock is ready

In each of these cases, the clock switch event assures that the proper make-before-break sequence is executed. That is, the new clock source must be ready before the old clock is deactivated and code must continue to execute as clock switching occurs.

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) that are under software control at any time. To limit the possible side effects that could result from this flexibility, dsPIC33F/PIC24H devices have a safeguard lock built into the switch process. That is, the OSCCON register is write-protected during clock switching.

42.12.1 Enabling Clock Switching

The Clock Switching Mode Configuration bits (FCKSM<1:0>) in the Oscillator Configuration register (FOSC<7:6>) must be programmed to enable clock switching and the FSCM (see Table 42-8).

Table 42-8: Configurable Clock Switching Modes

FCKSM<1:0> Values	Clock Switching Configuration	FSCM Configuration
`1x`	Disabled	Disabled
`01`	Enabled	Disabled
`00`	Enabled	Enabled

The first bit determines if clock switching is enabled (‘0’) or disabled (‘1’). The second bit determines if the FSCM is enabled (‘0’) or disabled (‘1’). FSCM can only be enabled if clock switching is also enabled. If clock switching is disabled (‘1’), the value of the second bit is irrelevant.

42.12.2 Clock Switch Sequence

The recommended process for a clock switch is as follows:

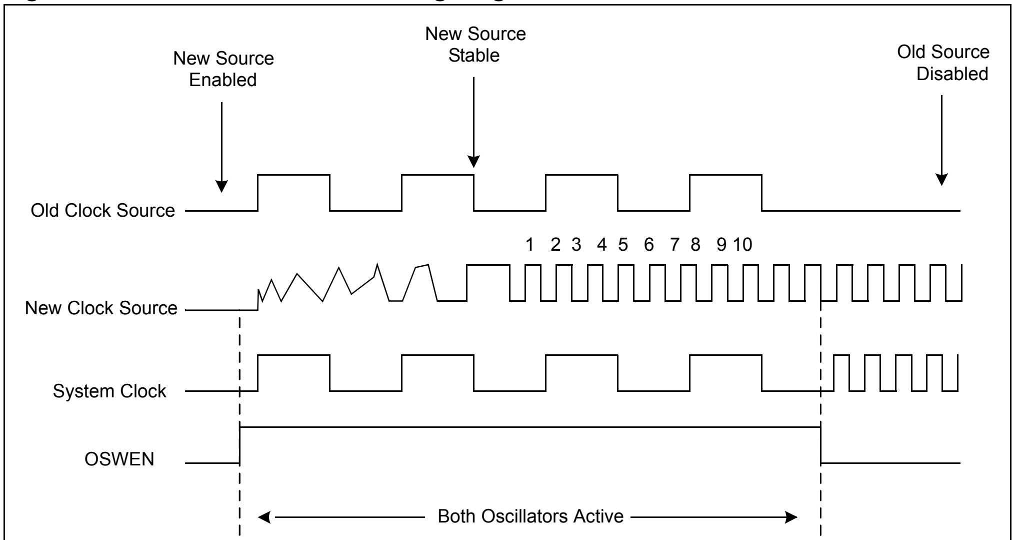
1. Read the COSC bits (OSCCON<14:12>) to determine the current oscillator source (if this information is relevant to the application).
2. Execute the unlock sequence that allows a write to the high byte of the OSCCON register.
3. Write the appropriate value to the NOSC control bits (OSCCON<10:8>) for the new oscillator source.
4. Execute the unlock sequence that allows a write to the low byte of the OSCCON register.
5. Set the OSWEN bit (OSCCON<0>) to initiate the oscillator switch.

After the previous steps are completed, the clock switch logic performs the following steps:

1. The clock switching hardware compares the COSC<2:0> Status bits (OSCCON<14:12>) with the new value of the NOSC control bit (OSCCON<10:8>). If they are the same, the clock switch is a redundant operation. In this case, the OSWEN bit (OSCCON<0>) is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the PLL Lock (OSCCON<5>) and Clock Fail status bits (OSCCON<3>) are cleared.
3. The new oscillator is turned on by the hardware (if it is not currently running). If a crystal oscillator (POSC or SOSC) must be turned on, the hardware waits for TOSCD until the crystal starts oscillating and TOST expires. If the new source uses the PLL, the hardware waits until a PLL lock is detected (OSCCON<5> = `1`).
4. The hardware waits for the new clock source to stabilize and then performs the clock switch.
5. The hardware clears the OSWEN bit (OSCCON<0>) to indicate a successful clock transition. In addition, the NOSC bit (OSCCON<10:8>) values are transferred to the COSC<2:0> status bits (OSCCON<14:12>).
6. The old clock source is turned off at this time, with the exception of the LPRC Oscillator (if the WDT or FSCM are enabled) or the SOSC (if the SOSCEN bit remains set). The timing of the transition between clock sources is illustrated in Figure 42-9.

> **Note 1:** Clock switching between XT, HS and EC Primary Oscillator modes is not possible without reprogramming the device.
>
> **2:** Direct clock switching between PLL modes is not possible. For example, clock switching should not occur between the POSC with PLL and Internal FRC Oscillator with PLL.
>
> **3:** Setting the CLKLOCK bit (OSCCON<7>) prevents clock switching when clock switching is enabled and fail-safe clock monitoring is disabled by the FCKSM Configuration bits (FOSC<7:6> = `01`). The OSCCON<7> bit cannot be cleared when it has been set by the user-assigned software. It clears on a POR.
>
> **4:** The processor continues to execute code throughout the clock switching sequence. Timing sensitive code should not be executed during this time.

Figure 42-9: Clock Transition Timing Diagram



Note: The system clock can be any selected source – Primary, Secondary, FRC, or LPRC.

The recommended code sequences for a clock switch are as follows:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte, in two back-to-back instructions:
   - Write 0x0078 to OSCCON<15:8>
   - Write 0x009A to OSCCON<15:8>
3. In the instruction immediately following the unlock sequence, write the new oscillator source to the NOSC control bits (OSCCON<10:8>).
4. Execute the unlock sequence for the OSCCON low byte in two, back-to-back instructions:
   - Write 0x0046 to OSCCON<7:0>
   - Write 0x0057 to OSCCON<7:0>
5. In the instruction immediately following the unlock sequence, set the OSWEN bit (OSCCON<0>).
6. Continue to execute code that is not clock-sensitive (optional).
7. Check to see if the OSWEN bit (OSCCON<0>) is '0'. If it is '0', the switch was successful.

Note: MPLAB® C Compiler for dsPIC® DSCs provides the following built-in C language functions for unlocking and writing to the OSCCON register:

```
__builtin_write_OSCCONH(value)
__builtin_write_OSCCONL(OSCCON | value)
```

For more information, refer to the MPLAB C Compiler Help.

Example 42-4 illustrates the code sequence for unlocking the OSCCON register and switching from FRC with PLL clock to the LPRC clock source.

Example 42-4: Code Example for Clock Switching

```
;Place the New Oscillator Selection (NOSC=0b101) in W0
MOV #0x5,WREG

;OSCCONH (high byte) Unlock Sequence
MOV     #OSCCONH, w1
MOV     #0x78, w2
MOV     #0x9A, w3
MOV.B   w2, [w1]    ; Write 0x0078
MOV.B   w3, [w1]    ; Write 0x009A

;Set New Oscillator Selection
MOV.B   WREG, OSCCONH

;OSCCONL (low byte) Unlock Sequence
MOV     #OSCCONL, w1
MOV     #0x46, w2
MOV     #0x57, w3
MOV.B   w2, [w1]    ; Write 0x0046
MOV.B   w3, [w1]    ; Write 0x0057

; Enable Clock Switch
BSET    OSCCON, #0  ; Request Clock Switching by Setting OSWEN bit
wait:
        btsc    OSCCONL,#OSWEN
        bra     wait
```


42.12.3 Clock Switching Consideration

When clock switching is incorporated into an application, consider these points when designing the code:

- The OSCCON unlock sequence is extremely timing critical. The OSCCON register byte is only writable for one instruction cycle following the sequence. Some high-level languages, such as C, may not preserve the timing-sensitive sequence of instructions when compiled. When clock switching is required for an application written in a high-level language, it is best to create the routine in assembler and link it to the application, and then calling it as a function when it is required.
- If the destination clock source is a crystal oscillator, the clock switch time will be dominated by the oscillator start-up time
- If the new clock source does not start, or is not present, clock switching hardware will continue to run from the current clock source. The user-assigned software can detect this situation because the OSWEN bit (OSCCON<0>) remains set indefinitely.
- If the new clock source uses the PLL, a clock switch will not occur until lock has been achieved. The user-assigned software can detect a loss of PLL lock because the LOCK bit (OSCCON<5>) is cleared and the OSWEN bit (OSCCON<0>) is set.
- Switching to a low-frequency clock source will result in slow device operation

42.12.4 Aborting a Clock Switch

If a clock switch does not complete, the clock switch logic can be reset by clearing the OSWEN bit (OSCCON<0>). When OSWEN is cleared, the clock switch process is aborted, the Oscillator Start-up Timer (if applicable) is stopped and reset, and the PLL (if applicable) is stopped.

Typical assembly code for aborting a clock switch is shown in Example 42-5. A clock switch procedure can be aborted at any time. A clock switch that is already in progress can also be aborted by performing a second clock switch.

Example 42-5: Aborting a Clock Switch

```
MOV     #OSCCON,W1     ; Pointer to OSCCON
MOV.b   #0x46,W2       ; First unlock code
MOV.b   #0x57,W3       ; second unlock code
MOV.b   W2, [W1]       ; Write first unlock code
MOV.b   W3, [W1]       ; Write second unlock code
BCLR    OSCCON,#OSWEN  ; ABORT the switch
```

42.12.5 Entering Sleep Mode During a Clock Switch

If the device enters Sleep mode during a clock switch operation, the clock switch operation is aborted. The processor keeps the old clock selection, and the OSWEN bit is cleared. The `PWRSAV` instruction is then executed normally.

It is particularly useful to perform a clock switch to the internal FRC oscillator before entering Sleep mode, as this will ensure fast wake-up from Sleep mode.

42.13 TWO-SPEED START-UP

The Internal External Start-up Option Configuration bit (IESO) in the Oscillator Source Selection register (FOSCSEL<7>) specifies whether to start the device with a user-selected oscillator source, or to initially start with the internal FRC and then automatically switch to the user-selected oscillator. If this bit is set to '1', the device will always power-up on the internal FRC oscillator, regardless of the other oscillator source settings (FOSCSEL<2:0>). The device then automatically switches to the specified oscillator, when it is ready.

Unless FSCM is enabled, the FRC oscillator is automatically turned off immediately after the clock switch is completed. The Two-Speed Start-up option is a faster way to get the device up and running and works independently of the state of the FCKSM<1:0> bits (FOSC<7:6>).

Two-Speed Start-up is useful when an external oscillator is selected by the FOSCSEL Configuration bits (FOSC<2:0) and a crystal-based oscillator has a longer start-up time.

As an internal RC oscillator, the FRC clock source is available immediately following a POR. With Two-Speed Start-up, the device starts executing code in its default oscillator configuration, FRC. The device continues to operate in this mode until the specified external oscillator source becomes stable, and at the same time it switches to that source.

The user software can check which clock source is currently providing the device clocking by checking the status of the COSC<2:0> bits (OSCCON<14:12>) against the NOSC<2:0> bits (OSCCON<10:8>). If these two sets of bits match, the clock switch has completed successfully and the device is running from the intended clock source.

Note: Two-Speed Start-up is redundant if the selected device clock source is FRC.

42.14 REFERENCE CLOCK OUTPUT

The reference clock output provides a clock signal to any remappable pin (RPn). The reference clock can be either the external oscillator or the system clock.

The ROSEL bit (REFOCON<12>) in the Reference Oscillator Control register selects between the external oscillator and the system clock. The RODIV<3:0> bits (REFOCON<11:8>) scale the reference clock to a desired clock output.

Figure 42-1 shows a block diagram for the reference clock. See the REFOCON register (Register 42-8) for the bits associated with the reference clock output. Refer to the specific device data sheet for more information on peripheral remapping.

42.15 REGISTER MAPS

Table 42-9 maps the bit functions for the Oscillator Special Function Control registers.

Table 42-10 maps the bit functions for the Oscillator Configuration registers.

Table 42-9: Oscillator Special Function Control Registers

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OSCCON	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	IOLOCK(2)	LOCK	—	CF	—	LPOSCEN	OSWEN	0000(1)
CLKDIV	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>					3040
PLLFBD	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
OSCTUN	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
REFOCON	ROON	—	ROSSLP	ROSEL	RODIV<3:0>				—	—	—	—	—	—	—	—	0000
ACLKCON	ENAPLL	APLLCK	SELACLK	—	—	APSTSCLR<2:0>			ASRCSEL	FRCSEL	—	—	—	—	—	—	0000
LFSR	—	LFSR<14:0>															0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The OSCCON register Reset values are dependent on the FOSCSEL Configuration bits and by the type of Reset.

2: The IOLOCK bit is not available on all dsPIC33F/PIC24H devices. Refer to the specific device data sheet for more information.

Table 42-10: Oscillator Configuration Registers

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
FOSCSEL	—	—	—	—	—	—	—	—	IESO	—	—	—	—	FNOSC<2:0>			xxxx(2)
FOSC	—	—	—	—	—	—	—	—	FCKSM<1:0>		IOL1WAY(1)	—	—	OSCIOFNC	POSCMD<1:0>		xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The IOL1WAY bit is not available on all dsPIC33F/PIC24H devices. Refer to the specific device data sheet for more information.

2: The configuration bits are programmed during device programming and it retains the programmed values on reset.

42.16 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H product families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Oscillator (Part IV) module are:

Title	**Application Note #**
PIC® Microcontroller Oscillator Design Guide	AN588
Low-Power Design using PIC® Microcontrollers	AN606
Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices	AN826

Note:	Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F/PIC24H families of devices.

42.17 REVISION HISTORY

Revision A (September 2007)

This is the initial released version of the document

Revision B (August 2008)

This revision incorporates the following updates:

- Figures:
  - Updated the label PLLCLK with FVCO(1) and added new labels in Figure 42-1
- Notes:
  - Added Note 1 to refer the FVCO values (see Figure 42-1).
  - Added a note for configuring the auxiliary clock (see **42.10.1 "Enabling the Auxiliary PLL"**)
  - Added a note on configuration bits in Oscillator Configuration Registers table (see Note 2 in Table 42-10).
- Registers:
  - Removed incorrect legend in FOSC: Oscillator Configuration Register (see Register 42-2) and CLKDIV: Clock Divisor Register (see Register 42-4).
  - Performed the following corrections in OSCCON: Oscillator Control Register (see Register 42-3):
    - Updated the incorrect Read/Write state for bit 9, bit 10, bit 12, bit 13 and bit 14.
    - Updated the incorrect bit description for COSC bit (bit 14-12) and NOSC bit (bit 10-8) as Reserved
    - Updated bit 1 and 2 as bit 2-1: Unimplemented: Read as '0'
  - The tuned frequencies for bit 5-0 in the OSCTUN: FRC Oscillator Tuning Register have been corrected (see Register 42-6).
  - Performed the following updates in ACLKCON: Auxiliary Clock Control Register (see Register 42-7):
    - Updated the bit descriptions for bit 6 and bit 7
    - Updated the values of the bit field for bit 10-8
    - Updated the term PLL as Fvco in bit 13
- Sections:
  - All references to the Secondary Oscillator have been removed
  - Updated the last sentence in bullet 3 under the clock switch logic section as "If the primary oscillator must be turned on, the hardware waits until a PLL lock is detected (OSCCON<5> = 1)" in **42.12.2 "Clock Switch Sequence"**
- Tables:
  - The All Resets column has been added in the Oscillator Configuration Registers table (see Table 42-10)
- Additional minor corrections such as language and formatting updates are incorporated throughout the document

Revision C (December 2009)

This revision incorporates the following content updates:

- Added a note with information to customers for utilizing family reference manual sections and data sheets as a joint reference (see note above **42.1 “Introduction”**).
- Changed all occurrences of OSCI to OSC1 and OSCO to OSC2
- Added information on the Secondary Oscillator to the following locations in their order of appearance:
  - Updated the logic in Figure 42-1 and added Note 3
  - Second bullet list item in **42.2 “CPU Clocking”**
  - Added S4 oscillator source and Note 3 to Table 42-1
  - Updated FNOSC<2:0> = `100` from “Reserved” to “Secondary Oscillator (SOSC)” and added Note 1 to Register 42-1
  - Updated COSC<2:0> = `100` and NOSC<2:0> = `100` from “Reserved” to “Secondary Oscillator (SOSC)” and added Note 2 to Register 42-3
  - Updated the second paragraph of **42.5.1 “Oscillator Start-up Time”**
  - Added **42.8 “Secondary Oscillator (Sosc)”**
  - Updated the second paragraph of **42.11.1 “FSCM Delay”**
  - Updated the third paragraph of **42.12 “Clock Switching”**
  - Updated Step 3 and Step 6 of the second procedure in **42.12.2 “Clock Switch Sequence”**
  - Updated the Note in Figure 42-9
- Registers:
  - Added Note 1 to OSCCON: Oscillator Control Register (Register 42-3)
  - Added Note 2 to CLKDIV: Clock Divisor Register (Register 42-4)
  - Added Note 1 to REFOCON: Reference Oscillator Control Register (Register 42-8)
  - Updated the SELACLK bit description for value ‘`0`’ (see Register 42-7)
- Figures:
  - Updated Figure 42-1
  - Updated Figure 42-3
- Added Note 2 regarding FRC Oscillator Tuning (TUN<5:0>) bits to Internal FRC Oscillator section (**42.6 “Internal FRC Oscillator”**)
- Added Note 2 in the shaded note box in **42.10.1 “Enabling the Auxiliary PLL”**
- Updated code examples (Example 42-1, Example 42-2 and Example 42-4)
- Additional minor corrections such as language and formatting updates have been incorporated throughout the document

Revision D (May 2011)

This revision incorporates the following updates:

- Figures:
  - Updated Figure 42-1
- Notes:
  - Updated the device name “dsPIC33F” to “dsPIC33F/PIC24H” devices in the Note that provides information to customers for utilizing family reference manuals and data sheets as a joint reference (see Note above **42.1 “Introduction”**)
  - Added Note 4 in Figure 42-1
  - Added Note 4 in Table 42-1
  - Updated the following in Register 42-3
    - Added Note 3 and Note 4
    - Added note reference to bit 10-8
  - Added Note 3 in Register 42-4
  - Added Note 1 in Register 42-5
  - Added Note 1 in Register 42-6
  - Added Note 1 in Register 42-7
  - Added Note 2 in **42.10.1 “Enabling the Auxiliary PLL”**
  - Updated the electrical specification range in Note 3, in **42.10.1 “Enabling the Auxiliary PLL”**
- Registers:
  - Updated the bit value and bit description for bit 0, bit 1 and bit 2 in Register 42-3
  - Added Register 42-9
- Sections
  - Added the following in the list of characteristics, in **42.1 “Introduction”**: Pseudo-random generator to trim the Fast RC (FRC) Oscillator
  - Added LFSR: Linear Feedback Shift Register, to the list of Special Function Registers (SFRs) in **42.4 “Special Function Registers (SFRs)”**
  - Updated the input frequency range for Posc in XT mode, in **42.7.1 “Input Clock Limitation at Start-up for PLL Mode”**
  - Added **42.10.3 “Linear Feedback Shift Register (LFSR)”**
- Tables:
  - Updated Table 42-9
- Added PIC24H to the document name in the running header
- Changes to formatting and text were incorporated throughout the document

Revision E (April 2012)

This revision includes the following updates:

- Added Note 5 to the Oscillator System Block Diagram (see Figure 42-1)
- Updated Note 2 in the Clock Pin Function Selection (see Table 42-3)
- Updated the dsPIC33F/PIC24H PLL Block Diagram (see Figure 42-8)
- Updated **42.10.2 “Auxiliary Clock Divider”**
- Minor updates to text and formatting were incorporated throughout the document

Note the following details of the code protection feature on Microchip devices:

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