Section 15. Quadratrure Encoder Interface (QEI)

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.

Please consult the note at the beginning of the **"Quadrature Encoder Interface (QEI)"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

15.1 INTRODUCTION

The Quadrature Encoder Interface (QEI) module provides the interface to incremental encoders for obtaining mechanical position data. Quadrature encoders, also known as incremental encoders or optical encoders, detect position and speed of rotating motion systems. Quadrature encoders enable closed loop control of motor control applications, such as Switched Reluctance (SR) motor and AC Induction Motor (ACIM).

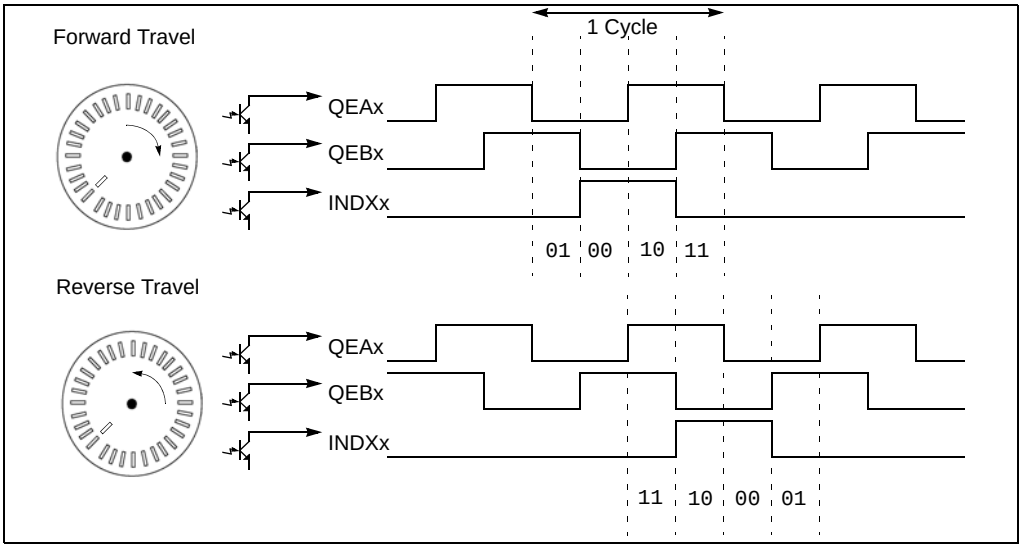
A typical quadrature encoder includes a slotted wheel attached to the shaft of the motor and an emitter/detector module that senses the slots in the wheel. Typically, three output channels, Phase A (QEAx), Phase B (QEBx) and Index (INDXx), provide information on the movement of the motor shaft, including distance and direction.

The Phase A and Phase B channels have a unique relationship. If Phase A leads Phase B, the direction of the motor is deemed positive or forward. If Phase A lags Phase B, the direction of the motor is deemed negative or reverse. The Index pulse occurs once per mechanical revolution and is used as a reference to indicate an absolute position. Figure 15-1 illustrates a relative timing diagram of these three signals.

The quadrature signals produced by the encoder can have unique states (`01`, `00`, `10` and `11`) that reflect the relationship between QEAx and QEBx. Figure 15-1 illustrates these states for one count cycle. The order of the states is reverse when the direction of travel changes.

The quadrature decoder increments or decrements the 16-bit Up/Down Counter (POSxCNT) for each change of state. The counter increments when QEAx leads QEBx and decrements when QEBx leads QEAx.

Figure 15-1: Quadrature Encoder Interface Signals



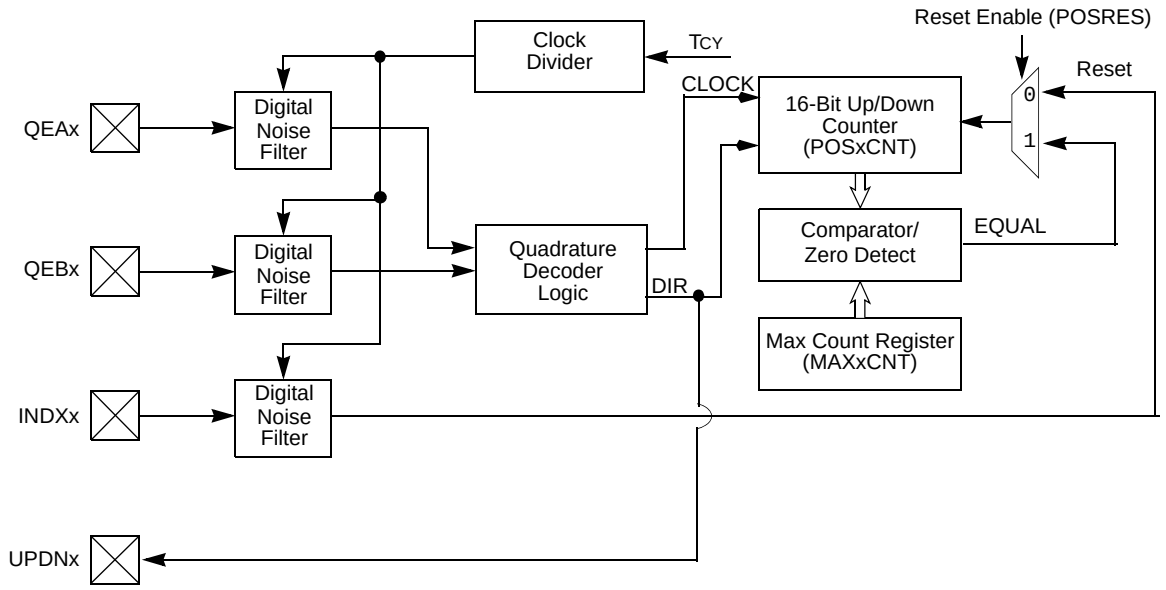
Note: dsPIC33F/PIC24H devices can have one or more QEI modules. An 'x' used in the names of pins, control/status bits and registers, denotes the particular QEI module number (x = 1 to 2). Refer to the **"Quadrature Encoder Interface (QEI)"** chapter in the specific device data sheet for more information.

The QEI consists of decoder logic to interpret the QEAx and QEBx signals, and an up/down counter to accumulate the count. Digital noise filter filters the inputs signals. Figure 15-2 illustrates a simplified block diagram of the QEI module.

The QEI module includes:

- Three input pins for two phase signals and index pulse
- Programmable digital noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- 16-bit up/down Position Counter (PC) (POSxCNT)
- Count direction status
- x2 and x4 count resolution
- Two modes of position counter reset:
  - Maximum Count (MAXxCNT) to reset the position counter
  - INDXx pulse to reset the position counter
- General purpose 16-bit Timer/Counter mode
- Interrupts generated by QEI or counter events

Figure 15-2: Quadrature Encoder Interface Module Simplified Block Diagram



Note: Index pulse reset is possible only if QEIM<2:0> = 100 or 110.

15.2 CONTROL AND STATUS REGISTERS

The QEI module has the following four user accessible registers. Figure 15-3 illustrates the registers that are accessible either in Byte mode or Word mode.

- **QEIxCON: QEI Control Register**

  This register controls the QEI operation and provides status flags for the state of the QEI module.

- **DFLTxCON: Digital Filter Control Register**

  This register controls the digital input filter operation.

- **Position Count Register (POSxCNT)**

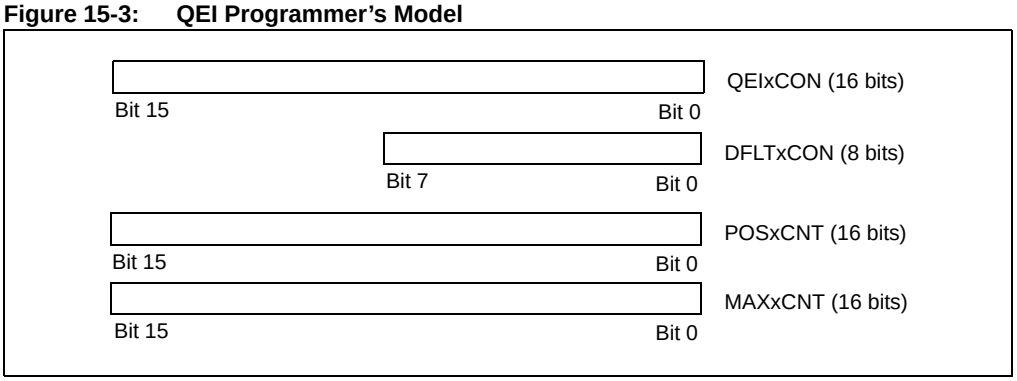
  This register allows reading and writing of the 16-bit position counter.

- **Maximum Count Register (MAXxCNT)**

  This register holds a value that is compared to the POSxCNT counter in some operations.

Note:	The POSxCNT register allows byte access; however, reading the register in Byte mode can result in partially updated values in subsequent reads. Either use Word mode reads/writes or ensure that the counter is not counting during byte operations.

Figure 15-3: QEI Programmer's Model



The QEIxCON (Register 15-1) and DFLTxCON (Register 15-2) registers define the QEI module control and digital filter control.

Register 15-1: QEIxCON: QEI Control Register

R/W-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
CNTERR	—	QEISIDL	INDEX	UPDN	QEIM<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SWPAB	PCDOUT	TQGATE(1)	TQCKPS<1:0>(1)		POSRES	TQCS(1)	UDSRC(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CNTERR:** Count Error Status Flag bit
1 = Position count error has occurred
0 = Position count error has not occurred
(CNTERR flag applies only when QEIM<2:0> = 110 or 100)

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **INDEX:** Index Pin State Status bit (read-only)
1 = Index pin is high
0 = Index pin is low

bit 11 **UPDN:** Position Counter Direction Status bit
1 = Position counter direction is positive (+)
0 = Position counter direction is negative (-)
(Read-only bit when QEIM<2:0> = 1xx)
(Read/Write bit when QEIM<2:0> = 001)

bit 10-8 **QEIM<2:0>:** Quadrature Encoder Interface Mode Select bits
111 = Quadrature Encoder Interface enabled (x4 mode) with position counter reset by match (MAXxCNT)
110 = Quadrature Encoder Interface enabled (x4 mode) with index pulse reset of position counter
101 = Quadrature Encoder Interface enabled (x2 mode) with position counter reset by match (MAXxCNT)
100 = Quadrature Encoder Interface enabled (x2 mode) with index pulse reset of position counter
011 = Unused (module disabled)
010 = Unused (module disabled)
001 = Starts 16-bit Timer
000 = Quadrature Encoder Interface/Timer off

bit 7 **SWPAB:** Phase A and Phase B Input Swap Select bit
1 = Phase A and Phase B inputs are swapped
0 = Phase A and Phase B inputs are not swapped

bit 6 **PCDOUT:** Position Counter Direction State Output Enable bit
1 = Position counter direction status output is enabled (QEI logic controls state of I/O pin)
0 = Position counter direction status output is disabled (normal I/O pin operation)

bit 5 **TQGATE:** Timer Gated Time Accumulation Enable bit(1)
1 = Timer gated time accumulation is enabled
0 = Timer gated time accumulation is disabled

Note 1: When configured for QEI mode, the TQGATE, TQCKPS, TQCS and UDSRC bits are ignored.

Register 15-1: QEIxCON: QEI Control Register (Continued)

bit 4-3 **TQCKPS<1:0>:** Timer Input Clock Prescale Select bits(1)
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 2 **POSRES:** Position Counter Reset Enable bit
1 = Index pulse resets position counter
0 = Index pulse does not reset position counter
(Bit only applies when QEIM<2:0> = 100 or 110)

bit 1 **TQCS:** Timer Clock Source Select bit(1)
1 = External clock from pin QEAx (on the rising edge)
0 = Internal clock (TCY)

bit 0 **UDSRC:** Position Counter Direction Selection Control bit(1)
1 = QEBx pin state defines position counter direction
0 = Control/Status bit, UPDN (QEIxCON<11>), defines timer counter (POSxCNT) direction

Note 1: When configured for QEI mode, the TQGATE, TQCKPS, TQCS and UDSRC bits are ignored.

Register 15-2: DFLTxCON: Digital Filter Control Register

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IMV<1:0>		CEID
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0
QEOUT	QECK<2:0>	—	—	—	—
bit 7					bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 **IMV<1:0>:** Index Match Value bits

These bits allow user-assigned applications to specify the state of the QEAx and QEBx input pins during an index pulse when the POSxCNT register is to be reset.
In x4 Quadrature Count Mode:
IMV1 = Required State of Phase B input signal for match on index pulse
IMV0 = Required State of Phase A input signal for match on index pulse
In x2 Quadrature Count Mode:
IMV1 = Selects phase input signal for index state match (Phase A = 0, Phase B = 1)
IMV0= Required state of the selected phase input signal for match on index pulse

bit 8 **CEID:** Count Error Interrupt Disable bit

1 = Interrupts due to count errors are disabled
0 = Interrupts due to count errors are enabled

bit 7 **QEOUT:** Digital Filter Output Enable bit

1 = Digital filter outputs are enabled on QEAx/QEBx/INDXx pins
0 = Digital filter outputs are disabled (normal pin operation)

bit 6-4 **QECK<2:0>:** Digital Filter Clock Divide Select bits

111 = 1:256 Clock divide for QEAx/QEBx/INDXx
110 = 1:128 Clock divide for QEAx/QEBx/INDXx
101 = 1:64 Clock divide for QEAx/QEBx/INDXx
100 = 1:32 Clock divide for QEAx/QEBx/INDXx
011 = 1:16 Clock divide for QEAx/QEBx/INDXx
010 = 1:4 Clock divide for QEAx/QEBx/INDXx
001 = 1:2 Clock divide for QEAx/QEBx/INDXx
000 = 1:1 Clock divide for QEAx/QEBx/INDXx

bit 3-0 **Unimplemented:** Read as '0'

15.3 PROGRAMMABLE DIGITAL NOISE FILTERS

The QEI module uses digital noise filters to reject noise on the incoming index pulse and quadrature phase signals. These filters reject low-level noise, large duration and short duration noise spikes that typically occur in motor systems.

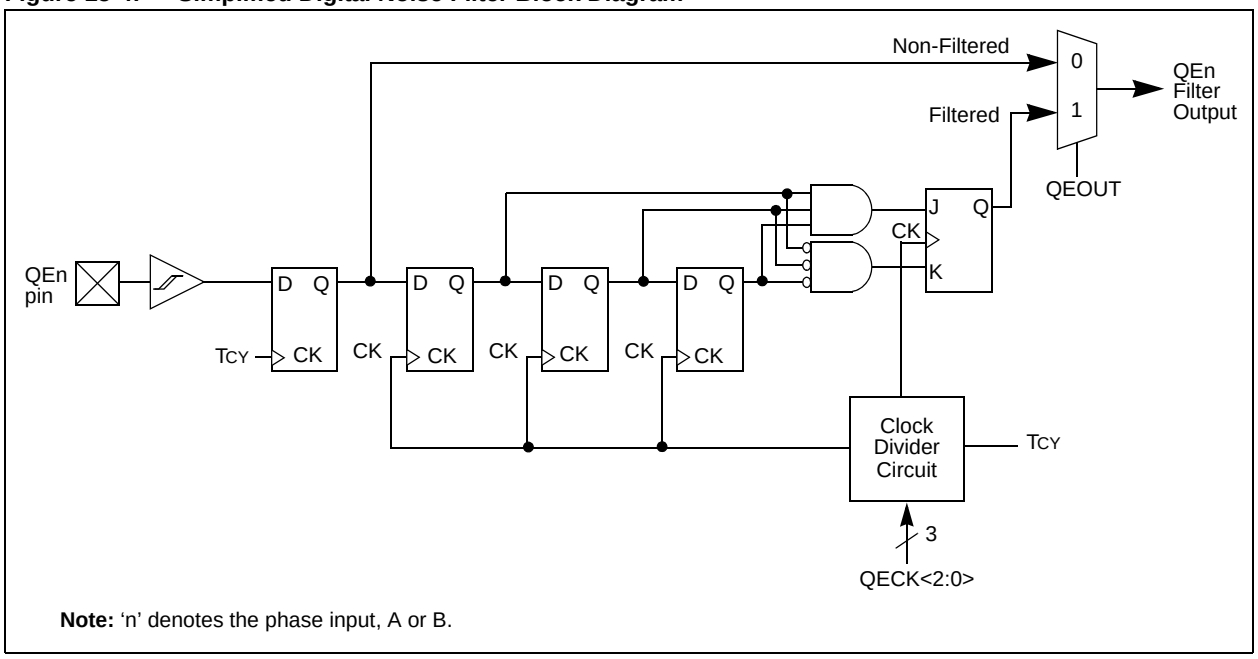
The filtered output signals can change only after an input level has the same value for three consecutive rising clock edges. The result is that short duration noise spikes between rising clock edges are ignored, and pulses shorter than two clock periods are rejected.

The rate of the filter clocks determine the low passband of the filter. A slower filter clock results in a passband rejecting lower frequencies. The filter clock is the device FCY clock divided by a programmable divisor.

Setting the Digital Filter Output Enable bit (QEOUT) in the Digital Signal Control register (DFLTxCON<7>), enables the filter for QEAx, QEBx, and INDXx inputs. The Digital Filter Clock Divide Select bits, QECK<2:0> (DFLTxCON<6:4>), specify the filter clock divisor used for the QEAx, QEBx and INDXx channels.

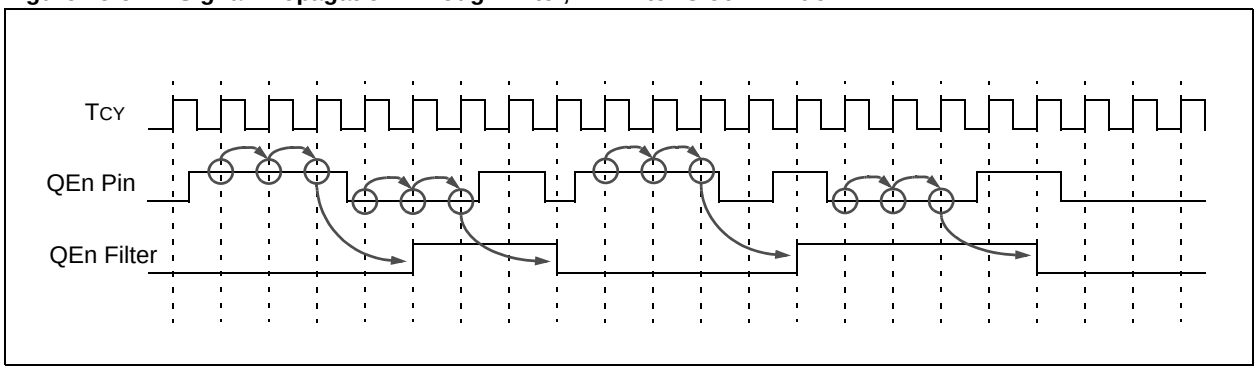
Figure 15-4 illustrates a simplified block diagram of the digital noise filter. Figure 15-5 illustrates the relationship between the incoming signal and the filtered output signal, where three consecutive clock pulses validate the input signal value.

Figure 15-4: Simplified Digital Noise Filter Block Diagram



Note: 'n' denotes the phase input, A or B.

Figure 15-5: Signal Propagation Through Filter, 1:1 Filter Clock Divide



15.4 QUADRATURE DECODER

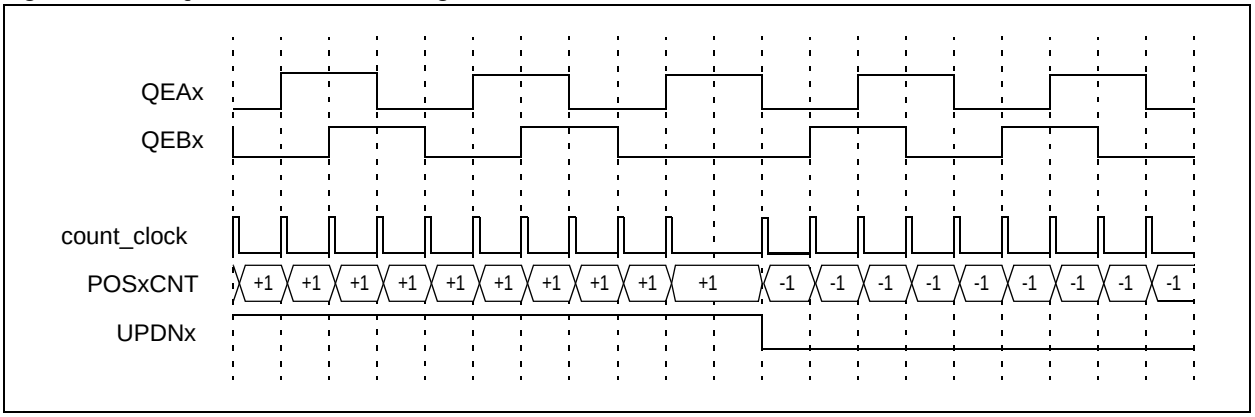
The quadrature decoder converts the incoming filtered signals into count information. The QEI circuitry multiplies the resolution of the input signals by a factor of two or four (x2 or x4 decoding).

The position measurement modes are selected when Quadrature Encoder Interface Mode Select bits, (QEIM<2:0>) (QEIxCON<10:8>), are set as QEIM<2:0> = 1xx.

When QEIM<2:0> = 1xx, the x4 measurement mode is selected, and the QEI logic clocks the PC on both edges of the Phase A and Phase B input signals.

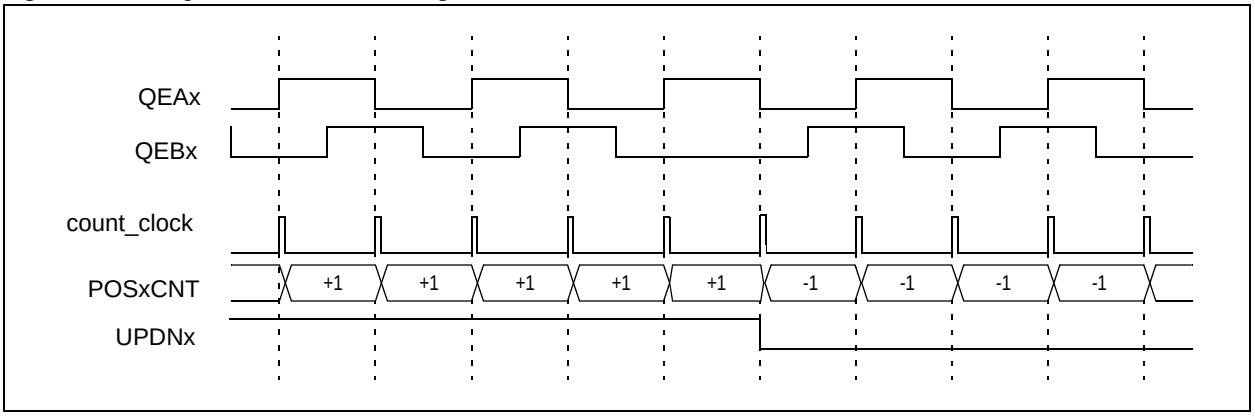
Figure 15-6 illustrates the x4 measurement mode that provides finer resolution data (more position counts) to determine the encoder position.

Figure 15-6: Quadrature Decoder Signals in x4 Mode



When QEIM<2:0> = 10x, the x2 measurement mode is selected and the QEI logic looks only at the rising and falling edge of the Phase A input for the PC increment rate. Figure 15-7 illustrates how every rising and falling edge of the Phase A signal causes the PC to increment or decrement. The Phase B signal is still used to determine the counter direction like the x4 measurement mode.

Figure 15-7: Quadrature Decoder Signals in x2 Mode



15.4.1 Explanation of Lead/Lag Test

The lead/lag test is performed by the QEI logic to determine the phase relationship of the QEAx and QEBx signals, and whether to increment or decrement the Position Count register (POSxCNT). Table 15-1 provides the lead/lag test details.

Table 15-1: Lead/Lag Test Description

Present Transition	Previous Transition	Condition	Action	
QEAx↑	QEB↓	QEAx leads QEBx channel	Set UPDNx	Increment POSCNT
	QEBx↑	QEAx lags QEBx channel	Clear UPDNx	Decrement POSCNT
	QEAx↓	Direction change	Toggle UPDNx	Increment or decrement POSCNT
QEAx↓	QEB↓	QEAx lags QEBx channel	Clear UPDNx	Decrement POSCNT
	QEBx↑	QEAx leads QEBx channel	Set UPDNx	Increment POSCNT
	QEAx↑	Direction change	Toggle UPDNx	Increment or decrement POSCNT
QEBx↑	QEAx↓	QEAx lags QEBx channel	Clear UPDNx	Decrement POSCNT
	QEAx↑	QEAx leads QEBx channel	Set UPDNx	Increment POSCNT
	QEB↓	Direction Change	Toggle UPDNx	Increment or decrement POSCNT
QEB↓	QEAx↓	QEAx leads QEBx channel	Set UPDNx	Increment POSCNT
	QEAx↑	QEAx lags QEBx channel	Clear UPDNx	Decrement POSCNT
	QEBx↑	Direction change	Toggle UPDNx	Increment or decrement POSCNT

15.4.2 Count Direction Status

As previously mentioned, the QEI logic generates an UPDNx signal based on the Phase A and Phase B time relationship. The UPDNx signal can be routed to an I/O pin. Setting the Position Counter Direction State Output Enable bit (PCDOUT) in the QEI Control register (QEIxCON<6>), and clearing the appropriate TRIS bit associated with the pin causes the UPDNx signal to drive the output pin. In addition to the output pin, the state of this internal UPDNx signal is supplied to the Special Function Register (SFR) bit (QEIxCON<11>) as a read-only bit, UPDNx.

15.4.3 Encoder Count Direction

The direction of quadrature counting is determined by the Phase A and Phase B Input Swap Select bit, SWPAB (QEIxCON<7>). If SWPAB = 0, the Phase A input is fed to the A input of the quadrature counter, and the Phase B input is fed to the B input of the quadrature counter. Therefore, as the Phase A signal leads the Phase B signal, the quadrature counter is incremented on each edge. This condition Phase A (QEAx) signal leads the Phase B (QEBx) signal is defined as the forward direction of motion.

Setting the SWPAB bit (QEIxCON<7>) to a logic ‘1’ causes the Phase A input to be fed to the B input of the quadrature counter, and the Phase B signal to be fed to the A input of the quadrature counter. Therefore, if the Phase A signal leads the Phase B signal at the dsPIC33F/PIC24H device pins, the Phase A input to the quadrature counter lags the Phase B input. This condition is recognized as rotation in the reverse direction, and the counter is decremented on each quadrature pulse.

15.4.4 Quadrature Rate

The revolutions per minute (RPM) of the position control system can vary. The RPM along with the quadrature encoder line count determines the frequency of the QEAx and QEBx input signals. The quadrature encoder signals can be decoded such that a count pulse is generated for every quadrature signal edge. This allows an angular position measurement resolution of up to four times the encoder line count.

For example, a 6,000 RPM motor, utilizing a 4096 resolution encoder, yields a quadrature count rate of: ((6000/60) * (4096 * 4)) = 1.6384 MHz. Similarly, a 10,000 RPM motor, utilizing a 8192 resolution encoder, yields a quadrature count rate of: [(10000/60) * (8192 * 4)] = 5.46 MHz.

For the maximum clock frequency at the QEAx and QEBx pins, refer to the **"Electrical Characteristics"** chapter in the specific device data sheet.

15.5 16-BIT UP/DOWN POSITION COUNTER (PC)

The 16-bit Up/Down PC (POSxCNT) counts up or down on every count pulse generated by the QEI logic. The counter acts as an integrator and its count value is proportional to the position. The direction of the count is determined by the quadrature decoder.

The user software can examine the contents of the count by reading the POSxCNT register. The user software can also write to the POSxCNT register to initialize a count. Changing the QEIM<2:0> bits (QEIxCON<10:8>) does not affect the POSxCNT register contents.

15.5.1 Using the Position Counter

Position Counter data can be used in several ways. In some systems, the position count is accumulated consistently and taken as an absolute value representing the total position of the system.

For example, a quadrature encoder is affixed to a motor that is controlling the print head in a printer. In operation, the system is initialized by moving the print head to the maximum left position and resetting the POSxCNT register. As the print head moves to the right, the quadrature encoder begins to accumulate counts in the POSxCNT register. As the print head moves to the left, the accumulated count decreases. As the print head reaches the right-most position, the maximum position count should be reached. If the maximum count is less than 2^{16}, the QEI module can encode the entire range of motion. However, if, the maximum count is more than 2^{16}, the user software must capture the additional count precision. Generally, to accomplish this, the module is set to a mode where it resets the counter when the count reaches a specified maximum value.

Setting the QEIM<2:0> bits (QEIxCON<10:8>) to '1x1' enables 16-bit mode where the Maximum Count register (MAXCNT) is used to reset the PC. The count is reset, when the counter reaches a predetermined maximum count while incrementing or the count reaches zero while decrementing. An interrupt is generated to allow the user software to increment or decrement a software counter containing the Most Significant bits (MSbs) of the position count. The maximum count can be 0xFFFF to enable a full range of the QEI counter and software counter, or some smaller value of significance, like the number of counts for one encoder revolution.

Setting the QEIM<2:0> bits (QEIxCON<10:8>) to '1x0' enables a mode used in other systems in which the position count can be cyclic. The position count references the position of the wheel within the number of rotations determined by the index pulse. For example, a tool platform moved by a screw rod, uses a quadrature encoder attached to the screw rod. In operation, the screw might require five and a half rotations to achieve the desired position. The user software detects five index pulses to count the full rotations and uses the position count to measure the remaining half rotation. In this method, the index pulse resets the PC to initialize the counter at each rotation and generates an interrupt for each rotation.

15.5.2 Using MAXCNT to Reset the Position Counter

When the QEIM<2:0> bits (QEIxCON<10:8>) = 1x1, the PC resets on a match of the position count with predetermined high values and low values. The index pulse Reset mechanism is not used.

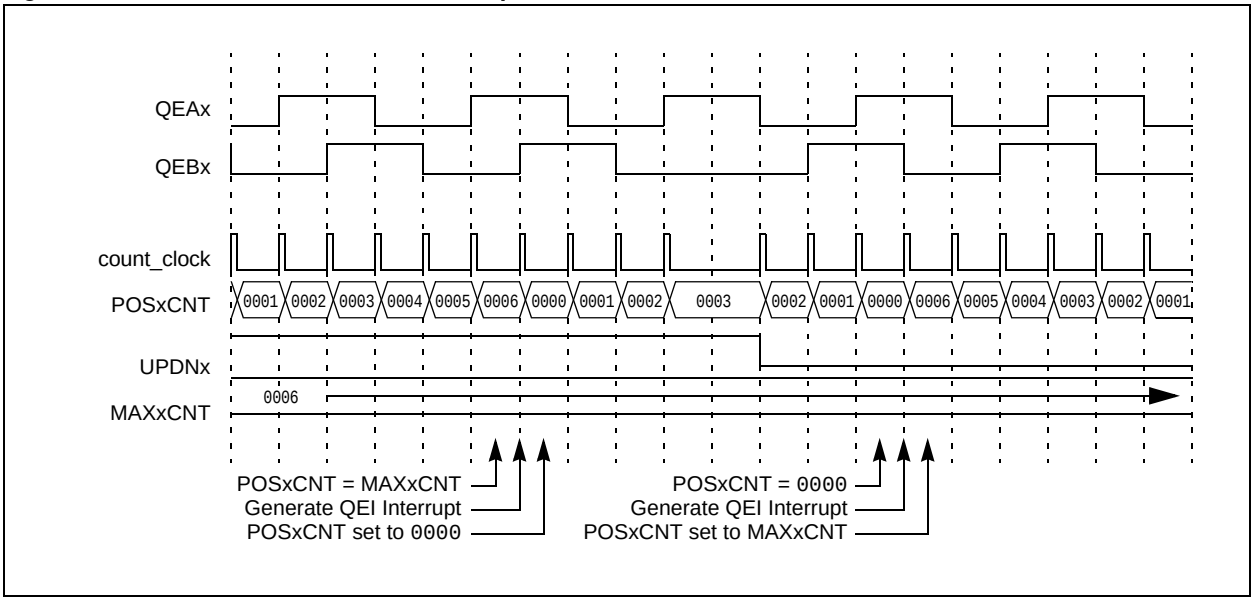
For this mode, the PC Reset mechanism operates as follows (for related timing details, see Figure 15-8):

- If the encoder is travelling in the forward direction (QEAx leads QEBx), and the value in the POSxCNT register matches the value in the MAXxCNT register, POSxCNT resets to '0' on the next occurring quadrature pulse edge that increments POSxCNT. An interrupt event is generated on this rollover event.
- If the encoder is travelling in the reverse direction (QEBx leads QEAx), and the value in the POSxCNT register counts down to '0', the POSxCNT register is loaded with the value in the MAXxCNT register on the next occurring quadrature pulse edge that decrements POSxCNT. An interrupt event is generated on this underflow event.

When using MAXxCNT as a position limit, the PC counts at either x2 or x4 of the encoder counts. For standard rotary encoders, the appropriate value to write to MAXxCNT is 4N – 1 for x4 position mode, and 2N – 1 for x2 position mode, where N is the number of counts per revolution of the encoder.

For absolute position information, where the range of the system exceeds 2^{16}, it is also appropriate to load a value of 0xFFFF into the MAXxCNT register. The module generates an interrupt on rollover or underflow of the PC.

Figure 15-8: Roll over/Roll under Reset-Up/Down PC

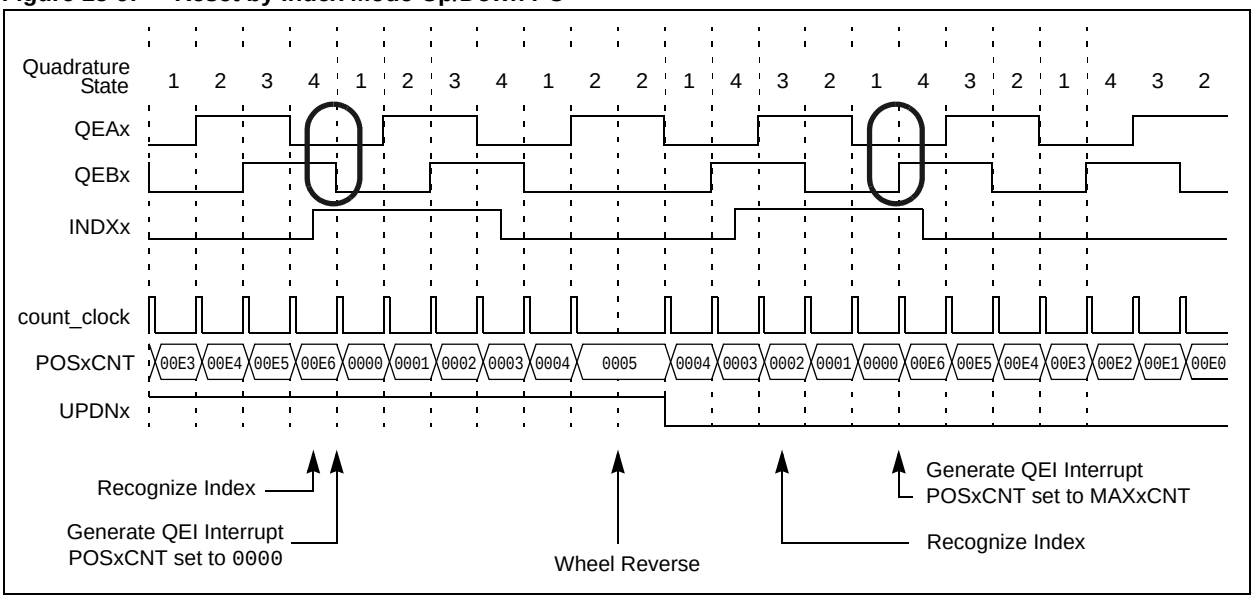


15.5.3 Using Index to Reset the Position Counter

When QEIM<2:0> = 1x0, the index pulse resets the position counter. For this mode, the position counter reset mechanism operates as follows (for related timing details, see Figure 15-9):

- The position count is reset, each time an index pulse is received on the INDXx pin
- If the encoder is travelling in the forward direction (QEAx leads QEBx), POSxCNT is reset to '0'
- If the encoder is travelling in the reverse direction (QEBx leads QEAx), the value in the MAXCNT register is loaded into POSxCNT

Figure 15-9: Reset by Index Mode-Up/Down PC



15.5.3.1 INDEX PULSE DETECTION CRITERIA

Incremental encoders from different manufacturers use differing timing for the index pulse. The index pulse can be aligned to any of the four quadrature states and can have a pulse width of a full cycle (four quadrature states), a half cycle (two quadrature states) or a quarter cycle (one quadrature state). Index pulses of a full cycle width or a half cycle width are normally termed "ungated" and index pulses of a quarter cycle width are normally termed "gated."

Regardless of the type of index pulse provided, the QEI maintains symmetry of the count as the wheel reverses direction. This means the index pulse must reset the position counter at the same relative quadrature state transition as the wheel rotates in the forward or reverse direction.

Figure 15-9 illustrates an example of how the first index pulse is recognized and resets POSxCNT as the quadrature state changes from 4 to 1. The QEI latches the state of this transition. Any subsequent index pulse detection uses state transition for the reset.

Figure 15-9 also demonstrates that as the wheel reverses, the index pulse again occurs; however, the reset of the PC cannot occur until the quadrature state changes from 1 to 4.

Note:	The QEI index logic ensures that the POSxCNT register is always adjusted at the same position relative to the index pulse, regardless of the direction of travel.

15.5.3.2 INDEX MATCH VALUE

The Index Match Value control bits, IMV<1:0> (DFLTxCON<10:9>), allow the user software to select the state of the QEAx and QEBx input pins during an index pulse when the POSxCNT register is to be reset (see Register 15-2).

15.5.3.3 INDEX PULSE STATUS

The Index Pin State Status bit, INDEX (QEIxCON<12>), provides the status of the logic state on the index pin. This status bit is useful in position control systems during the “homing” sequence, where the system searches for a reference position. The INDEX bit (QEIxCON<12>) indicates the status of the index pin after the bit is processed by the digital filter (if enabled).

15.5.3.4 USING THE INDEX PIN AND MAXCNT FOR ERROR CHECKING

When the counter operates in Reset on Index Pulse mode, the QEI also detects the POSxCNT register boundary conditions. This operation can detect system errors in the incremental encoder system.

For example, assume a wheel encoder has 100 lines. When used in x4 measurement mode and reset on the index pulse, the counter should count from 0 to 399 (0x018E) and reset. If the value of the POSxCNT register achieves 0xFFFF or 0x0190, a system error occurs.

The content of the POSxCNT register is compared with MAXxCNT + 1, if counting up, and compared with 0xFFFF, if counting down. If the QEI detects one of these values, a position count error condition can generate by setting the Count Error Status Flag bit, CNTERR (QEIxCON<15>), and optionally generating a QEI interrupt.

If the Counter Error Interrupt Disable control bit, CEID (DFLTxCON<8>), is cleared (by default), a QEI interrupt is generated when a position count error is detected. If the CEID control bit (DFLTxCON<8>) is set, an interrupt does not occur.

The PC continues to count encoder edges after detecting a position count error. No interrupt is generated for subsequent position count error events until the CNTERR bit (QEIxCON<15>) is cleared by the user software.

15.5.3.5 POSITION COUNTER RESET ENABLE (POSRES)

The Position Counter Reset Enable bit, POSRES (QEIxCON<2>), enables a reset of the position counter when the index pulse is detected. This bit applies only when the QEI module is configured by setting the QEIM<2:0> bits (QEIxCON<10:8>) to ‘100‘ or ‘110 ‘.

- If the POSRES bit (QEIxCON<2>) is set to ‘1’, the PC is reset when the index pulse is detected
- If the POSRES bit (QEIxCON<2>) is set to ‘0’, the PC is not reset when the index pulse is detected. The PC continues counting up or down and is reset on the rollover or underflow condition. The QEI continues to generate interrupts on the detection of the index pulse.

15.6 USING QEI AS AN ALTERNATE 16-BIT TIMER/COUNTER

When the QEI module is configured with QEIM<2:0> = 001, the QEI module is configured as a 16-bit timer/counter. Figure 15-10 illustrates the setup and control for the auxiliary timer that is accomplished through the QEIxCON register.

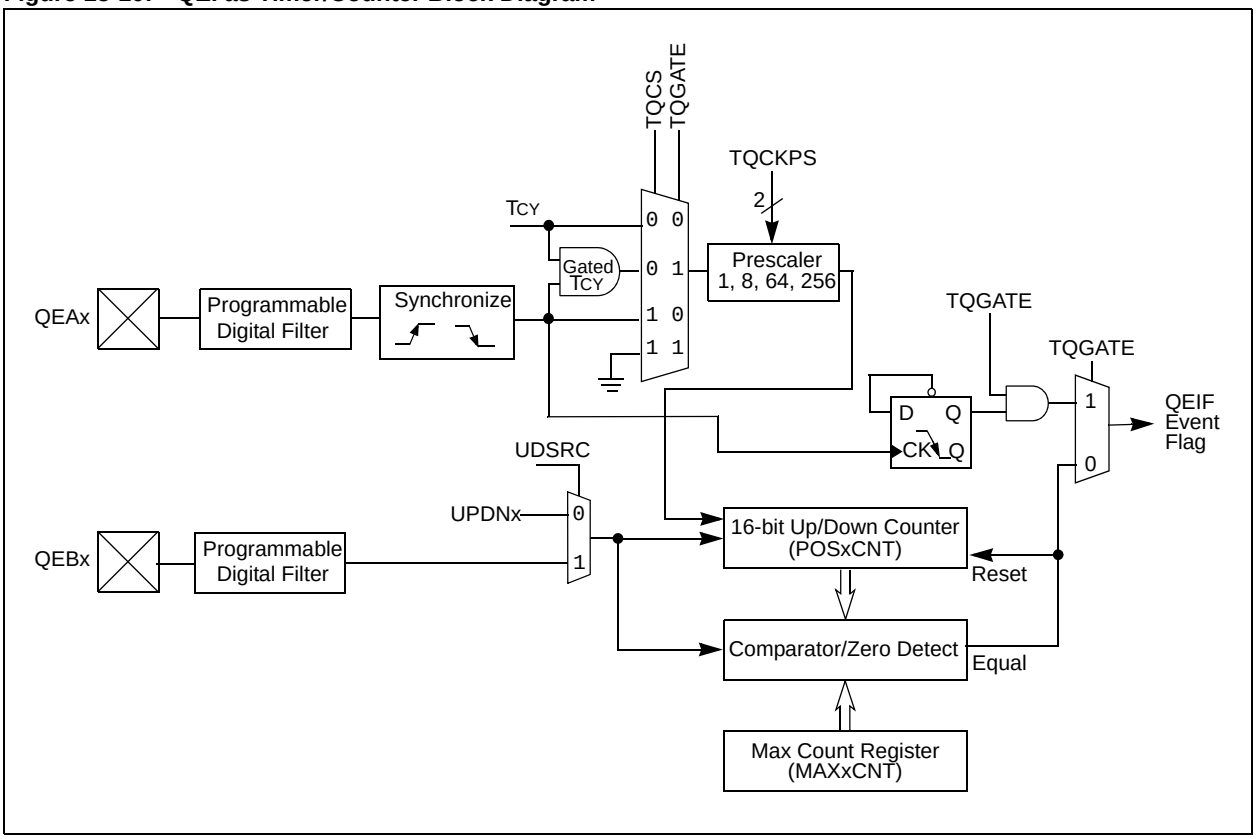
> **Note:** The digital filter is not active when the QEI is configured as a general purpose counter.

The QEI timer functions similar to the other dsPIC33F/PIC24H timers. For more information on timers, refer to **Section 11. "Timers"** (DS70205).

When configured as a timer, the POSxCNT register serves as a timer register similar to the TMRn registers of the General Purpose Timers (GPTs). The MAXxCNT register serves as a period register similar to the PRn registers of the GP timers. When a timer/period register match occurs, the QEIF flag is asserted.

> **Note:** Changing operational modes, for example, from QEI to Timer or Timer to QEI, does not affect the Timer/PC register contents.

Figure 15-10: QEI as Timer/Counter Block Diagram



15.6.1 Up/Down Timer Operation

Unlike most other timers, the QEI timer can increment or decrement.

- When the timer is configured to count up, the timer (POSxCNT) increments until the count matches the period register (MAXxCNT). The timer resets to zero and restarts incrementing.
- When the timer is configured to count down, the timer (POSxCNT) decrements until the count matches the period register (MAXxCNT). The timer resets to zero and restarts decrementing.

When the timer is configured to count down, the following two general operational guidelines must be followed for correct operation:

- The MAXxCNT register serves as the period match register, but the desired match value is derived from the starting count of 0xFFFF. For example, a timer count of 0x1000 is desired for a match condition.The period register must be loaded with 0xF000.
- On a match condition, the timer resets to zero

The Position Counter Direction Selection Control bit, UDSRC (QEIxCON<0>), determines what controls the timer count direction state. Either an I/O pin or a SFR control bit specifies the count direction control.

- When UDSRC = 1, the timer count direction is controlled from the QEBx pin. If the QEBx pin is 1, the count direction increments. If the QEBx pin is '0', the count direction decrements.
- When UDSRC = 0, the timer count direction is controlled from the UPDN bit (QEIxCON<11>). When UPDN = 1, the timer increments. When UPDN = 0, the timer decrements.

15.6.2 Timer Clock Source

The Timer Clock Source Select bit, TQCS (QEIxCON<1>), selects the internal or external clock. The QEI timer can use the QEAx pin as an external clock input when the TQCS bit (QEIxCON<1>) is set. The QEI timer does not support External Asynchronous Counter mode. If an external clock source is used, the clock is automatically synchronized to the internal instruction cycle (T_{CY}).

15.6.3 Timer Gate Operation

The QEAx pin functions as a timer gate when the Timer Gated Time Accumulation Enable bit, TQGATE (QEIxCON<5>), is set and the TQCS bit (QEIxCON<1>) is cleared.

If the TQCS bit (QEIxCON<1>) and the TQGATE bit (QEIxCON<5>) are concurrently set, the timer does not increment and generates an interrupt.

15.7 QEI INTERRUPTS

Depending on the operating mode, the QEI module generates interrupts for the following events:

- In Reset On Match mode (QEIM<2:0> = 111 and 101), an interrupt occurs on position counter rollover/underflow
- In Reset On Index mode (QEIM<2:0> = 110 and 100), an interrupt occurs on detection of index pulse and optionally when the CNTERR bit (QEIxCON<15>) is set
- When operating as a timer/counter (QEIM<2:0> = 001), an interrupt occurs on a period match event or a timer-gate falling-edge event when TQGATE = 1

When a QEI interrupt occurs, the QEI Interrupt Flag (QEIxIF) is set and it must be cleared in software.

A QEI interrupt is enabled as a source of interrupt through the respective QEI Interrupt Enable bit (QEIxIE) in the IECx register. The interrupt priority level bits (QEIxIP<2:0>) in the IPCx register must be written with a non zero value for the timer to be a source of interrupt. For more information, refer to **Section 6. "Interrupts"** (DS70184).

15.8 I/O PIN CONTROL

Enabling the QEI module causes the associated I/O pins to come under the control of the QEI and prevents lower priority I/O functions such as ports from affecting the I/O pin.

Table 15-2 and Table 15-3 describes how the I/O pins can assume differing functions depending on the mode specified by the QEIM<2:0> bits (QEIxCON<10:8>) and other control bits.

Table 15-2: Quadrature Encoder Module Pinout I/O Descriptions

Pin Name	Pin Type	Buffer Type	Description
QEAx	I I I	ST ST ST	Quadrature encoder Phase A input, or Auxiliary timer external clock input, or Auxiliary timer external gate input
QEBx	I I	ST ST	Quadrature encoder Phase B input, or Auxiliary timer up/down select input
INDXx	I	ST	Quadrature encoder index pulse input
UPDNx	O	—	Position up/down counter direction status, QEI mode

Legend: I = Input, O = Output, ST = Schmitt Trigger

Table 15-3: Module I/O Mode Functions

QEIM<2:0>	PCDOUT	UDSRC	TQGATE	TQCS	QEAx Pin	QEBx Pin	INDXx Pin	UPDNx Pin
000, 010, 011 Module off	N/A	N/A	N/A	N/A	—	—	—	—
001 Timer mode	N/A	0	0	0	—	—	—	—
		1	0	0	—	Input (QEBx)	—	—
		0	1	0	Input (TQGATE) port not disabled		—	—
		1	1	0	Input (TQGATE) port not disabled	Input (QEBx)	—	—
		0	N/A	1	Input (TQCKI) Port not disabled	—	—	—
		1	N/A	1	Input (TQCKI) port not disabled	Input (QEBx)	—	—
101, 111 QEI Reset by count	0	N/A	N/A	N/A	Input (QEAx)	Input (QEBx)	—	—
	1	N/A	N/A	N/A	Input (QEBx)	Input (QEBx)	—	Output (UPDNx)
100, 110 QEI Reset by index	0	N/A	N/A	N/A	Input (QEAx)	Input (QEBx)	Input (INDXx)	—
	1	N/A	N/A	N/A	Input (QEAx)	Input (QEBx)	Input (INDXx)	Output (UPDNx)

Legend: '—' indicates the pin is not used by the QEI module in this configuration. Instead, the pin is controlled by I/O port logic.

15.9 OPERATION DURING POWER-SAVING MODES

15.9.1 When the Device Enters Sleep Mode

When the device enters Sleep mode, QEI operations cease. The POSxCNT register stops at the current value. The QEI does not respond to active signals on the QEAx, QEBx, INDXx or UPDNx pins. The QEIxCON register remains unchanged.

If the QEI is configured as a timer/counter (QEIM<2:0> = 001), and the clock is provided externally (TQCS = 1), the QEI module ceases operation during Sleep mode.

When the QEI module wakes up, the quadrature decoder accepts the next transition on the QEAx or QEBx signals and compares that transition to the last transition before Sleep mode to determine the next action.

15.9.2 When the Device Enters Idle Mode

The QEI module can enter a power-saving state in Idle mode, depending on the Stop in Idle Mode bit, QEISIDL (QEIxCON<13>), setting.

- If QEICSIDL = 1, the QEI module enters the power-saving mode, with effects similar to entering Sleep mode
- If QEICSIDL = 0, the QEI module does not enter a power-saving mode. The QEI module continues to operate normally while the device is in Idle mode

15.10 EFFECTS OF A RESET

A Reset forces module registers to their initial Reset state. For all initialization and reset conditions for QEI module related registers, see QEIxCON register (Register 15-1). The quadrature decoder and the POSxCNT counter are reset to an initial state.

15.11 REGISTER MAP

Table 15-4 maps the bit functions for the SFRs associated with the Quadratrure Encoder Interface (QEI) module.

Table 15-4: Special Function Registers Associated with QEI

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QEIxCON	CNTERR	—	QEISIDL	INDEX	UPDN	QEIM<2:0>			SWPAB	PCDOUT	TQGATE	TQCKPS<1:0>		POSRES	TQCS	UDSRC	0000
DFLTxCON	—	—	—	—	—	IMV<1:0>		CEID	QEOUT	QECK<2:0>			—	—	—	—	xxxx
POSxCNT	Position Count Register																0000
MAXxCNT	Maximum Count Register																1111

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

15.12 DESIGN TIPS

Question 1: ***I have initialized the QEI, but the POSxCNT register does not seem to change when quadrature signals are applied to the QEAx/QEBx pins.***

Answer: On many devices, the QEI pins are multiplexed with analog input pins. Ensure that the QEI pins are configured as digital pins using the ADxPCFG control register.

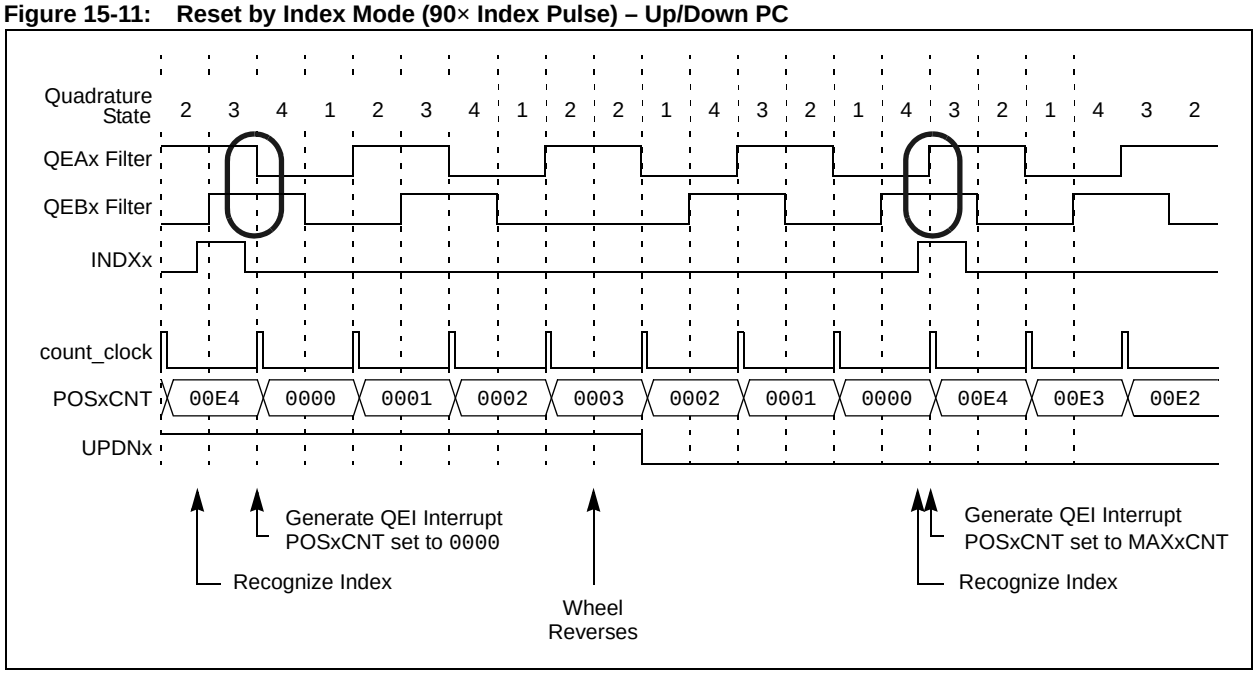
Question 2: ***How fast can my quadrature signals be?***

Answer: The answer depends on the setting of the filter parameters for the quadrature signals. For details, refer to the **"Electrical Characteristics"** chapter in the specific device data sheet.

Question 3: ***My encoder has a 90× Index Pulse and the count does not reset properly.***

Answer: Depending on how the count clock is generated, and which quadrature state transition is used for the index pulse, a quarter cycle index pulse may not be recognized before the required transition. To correct this, use a filter on the quadrature clocks that has a higher filter prescaler than that of the index pulse. This has the effect of delaying the quadrature clocks somewhat, allowing for proper detection of the index pulse.

Figure 15-11: Reset by Index Mode (90× Index Pulse) – Up/Down PC



15.13 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Quadratrure Encoder Interface (QEI) module are:

Title	Application Note #
Servo Control of a DC-Brush Motor	AN532
PIC18CXXX/PIC16CXXX DC Servomotor Application	AN696
Using the dsPIC30F for Vector Control of an ACIM	AN908

Note: For additional Application Notes and code examples for the dsPIC33F/PIC24H device family, visit the Microchip web site (www.microchip.com).

15.14 REVISION HISTORY

Revision A (May 2007)

This is the initial released version of the document

Revision B (March 2010)

This revision incorporates the following updates:

- Added a note on the QEI configured as a general purpose timer/counter, see **15.6 “Using QEI as an Alternate 16-bit Timer/Counter”**
- The Register Map table (Table 15-4) is updated as follows:
  - Added a Legend to the footer
  - Updated the All Resets values
  - Removed references to Interrupt registers
  - Renamed registers to QEIxCON, DFLTxCON, POSxCNT, and MAXxCNT and removed redundant entries
  - Removed the shaded note box
- Additional minor corrections such as language and formatting updates are incorporated throughout the document

Revision C (September 2012)

This revision incorporates the following updates:

- Sections:
  - Updated the following in **15.4 “Quadrature Decoder”**
    - Updated QEIM<2:0> = `001` to QEIM<2:0> = `1xx` in the second and third paragraphs
    - Updated QEIM<2:0> = `000` to QEIM<2:0> = `10x` in the fifth paragraph (above Figure 15-7)
  - Updated the following in **15.5.1 “Using the Position Counter”**:
    - Updated QEIM<2:0> bit to ‘`001`’ to QEIM<2:0> bit to ‘`1x1`’ in the third paragraph
    - Updated QEIM<2:0> bit to ‘`000`’ to QEIM<2:0> bit to ‘`1x0`’ in the third paragraph
  - Updated QEIM<2:0> bits = `001` to QEIM<2:0> bits = `1x1` in **15.5.2 “Using MAXCNT to Reset the Position Counter”**
  - Updated QEIM<2:0> bits = `000` to QEIM<2:0> bits = `1x0` in **15.5.3 “Using Index to Reset the Position Counter”**
- Minor updates to text and formatting were incorporated throughout the document

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