Section 13. Output Compare

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33E/PIC24E devices.

Please consult the note at the beginning of the **"Output Compare"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

13.1 INTRODUCTION

The output compare module in dsPIC33E/PIC24E devices compares the Timer register value with the value of one or two Compare registers, depending on its mode of operation. The output compare module on compare match events can generate a single output transition or a train of output pulses. Like most PIC® MCU peripherals, the output compare module can also generate interrupts on a compare match event.

Each output compare timer can use one of the available six selectable time clocks. The clock is selected using the OCTSEL<2:0> (OCxCON1<12:10>) bits. Refer to the applicable device data sheet for more information about specific timers that can be used as a time base for the output compare timer.

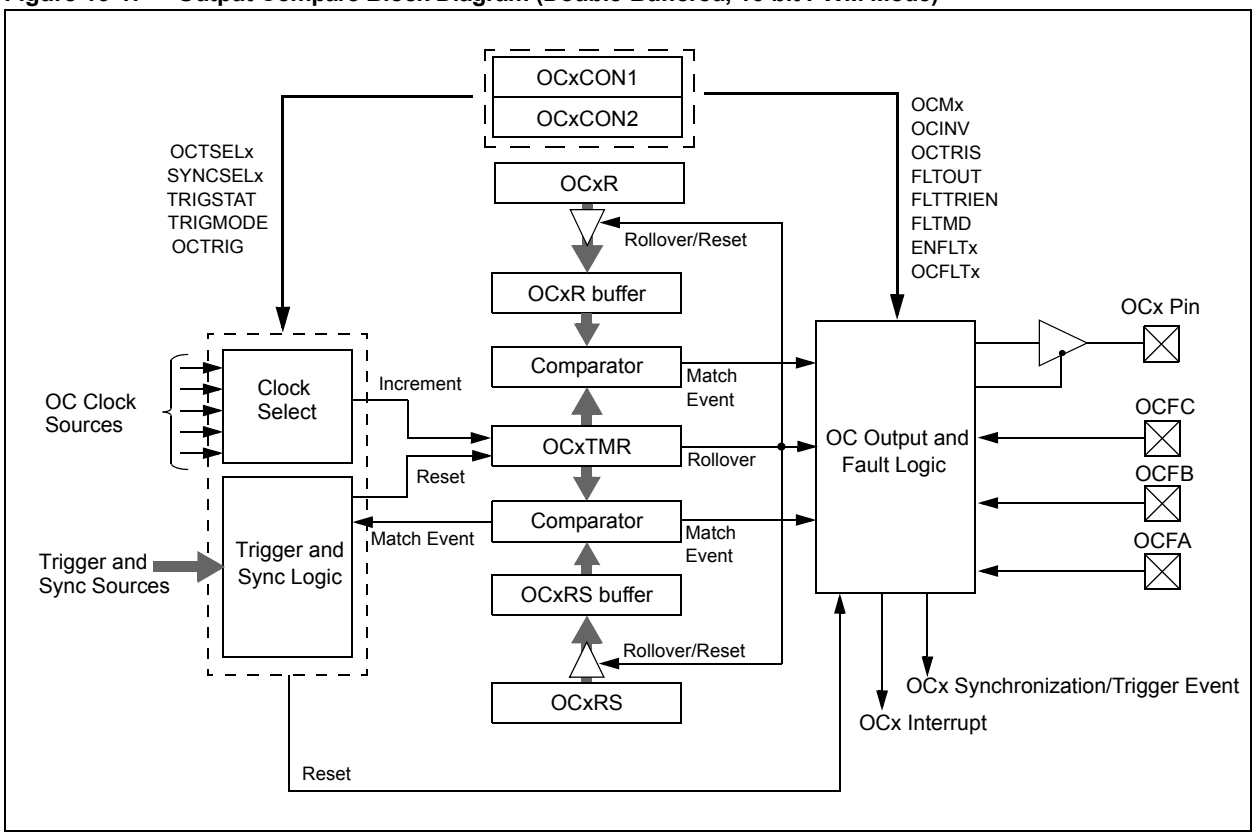
Figure 13-1 illustrates the block diagram of the output compare module.

Note 1: For more information on the number of available channels, refer to the specific device data sheet.

2: All the output compare channels are functionally identical. In this section, an 'x' in the pin, register or bit name denotes the specific output compare channel.

3: The OCx output must be assigned to an available RPn pin before the use, if the device supports Peripheral Pin Select (PPS). For more information, refer to the Peripheral Pin Select section in the data sheet.

Figure 13-1: Output Compare Block Diagram (Double-Buffered, 16-bit PWM Mode)



13.2 OUTPUT COMPARE REGISTERS

Each output compare channel is comprised of the following registers:

- **OCxCON1: Output Compare x Control Register 1**
- **OCxCON2: Output Compare x Control Register 2**
- **OCxR: Compare Register**
- **OCxRS: Secondary Compare Register**
- **OCxTMR: Internal Time Base Register**

Register 13-1: OCxCON1: Output Compare x Control Register 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB
bit 15							bit 8

R/W-0	R/W-0 HCS	R/W-0 HCS	R/W-0 HCS	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>		
bit 7							bit 0

Legend:	HCS = Hardware Clearable/Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **OCSIDL:** Stop Output Compare x in Idle Mode Control bit
1 = Output Compare x halts in CPU Idle mode
0 = Output Compare x continues to operate in CPU Idle mode

bit 12-10 **OCTSEL<2:0>:** Output Compare x Clock Select bits
111 = Peripheral clock (FCY)
110 = Reserved
101 = Reserved
100 = Timer1 clock (only the synchronous clock is supported)
011 = Timer5 clock
010 = Timer4 clock
001 = Timer3 clock
000 = Timer2 clock

bit 9 **ENFLTC:** Fault C Input Enable bit
1 = Output Compare Fault C input (OCFC) is enabled
0 = Output Compare Fault C input (OCFC) is disabled

bit 8 **ENFLTB:** Fault B Input Enable bit
1 = Output Compare Fault B input (OCFB) is enabled
0 = Output Compare Fault B input (OCFB) is disabled

bit 7 **ENFLTA:** Fault A Input Enable bit
1 = Output Compare Fault A input (OCFA) is enabled
0 = Output Compare Fault A input (OCFA) is disabled

bit 6 **OCFLTC:** PWM Fault C Condition Status bit
1 = PWM Fault C condition on OCFC pin has occurred
0 = No PWM Fault C condition on OCFC pin has occurred

bit 5 **OCFLTB:** PWM Fault B Condition Status bit
1 = PWM Fault B condition on OCFB pin has occurred
0 = No PWM Fault B condition on OCFB pin has occurred

bit 4 **OCFLTA:** PWM Fault A Condition Status bit
1 = PWM Fault A condition on OCFA pin has occurred
0 = No PWM Fault A condition on OCFA pin has occurred

Register 13-1: OCxCON1: Output Compare x Control Register 1 (Continued)

bit 3 **TRIGMODE:** Trigger Status Mode Select bit
1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
0 = TRIGSTAT is cleared only by software

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS
110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR
101 = Double Compare Continuous Pulse mode: Initialize OCx pin low, toggle OCx state continuously on alternate matches of OCxR and OCxRS
100 = Double Compare Single-Shot mode: Initialize OCx pin low, toggle OCx state on matches of OCxR and OCxRS for one cycle
011 = Single Compare mode: Compare events with OCxR, continuously toggle OCx pin
010 = Single Compare Single-Shot mode: Initialize OCx pin high, compare event with OCxR, forces OCx pin low
001 = Single Compare Single-Shot mode: Initialize OCx pin low, compare event with OCxR, forces OCx pin high
000 = Output compare channel is disabled

Register 13-2: OCxCON2: Output Compare x Control Register 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB<1:0>		OC32
bit 15							bit 8

R/W-0	R/W-0 HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>(1)				
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit
1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
1 = PWM output is driven high on a Fault
0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
1 = OCx pin is tri-stated on Fault condition
0 = OCx pin I/O state defined by FLTOUT bit on Fault condition

bit 12 **OCINV:** OCMP Invert bit
1 = OCx output is inverted
0 = OCx output is not inverted

bit 11 **Unimplemented:** Read as '0'

bit 10-9 **DCB<1:0>:** PWM Duty Cycle Least Significant bits
These bits can be considered as the Least Significant bits of the duty cycle in the Pulse Generation modes. They are also used to delay the falling edge of the OCx output in all other modes; rising edge when output conversion is active (OCINV (OCxCON2<12> = 1).
11 = OCx output falling edge transitions on rising edge of system clock plus 3/4 TCY
10 = OCx output falling edge transitions on rising edge of system clock plus 1/2 TCY
01 = OCx output falling edge transitions on rising edge of system clock plus 1/4 TCY
00 = OCx output falling edge transitions on rising edge of system clock

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
1 = Cascade module operation enabled
0 = Cascade module operation disabled

bit 7 **OCTRIG:** OCx Trigger/Sync Select bit
1 = Trigger OCx from source designated by SYNCSELx bits
0 = Synchronize OCx with source designated by SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
1 = Timer source has been triggered and is running
0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** OCx Output Pin Direction Select bit
1 = OCx is tri-stated
0 = Output compare module drives the OCx pin

Note 1: When OCx is switched off, it sends a trigger out signal. If any other OCy module uses OCx as a trigger source, it must deselect OCx as a trigger source before OCx is switched off.

Register 13-2: OCxCON2: Output Compare x Control Register 2 (Continued)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

11111 = OCxRS compare event is used for synchronization
11110 = IC9 module synchronizes or triggers OCx
11101 = IC6 module synchronizes or triggers OCx
11100 = Reserved
11011 = ADC1 module synchronizes or triggers OCx
11010 = CMP3 module synchronizes or triggers OCx
11001 = CMP2 module synchronizes or triggers OCx
11000 = CMP1 module synchronizes or triggers OCx
10111 = IC4 module synchronizes or triggers OCx
10110 = IC3 module synchronizes or triggers OCx
10101 = IC2 module synchronizes or triggers OCx
10100 = IC1 module synchronizes or triggers OCx
10011 = IC8 module synchronizes or triggers OCx
10010 = IC7 module synchronizes or triggers OCx
10001 = Reserved
10000 = Reserved
01111 = Timer5 synchronizes or triggers OCx
01110 = Timer4 synchronizes or triggers OCx
01101 = Timer3 synchronizes or triggers OCx
01100 = Timer2 synchronizes or triggers OCx
01011 = Timer1 synchronizes or triggers OCx
01010 = IC5 module synchronizes or triggers OCx
01001 = OC9 module synchronizes or triggers OCx(1)
01000 = OC8 module synchronizes or triggers OCx(1)
00111 = OC7 module synchronizes or triggers OCx(1)
00110 = OC6 module synchronizes or triggers OCx(1)
00101 = OC5 module synchronizes or triggers OCx(1)
00100 = OC4 module synchronizes or triggers OCx(1)
00011 = OC3 module synchronizes or triggers OCx(1)
00010 = OC2 module synchronizes or triggers OCx(1)
00001 = OC1 module synchronizes or triggers OCx(1)
00000 = No sync or trigger source for OCx

Note 1: When OCx is switched off, it sends a trigger out signal. If any other OCy module uses OCx as a trigger source, it must deselect OCx as a trigger source before OCx is switched off.

Register 13-3: OCxR: Compare Register

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Compare Value<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Compare Value<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **Compare Value<15:0>:** Compare Register Value bits

Register 13-4: OCxRS: Secondary Compare Register

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Secondary Compare Value<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Secondary Compare Value<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **Secondary Compare Value<15:0>:** Secondary Compare Register Value bits

13.3 MODES OF OPERATION

Each output compare module comprises the following modes of operation:

- Single Compare Match mode
- Dual Compare Match mode generating:
  - Single output pulse
  - Continuous output pulse
- Simple Pulse-Width Modulation mode with/without Fault protection:
  - Edge-aligned
  - Center-aligned
- Cascade mode (32-bit operation)

Before understanding the modes, it is necessary to understand the synchronization/trigger. In synchronous operation, the internal timer is reset (to zero) when the source selected by the SYNCSEL<4:0> (OCxCON2<4:0>) bits send a Sync signal. In Trigger mode, the internal timer is held in the Reset state until the selected trigger source sends a Sync signal.

The Synchronous or Trigger mode is selected by the OCTRIG (OCxCON2<7>) bit and the synchronization/trigger source can be selected by the SYNCSEL<4:0> bits as indicated in **13.2 "Output Compare Registers"**.

Note 1:	SYNCSEL<4:0> = `0b00000` puts the timer in a Free-Running mode with no synchronization.
2:	SYNCSEL<4:0> = `0b11111` makes the timer reset when it reaches the value of OCxRS, making the OCx module use its own Sync signal.
3:	OCx module sends a synchronization/trigger signal when its timer matches OCxRS.

For more information on Synchronous/Trigger mode, refer to **13.3.3.7 "Synchronous Operation"**.

13.3.1 Single Compare Match Mode

When control bits, OCM<2:0> of the OCxCON1 register = `0b001`, `0b010` or `0b011`, the selected output compare channel is configured as:

- If OCM = `0b001`: The OCx pin is initially set low; a subsequent compare event with OCxR sets the pin high
- If OCM = `0b010`: The OCx pin is initially set high; a subsequent compare event with OCxR sets the pin low
- If OCM = `0b011`: The OCx pin is initially set low, a subsequent compare event with OCxR toggles the pin

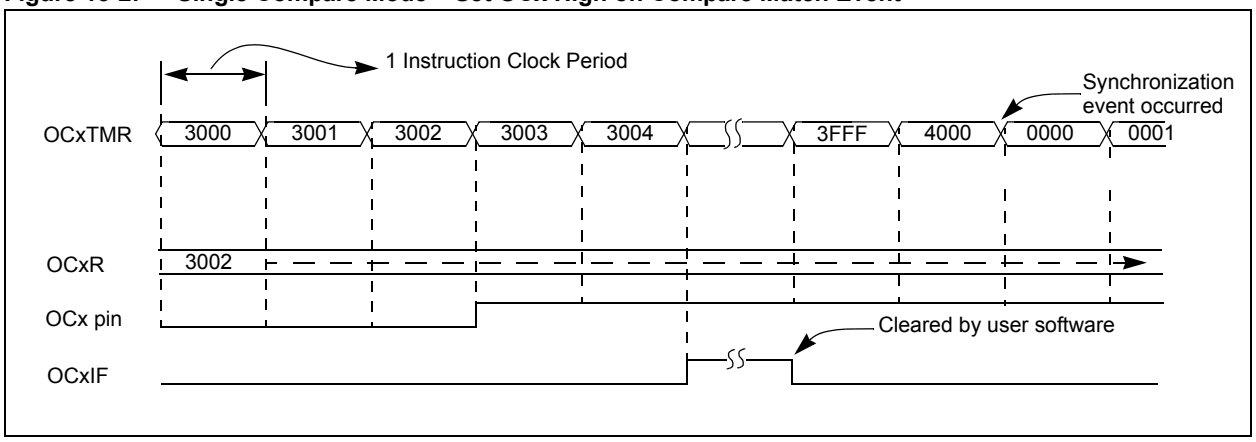
In Single Compare Match mode, the OCxR register is used to generate compare events. This register is loaded with a value and is compared with the module Timer register. The interrupt is set on each compare event if there is a level change in the OCx pin.

13.3.1.1 SINGLE COMPARE MODE OUTPUT DRIVEN HIGH

To configure the module for this mode, set control bits OCM<2:0> (OCxCON1<2:0>) = 0b001. After this Compare mode is enabled, the output pin, OCx, would be initially driven low and remain low until a match between the timer and the OCxR registers occurs. Figure 13-2 illustrates the following key timing events:

- The OCx pin is driven high one instruction clock after a compare match between the timer and the OCxR register. The OCx pin remains high until a mode change or the module is turned off.
- The timer counts up until it rolls over, or a synchronization event occurs, and then resets (to 0x0000) on the next instruction clock.
- The respective channel interrupt flag, OCxIF, is asserted two instruction clocks after the OCx pin is driven high.

Figure 13-2: Single Compare Mode – Set OCx High on Compare Match Event

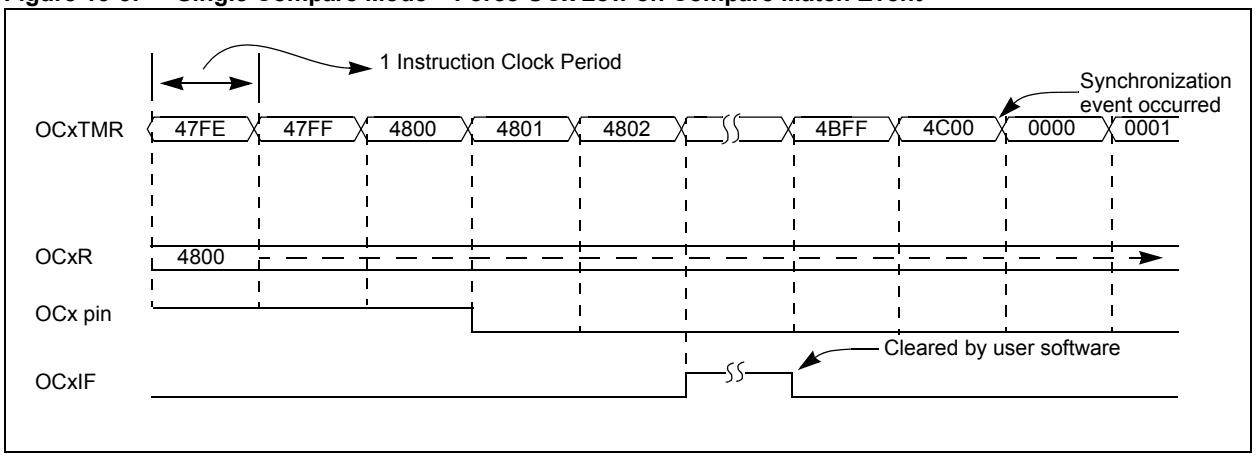


13.3.1.2 SINGLE COMPARE MODE OUTPUT DRIVEN LOW

To configure the output compare module for this mode, set control bits OCM<2:0> = 0b010. After this Compare mode is enabled, the output pin and the OCx would be initially driven high and remain high until a match occurs between the Timer and the OCxR registers. Figure 13-3 illustrates the key timing events.

- The OCx pin is driven low one instruction clock after a compare match event occurs between the timer and the OCxR register. The OCx pin remains low until a mode change or the module is turned off.
- The timer counts up until it rolls over or a synchronization event occurs, and then resets to 0x0000 on the next instruction clock.
- The respective channel interrupt flag, OCxIF, is asserted two instruction clocks after OCx pin is driven low.

Figure 13-3: Single Compare Mode – Force OCx Low on Compare Match Event

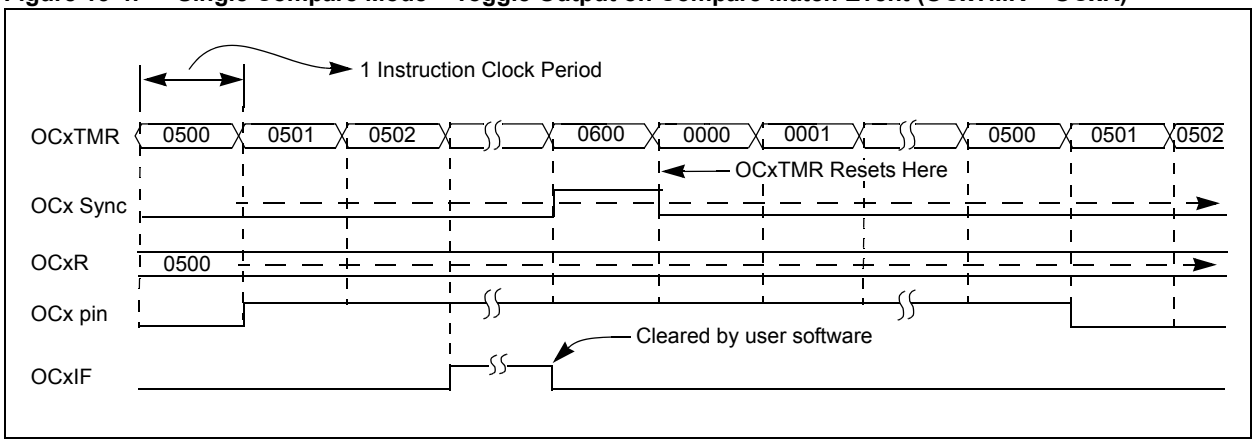


13.3.1.3 SINGLE COMPARE MODE TOGGLE OUTPUT

To configure the output compare module for this mode, set control bits OCM<2:0> = 0b011. After this Compare mode has been enabled, the output pin and the OCx toggle on every match event between the timer and the OCxR registers. Figure 13-4 illustrates the key timing events.

- The OCx pin is toggled one instruction clock after a compare match occurs between the timer and OCxR register. The OCx pin remains at this new state until the next toggle event, or until a mode change has been made or the module is turned off.
- The timer counts up until it rolls over or synchronization occurs, and then resets to 0x0000 on the next instruction clock.
- The respective channel interrupt flag, OCxIF, is asserted two instruction clocks after the OCx pin is toggled.
- The internal OCx pin output logic is set to a logic '0' on a device Reset. However, the operational OCx pin state for the Toggle mode can be set by the user-assigned software.

Figure 13-4: Single Compare Mode – Toggle Output on Compare Match Event (OCxTMR > OCxR)



Example 13-1: Single Compare Mode Toggle Output

```
OC1CON1 = 0;              /* It is a good practice to clear off the control bits initially */
OC1CON2 = 0;
OC1CON1bits.OCTSEL = 0x07;/* This selects the peripheral clock as the clock input to the OC
                          module */
OC1R = 1000;              /* This is just a typical number, user must calculate based on the
                          waveform requirements and the system clock */
OC1CON1bits.OCM = 3;      /* This selects the toggle mode */
```

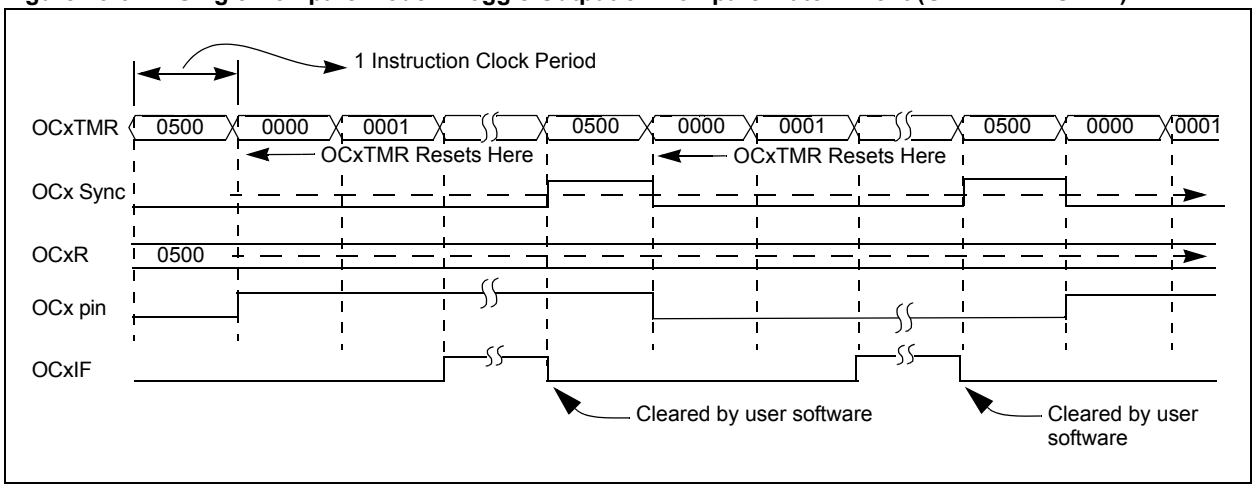
13.3.1.4 SPECIAL CASES OF SINGLE COMPARE MODE

Consider the following few special cases:

Table 13-1: Special Cases of Single Compare Mode

Special Condition	Operation	Output
When OCxR > timer period (as determined by the Sync source)	No compare event occurs and the compare output remains at the initial condition.	No change in output level
When OCxR = timer period (as determined by the Sync source)	The compare output functions normally. Combining this with the Toggle mode can be used to generate a fixed frequency square wave as illustrated in Figure 13-5.	Output level transition
When the module is enabled into a Single Compare mode, OCxR = 0x0000, and the timer is held in Reset, the Sync source is active	The compare output remains in the initial condition.	No change in output level
If, after a compare event, the OCxR register is cleared and the Sync source becomes active	Output remains in the new state.	No further change in output level

Figure 13-5: Single Compare Mode – Toggle Output on Compare Match Event (OCxTMR = OCxR)



13.3.2 Dual Compare Match Mode

When control bits, OCM<2:0> = 0b100 or 0b101, the selected output compare channel is configured for one of these following Dual Compare Match modes:

- Single Output Pulse mode
- Continuous Output Pulse mode

In the Dual Compare mode, the module uses both the OCxR and OCxRS registers for the compare match events. The OCxR register is compared with the incrementing timer count, OCxTMR, and the rising (leading) edge of the pulse is generated at the OCx pin on a compare match event. The OCxRS register is then compared to the same incrementing timer count, OCxTMR, and the falling (trailing) edge of the pulse is generated at the OCx pin on a compare match event.

13.3.2.1 DUAL COMPARE SINGLE PULSE MODE

When control bits, OCM<2:0> = 0b100, the selected output compare channel is configured so that the OCx pin is initialized low and a single output pulse is generated. Refer to Figure 13-6 and Figure 13-7.

1. Once the Dual Compare Single Pulse mode is enabled, the OCx pin will be driven low.
2. Upon the first timer compare match with OCxR, the Compare register and its pin (OCx) would be driven high.
3. When the incrementing timer count matches Compare register, OCxRS, the second and trailing edge (high-to-low) of the pulse is driven onto the OCx pin. At this second compare, the OCxIF interrupt flag bit gets set.

Note 1: While the mode bits do not change after the falling edge of the pulse, if another write with the same value occurs on the same control bits, a new single output pulse sequence is generated.

2: OCxRS must be greater than the OCxR by a minimum of 2.

Figure 13-6: Dual Compare Mode Single Output Pulse

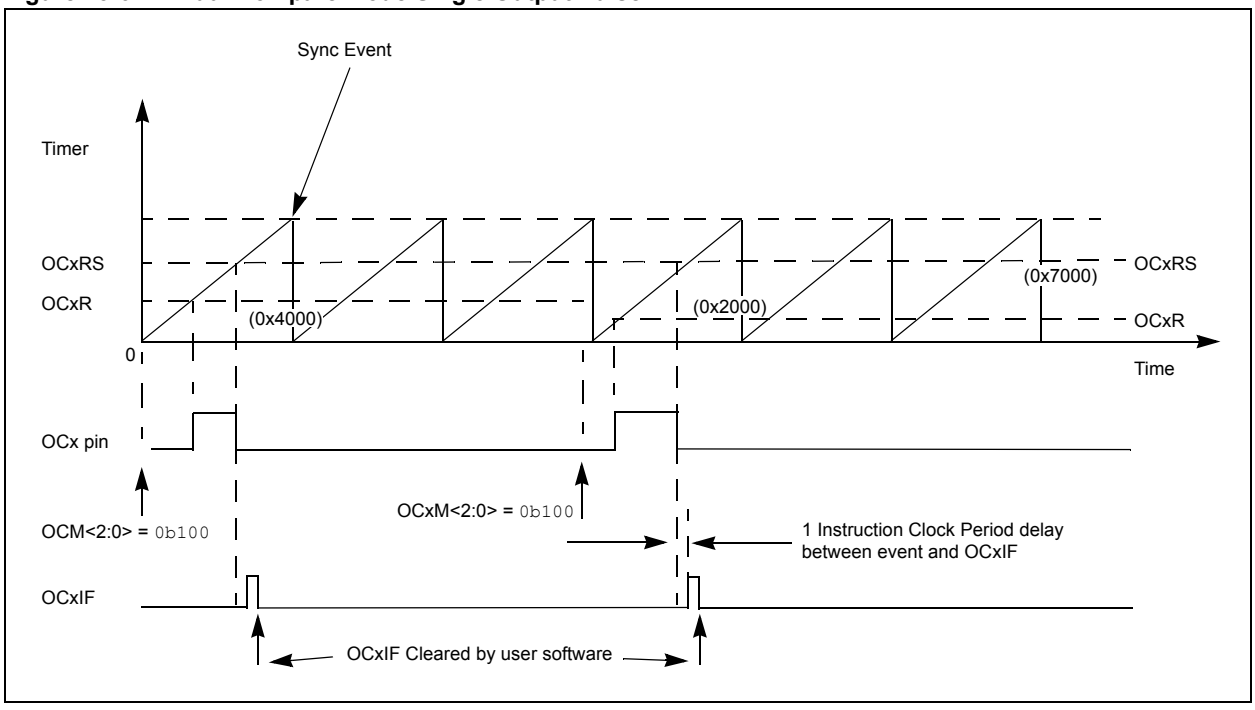
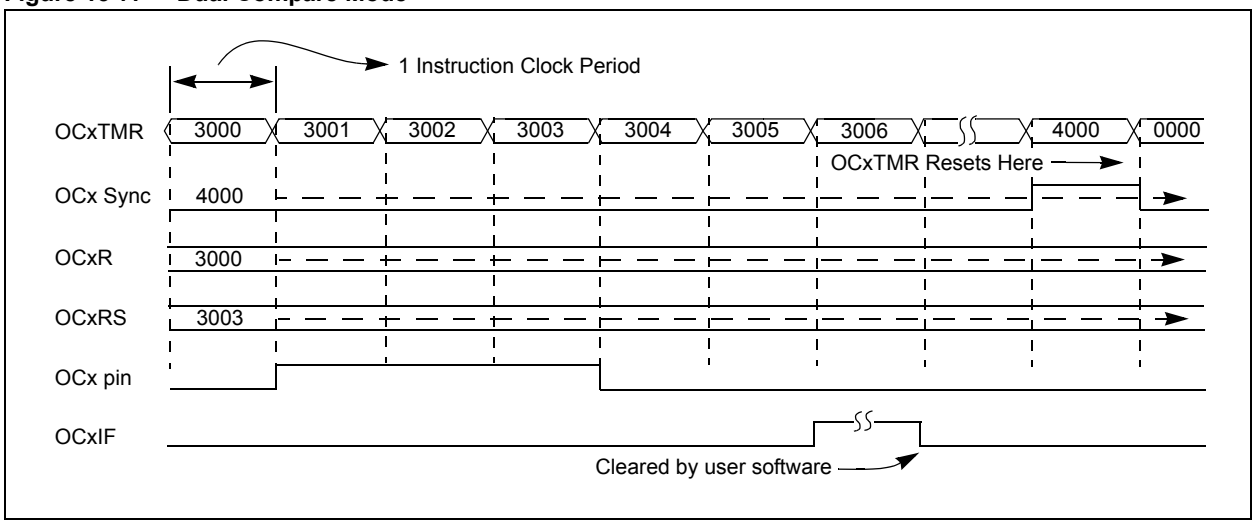


Figure 13-7: Dual Compare Mode



13.3.2.2 TO SET UP SINGLE OUTPUT PULSE GENERATION

To configure the module for generating a single output pulse, perform these steps:

1. Determine the instruction cycle time, TCY.
2. Calculate the desired pulse-width value base upon TCY.
3. Calculate the time to start pulse from timer start value of 0x0000.
4. Write pulse-width start and stop times into OCxR and OCxRS Compare registers.
5. Select SYNCSEL<4:0> so that the synchronization is active after the timer is equal to or greater than the value in OCxRS.
6. Set OCM<2:0> = `0b100`.
7. Issue another write to set OCM<2:0> = `0b100`, to initiate another single pulse with the same parameters.
8. Disable the OCx by writing OCM<2:0> = `0b000`, change the parameters, and then enable the OCx by writing OCM<2:0> = `0b100` to initiate another single pulse with different parameters.

Note 1: Refer to Table 13-2 for several simple examples of single output pulse-width calculations.

2: Refer to Table 13-3 for several simple examples of Dual Compare Match mode generating a single output pulse.

Table 13-2: Dual Compare Mode – Single Output Pulse-Width Calculation Examples

Instruction Cycle Time (TCY)	Desired on Time		Start Pulse Time from Timer = 0x0000		End Pulse Time (OCxRS) Register
	Time	Hex Value	Time	Hex Value (OCxR)	
16.6 ns	1 μs	0x003C	10 μs	0x0258	0x0294
30 ns	1 μs	0x0021	10 μs	0x014D	0x016E
30 ns	2 μs	0x0042	10 μs	0x014D	0x018F
50 ns	3 μs	0x003C	10 μs	0x00C8	0x0104
100 ns	5 μs	0x0032	50 μs	0x0064	0x0096
300 ns	10 μs	0x0021	100 μs	0x014D	0x018F
500 ns	20 μs	0x0028	500 μs	0x03E8	0x0410
500 ns	30 μs	0x003C	2 ms	0x0FA0	0x0FDC

Equation 13-1:

OCxR Value = Desired Time/Instruction Cycle Time (TCY)

Example 13-2: Dual Compare Mode – Single Output Pulse-Width

```
OC1CON1 = 0;                /* It is a good practice to clear off the control bits initially */
OC1CON2 = 0;
OC1CON1bits.OCTSEL = 0x07; /* This selects the peripheral clock as the clock input to the OC
                               module */
OC1R = 1000;                /* This is just a typical number, user must calculate based on the
                            waveform requirements and the system clock */
OC1RS = 2000;
OC1CON1bits.OCM = 4;        /* This selects the Single Output Pulse mode */
```

Table 13-3: Special Cases for Dual Compare Match Mode Generating a Single Output Pulse

Special Condition	Operation	Output
Synchronization occurs when timer value is equal to OCxRS	Timer resets to zero in the next cycle, but the pulse is unaffected.	Pulse
Synchronization occurs before the timer value reaches OCxR	Timer resets to zero before any output transition.	Remains low
Synchronization occurs before the timer value reaches OCxRS but after it reaches OCxR	Only a single transition (low-to-high) is generated (see Figure 13-8).	Low-High
OCxR = OCxRS = 0x0000 and Sync occurs	The output is initialized low and does not change. No interrupt is generated.	Remains low
OCxRS < OCxR	The timer counts up to the first compare (TMRx = OCxR) and the first (rising) edge is generated. The timer then continues to count and eventually resets when the synchronization occurs or rolls over. The timer then restarts from 0x0000 and counts up to the second compare (TMRx = OCxRS) and the second (falling) edge of the signal is generated. The falling edge of the output pulse generates an interrupt condition.	Pulse
OCxR = OCxRS	The timer counts up to the first compare (Timer = OCxR) and the first (rising) edge is generated. The timer continues to count and eventually resets when the synchronization occurs or a rollover from 0xFFFF occurs. The timer then restarts from 0x0000 and counts up to the second compare (TMRx = OCxRS), and the second (falling) edge of the signal is generated. The falling edge of the output pulse generates an interrupt condition.	Pulse
OCxR = 0x0000 and OCxRS > OCxR	The first cycle of the timer counts until the synchronization occurs or rolls over; the output compare pin remains low. After the Timer register resets to zero, the output compare pin goes high. Upon the next timer match with the register, OCxRS, the output compare pin goes low and remains. The falling edge of the output pulse generates an interrupt condition (see Figure 13-9).	Pulse except for the first cycle

Figure 13-8: Dual Compare Mode – Single Output Pulse (Sync Before Timer Reaches OCxRS)

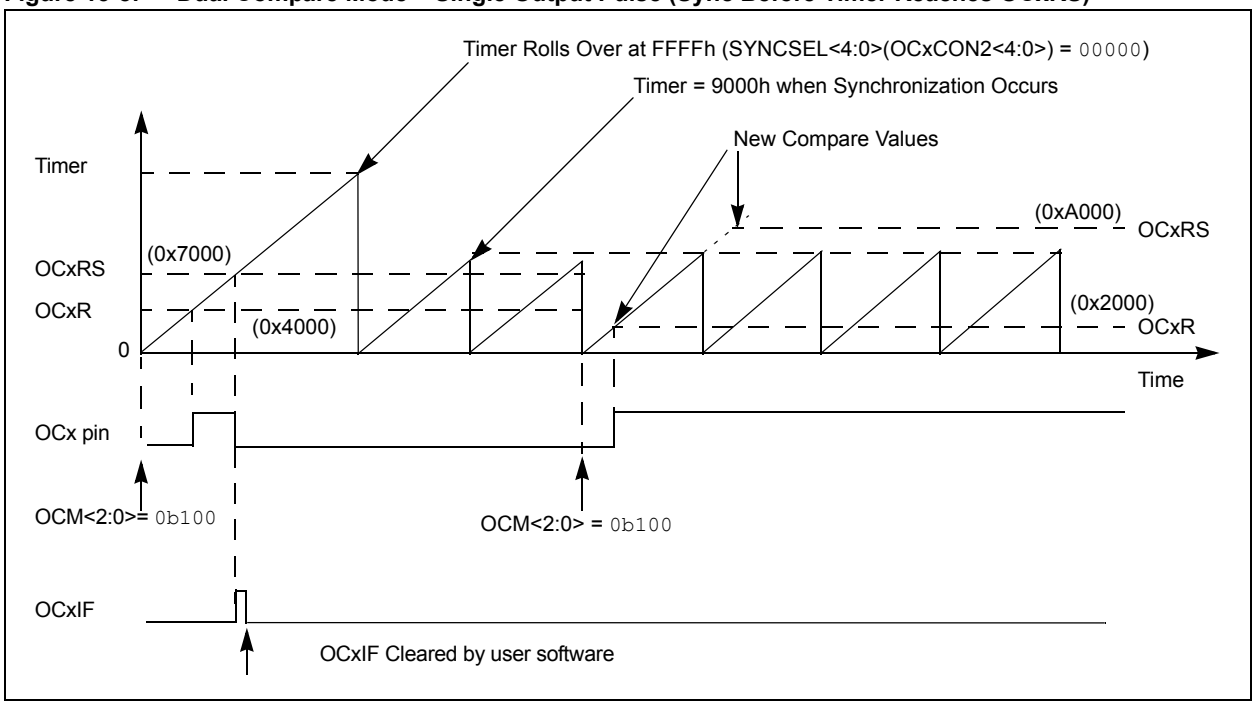
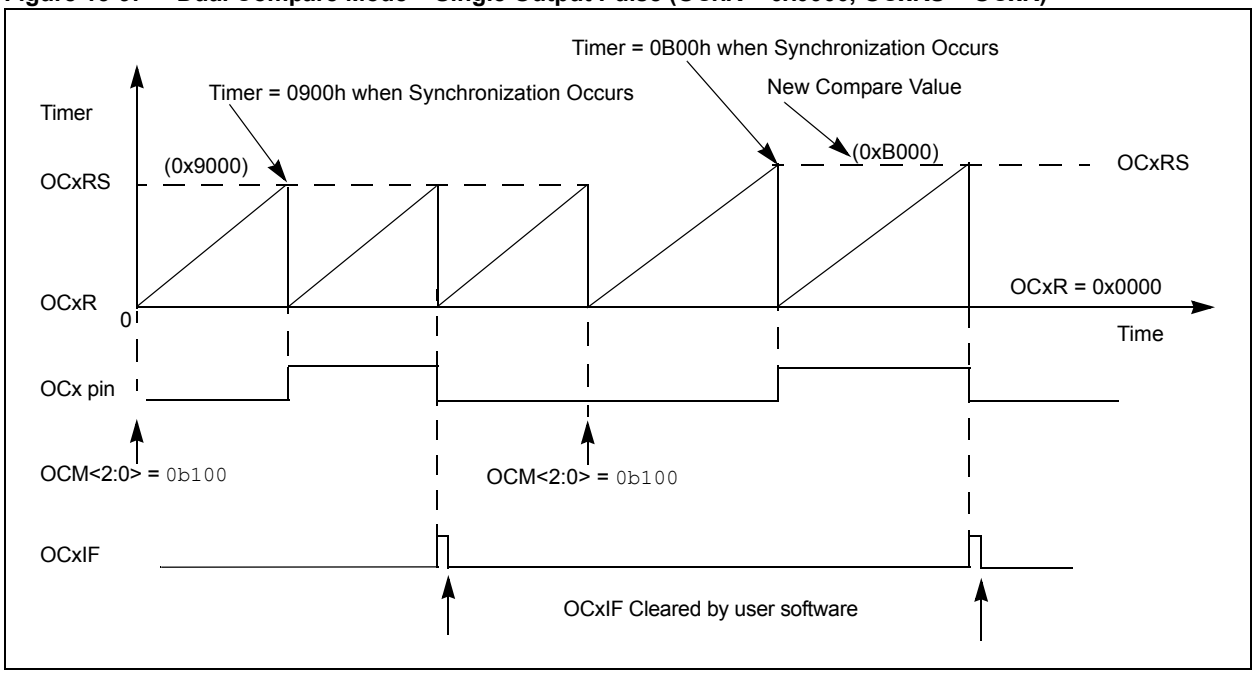


Figure 13-9: Dual Compare Mode – Single Output Pulse (OCxR = 0x0000, OCxRS > OCxR)



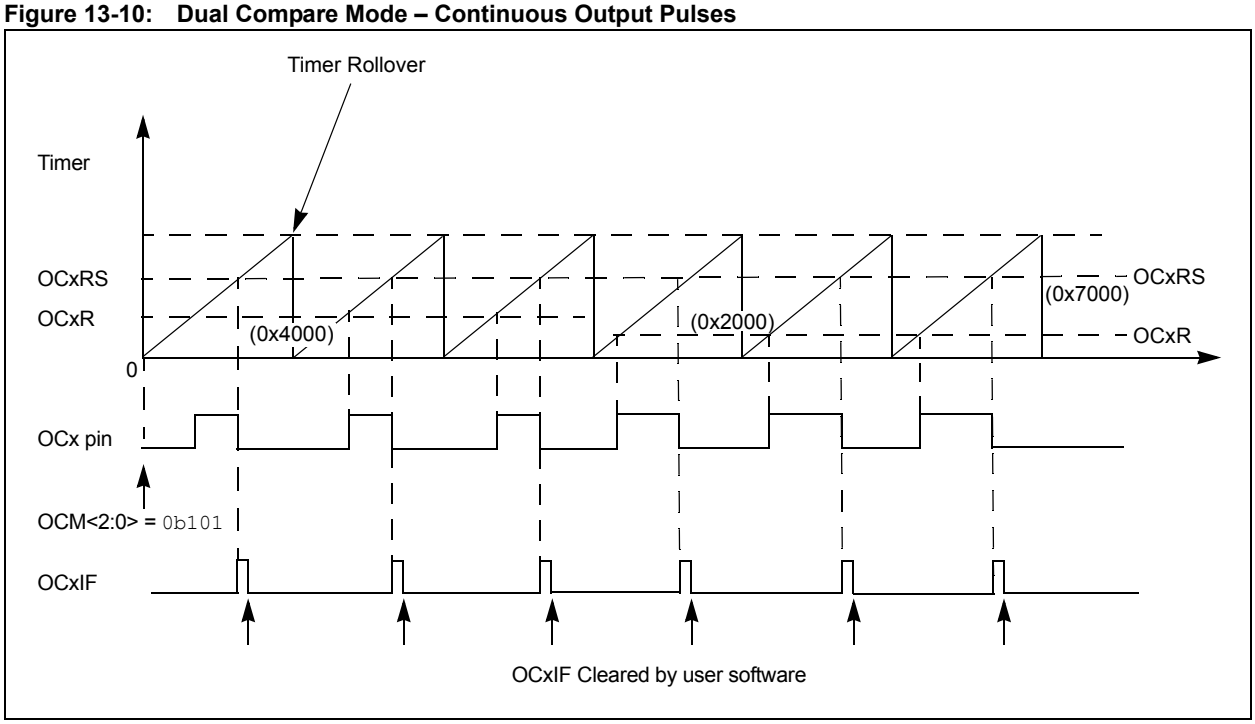
13.3.2.3 DUAL COMPARE CONTINUOUS PULSE MODE

When control bits, OCM<2:0> = 0b101, the selected output compare channel is configured so that the OCx pin is initialized low and continuous output pulses are generated. Figure 13-10 illustrates the Dual Compare Continuous Output Pulse mode.

- Once the Dual Compare Continuous Output Pulse mode is enabled, the pin state would be driven low.
- Upon the first timer compare match with compare register, OCxR, the OCx pin will be driven high.
- When the incrementing timer count matches Compare register, OCxRS, the second and the trailing edge (high-to-low) of the pulse are driven onto the OCx pin. At this second compare, the OCxIF interrupt flag bit is set.

Note 1:	Unlike the Single Output Pulse mode, the output pulses continue indefinitely until the mode is terminated by user firmware or by a Reset. The falling edge of each output pulse sets the interrupt flag.
2:	One way of generating a pulse with 50% duty cycle is by setting OCxR = OCxRS (this value must be within the Period register range as the period is determined by the Sync source).

Figure 13-10: Dual Compare Mode – Continuous Output Pulses



13.3.2.4 SETUP FOR CONTINUOUS OUTPUT PULSE GENERATION

To configure this module for the generation of a continuous stream of output pulses, perform the following steps:

1. Determine instruction cycle time, TCY.
2. Calculate the timer to start pulse-width from the timer start value of 0x0000.
3. Calculate the timer to stop pulse-width from the timer start value of 0x0000.
4. Write pulse-width start and stop times into the OCxR and OCxRS Compare registers. The Sync signal should occur when OCxRS = timer or after.
5. Set OCM<2:0> = 0b101; the timer must be enabled.

Example 13-3: Continuous Output Pulse Generation

```
OC1CON1 = 0;
OC1CON2 = 0;                /* It is a good practice to clear off the control bits initially */
OC1CON1bits.OCTSEL = 0x07; /* This selects the peripheral clock as the clock input to the OC
                            module */
OC1R = 1000;                /* This is just a typical number, user must calculate based on the
                            waveform requirements and the system clock */
OC1RS = 2000;
T1CON = 0;
PR1 = 3000;                 /* Determines the period */
OC1CON2bits.SYNCSEL = 0x0B;/* TMR1 is the sync source */
OC1CON1bits.OCM = 5;        /* This selects the Continuous Pulse mode*/
T1CONbits.TON = 1;          /* OC1TMR does not run until the sync source is switched on */
```

Table 13-4: Dual Compare Mode – Continuous Output Pulse-Width Calculation Examples

Instruction Cycle Time (TCY)	Desired Pulse-Width		Start Pulse Time from Timer = 0x0000		Period Register Contents	End Pulse Time (OCxRS) Register (for 50% duty cycle)
	Time	Hex Value	Time	Hex Value (OCxR)		
30 ns	1 μs	0x0021	10 μs	0x014D	0x016F	0x015D
30 ns	2 μs	0x0042	10 μs	0x014D	0x0190	0x016F
50 ns	3 μs	0x003C	10 μs	0x00C8	0x0105	0x00E6
100 ns	5 μs	0x0032	50 μs	0x0064	0x0097	0x007D
300 ns	10 μs	0x0021	100 μs	0x014D	0x0190	0x015D
500 ns	20 μs	0x0028	500 μs	0x03E8	0x057A	0x03FC
500 ns	30 μs	0x003C	2 ms	0x0FA0	0x0FC9	0x0FBE

Equation 13-2:

$$Hex\ Value = Desired\ Time/Instruction\ Cycle\ Time\ (T_{CY})$$

Note: Timer module with the same clock as OCx is used as the Sync source in this example.

Table 13-5: Special Cases for Dual Compare Match Mode Generating Continuous Output Pulse

Special Condition	Operation	Output
Synchronization occurs when the timer value is equal to OCxRS	Timer resets to zero in the next cycle, but the pulse is unaffected (see Figure 13-11).	Pulses
Synchronization occurs before the timer value reaches OCxR	Timer resets to zero before any output transition.	Remains low
Synchronization occurs before the timer value reaches OCxRS but after it reaches OCxR	Only a single transition (low-to-high) is generated (see Figure 13-12).	Low-High
OCxR = OCxRS = 0x0000 and synchronization occurs	The output is initialized low and does not change. No interrupt is generated.	Remains low
OCxRS < OCxR	The timer counts up to the first compare (TMRx = OCxR) and the first (rising) edge is generated. The timer then continues to count and eventually resets when synchronization occurs or rolls over. The timer then restarts from 0x0000 and counts up to the second compare (TMRx = OCxRS) and the second (falling) edge of the signal is generated. The falling edge of the output pulse generates an interrupt condition. The sequence repeats until the module is disabled.	Pulses
OCxR = OCxRS	The timer counts up to the first compare (Timer = OCxR) and the first (rising) edge is generated. The timer continues to count and eventually resets when synchronization occurs or a rollover from FFFFh occurs. The timer then restarts from 0x0000 and counts up to the second compare (TMRx = OCxRS), and the second (falling) edge of the signal is generated. The falling edge of the output pulse generates an interrupt condition. The sequence repeats until the module is disabled.	Pulses
OCxR = 0x0000 and OCxRS > OCxR	The first cycle of the timer counts until synchronization occurs or rolls over; the output compare pin remains low. After the Timer register resets to zero, the output compare pin goes high. Upon the next timer match with the register, OCxRS, the output compare pin goes low and remains low. The falling edge of the output pulse generates an interrupt condition (see Figure 13-13). The sequence repeats until the module is disabled.	Pulses except for the first cycle

Figure 13-11: Dual Compare Mode – Continuous Output Pulse (Sync Occurs When Timer = OCxRS)

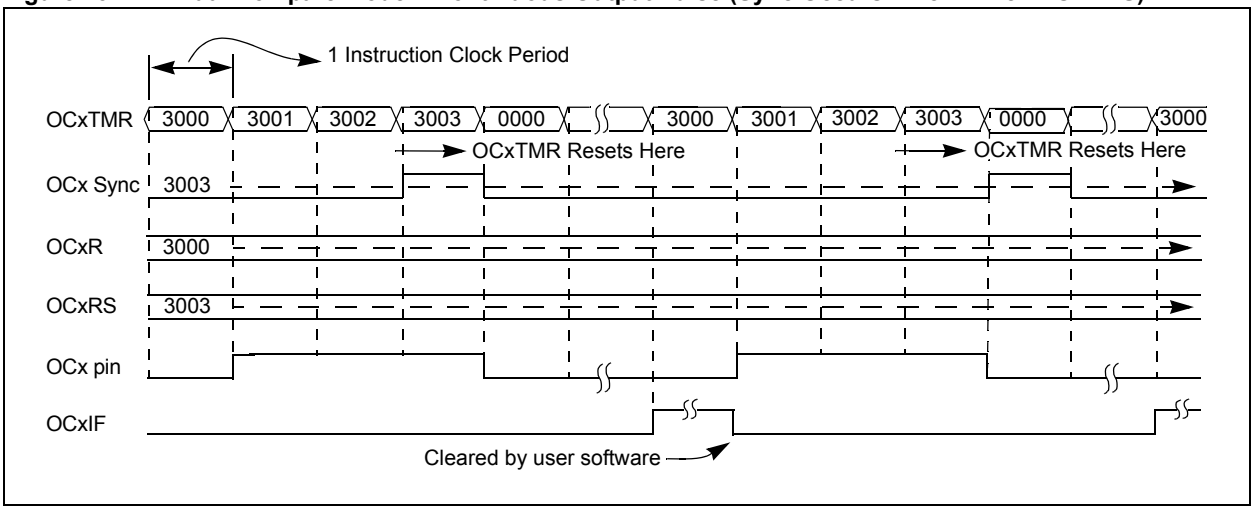


Figure 13-12: Dual Compare Mode – Continuous Output Pulse (Sync Before Timer Reaches OCxRS)

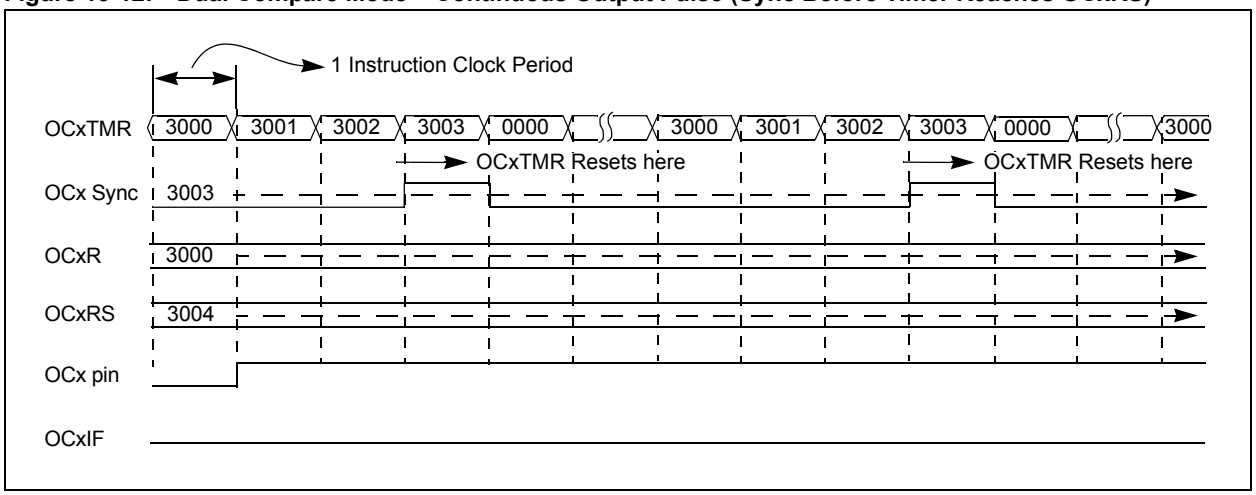
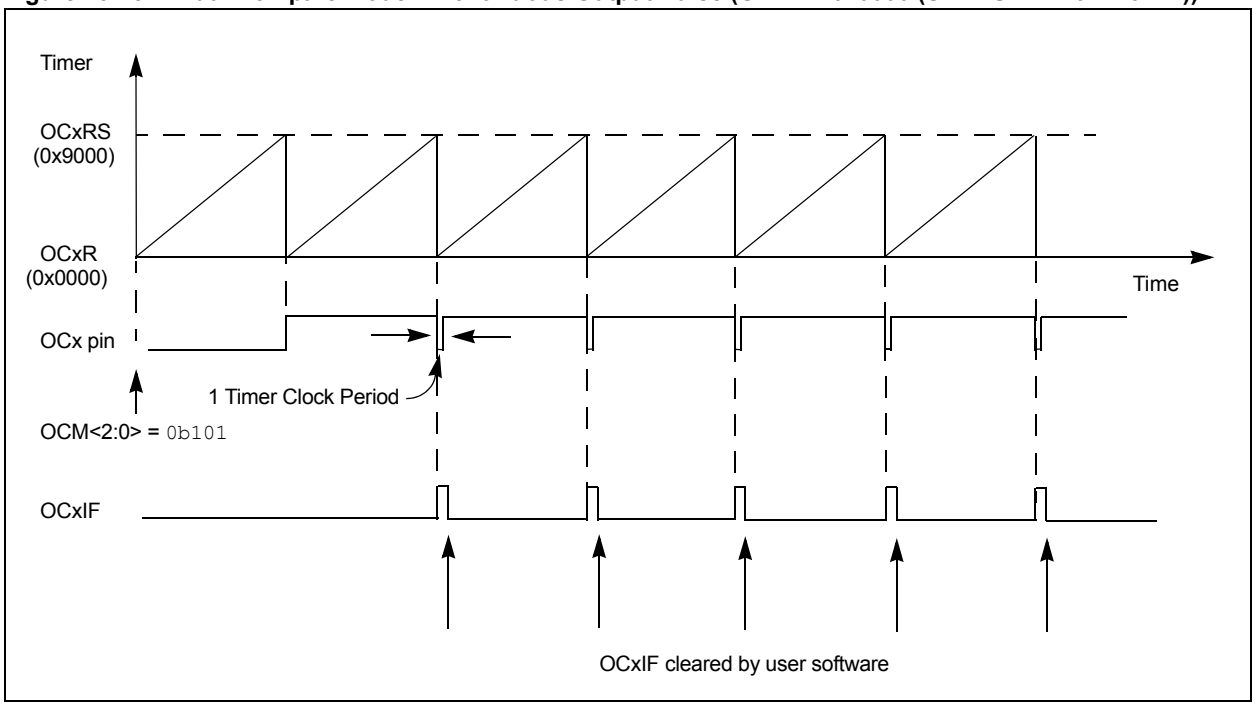


Figure 13-13: Dual Compare Mode – Continuous Output Pulse (OCxR = 0x0000 (SYNCSEL<4:0> = 0x1F))



13.3.3 Pulse-Width Modulation (PWM) Mode

When control bits OCM<2:0> = 0b110 or 0b111, the PWM mode is selected. The registers, OCxR and OCxRS, are double-buffered in these modes. This means that the changes on these registers will be reflected only after a timer rollover from 0xFFFF or after a Sync event occurs. As a result, any changes in these registers during operation occurs only with the next pulse. Also, in these modes, Fault input is supported (described in the next sections).

13.3.3.1 EDGE-ALIGNED PWM MODE

When control bits, OCM<2:0> = 0b110, the Edge-Aligned PWM mode of operation is selected. OCxR contains the current duty cycle and the SYNCSEL bits determine the period. OCxRS can be made to determine the period by setting SYNCSEL<4:0> = 0x1F.

Figure 13-14 and Figure 13-15 illustrate the PWM mode operation.

Edge-Aligned PWM Mode Operation:

- When synchronization occurs, the following four events occur on the next increment cycle:
  - The timer is reset to zero and resumes counting
  - The OCx pin is set high (exception: if OCxRS = 0b0000, the OCx pin would not be set)
  - The OCxR and OCxRS Buffered registers are updated from OCxR and OCxRS
  - Interrupt flag, OCxIF, is set
- When the timer and OCxR match, the pin would be set low. This match does not generate interrupts.

Figure 13-14: PWM Output Timing

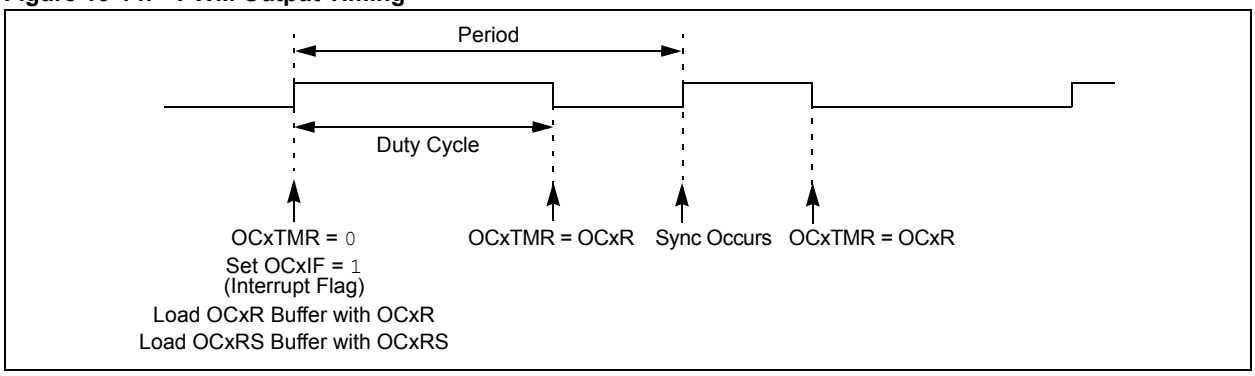
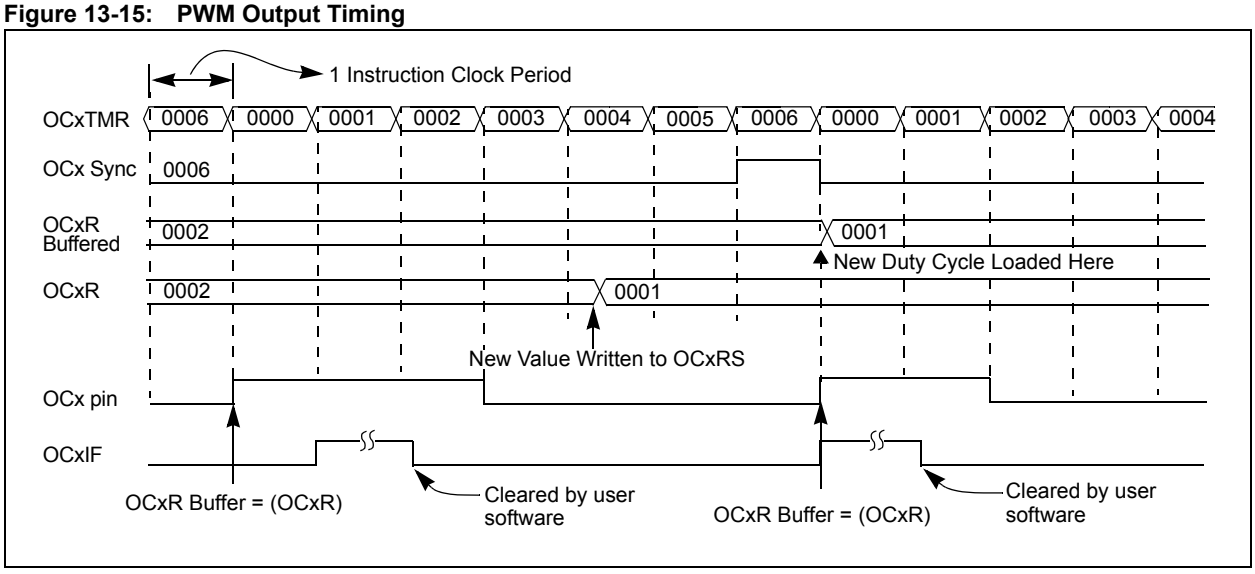


Figure 13-15: PWM Output Timing



13.3.3.2 EDGE-ALIGNED PWM MODE INITIALIZATION

1. After the PWM mode is enabled by setting OCM<2:0> = 0b110, the OCx pin would be driven low if OCxR = 0x0000. If OCxR is not equal to zero, the OCx pin will be set high (see Figure 13-16 and Figure 13-17).
2. When OCxR is not equal to zero and the pin state is set to high, the first match between the OCxR and the timer clears the OCx pin. The OCx pin would remain low until a valid compare between synchronization occurs or a rollover occurs (see Figure 13-17).

Figure 13-16: Edge-Aligned PWM Mode with OCxR = 0 (at Module Initialization, OCxR = 0x0000, OCxRS = 0x5000)

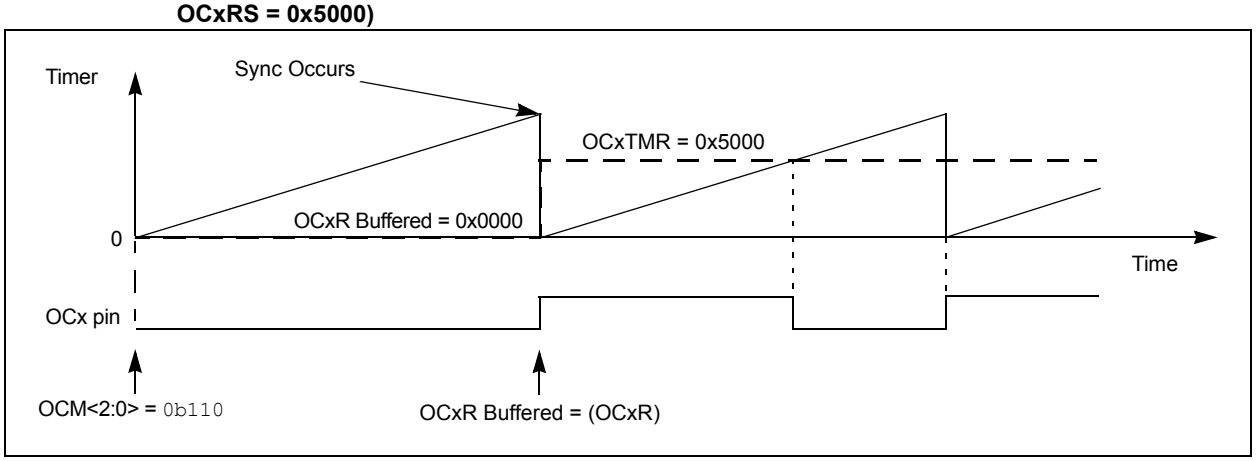
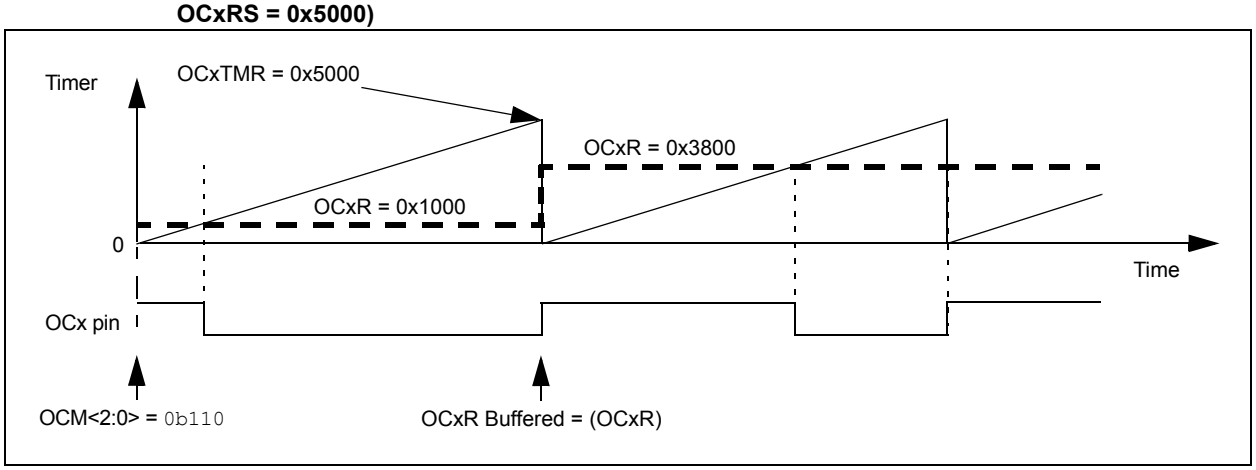


Figure 13-17: Edge-Aligned PWM Mode with OCxR > 0 (at Module Initialization, OCxR = 0x1000, OCxRS = 0x5000)



13.3.3.3 USER SETUP FOR PWM OPERATION

Perform the following steps while configuring the output compare module for the PWM operation:

1. Determine instruction cycle time, TCY.
2. Calculate desired pulse on time value based upon TCY and write it into OCxR.
3. Calculate the period value based upon TCY and write it into OCxRS.
4. Write 0x1F to SYNCSEL<4:0>.
5. Set the required clock source.
6. Set OCM<2:0> of OCxCON1 = `0b110` to select Edge-Aligned PWM mode.

Example 13-4: PWM Mode

```
OC1CON1 = 0;                /* It is a good practice to clear off the control bits initially */
OC1CON2 = 0;
OC1CON1bits.OCTSEL = 0x07; /* This selects the peripheral clock as the clock input to the OC
                           module */
OC1R = 1000;                /* This is just a typical number, user must calculate based on the
                           waveform requirements and the system clock */
OC1RS = 2000;               /* Determines the Period */
OC1CON1bits.OCM = 6;        /* This selects the Edge Aligned PWM mode*/
```

13.3.3.4 PWM MODE SPECIAL COMPARE CONDITIONS

Table 13-6 lists the PWM mode special compare conditions.

Table 13-6: Special Compare Mode Conditions

Special Condition	Operation	Output
OCxR = `0`	The OCx pin would be set low (see Figure 13-18).	Low
OCxR > OCxRS	The OCx pin would be set high (see Figure 13-19).	High
OCxR = OCxTMR and synchronization occurs	The OCx pin would remain high (see Figure 13-20).	High

Figure 13-18: PWM Output Timing (0% Duty Cycle, OCxR = 0x0000)

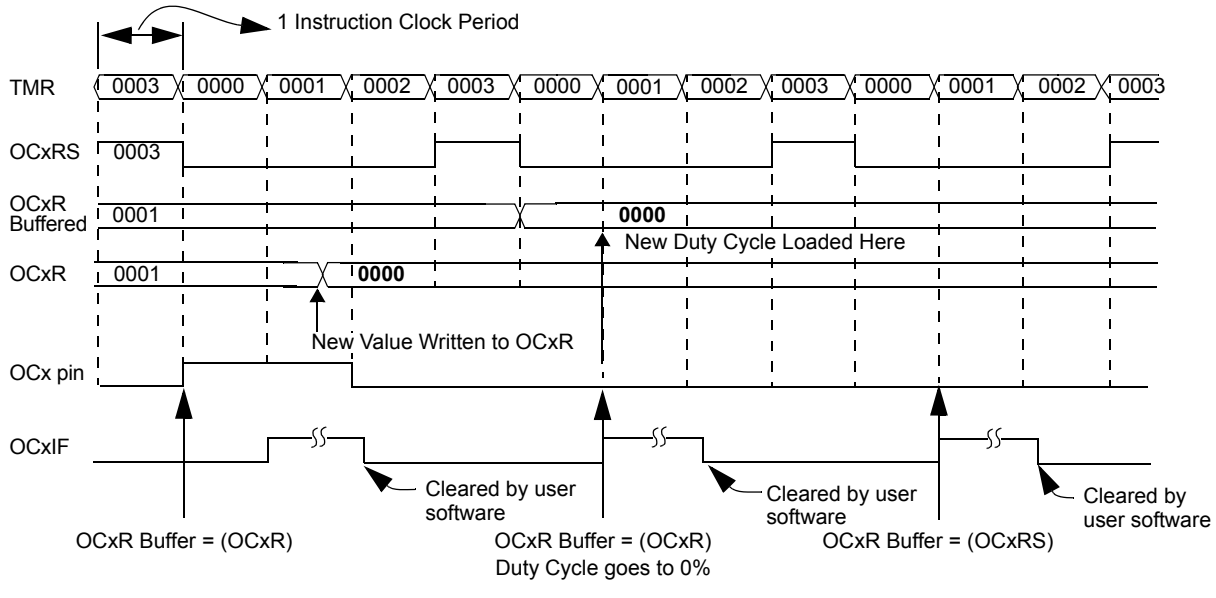


Figure 13-19: PWM Output Timing (100% Duty Cycle, OCxR > OCxRS (SYNCSEL<4:0> = 0x1F))

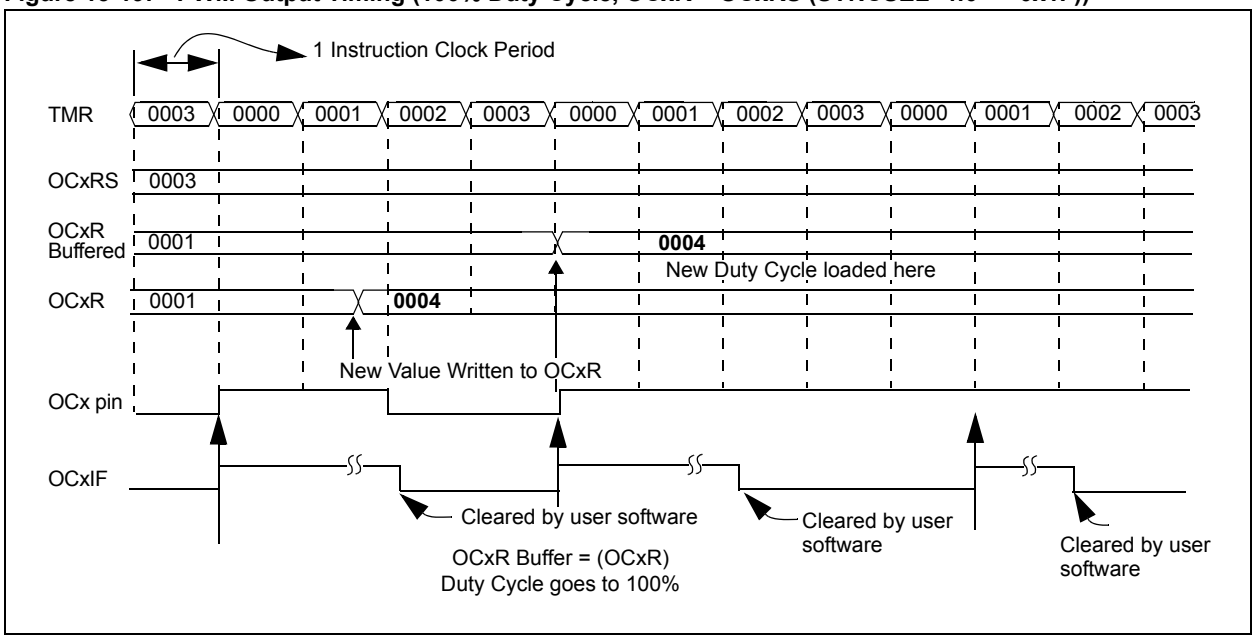
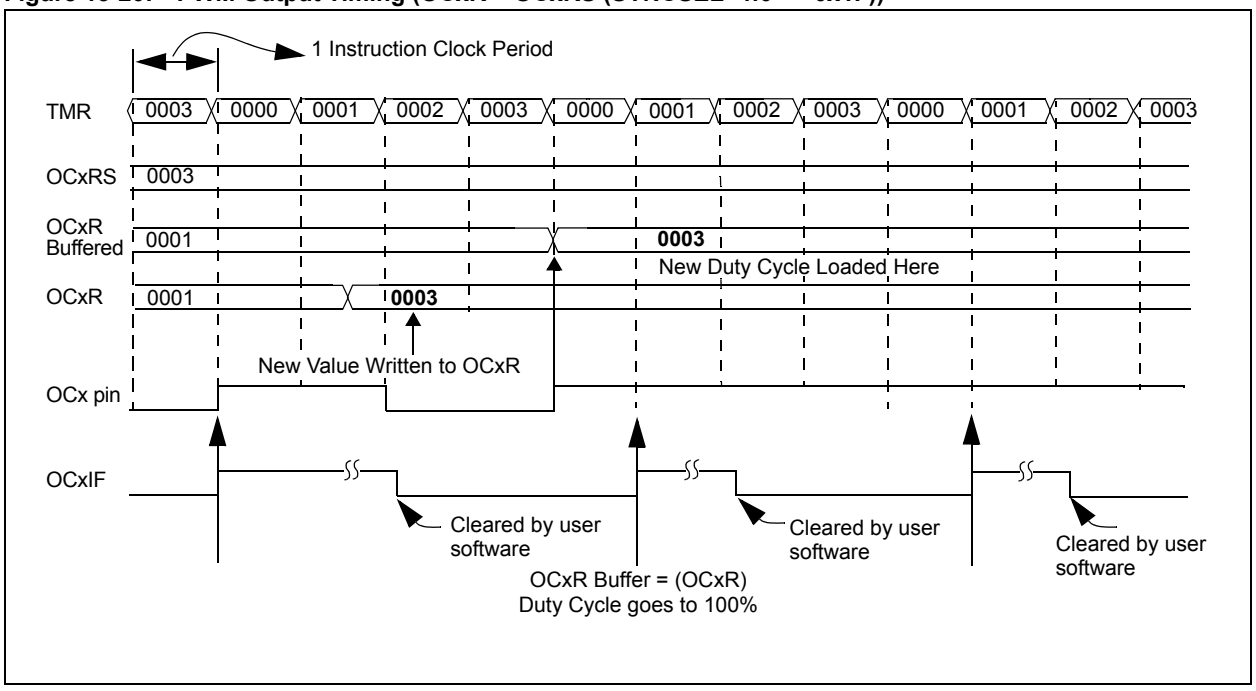


Figure 13-20: PWM Output Timing (OCxR = OCxRS (SYNCSEL<4:0> = 0x1F))



13.3.3.5 CENTER-ALIGNED PWM MODE

The Center-aligned PWM mode (OCM<2:0> = 0b111) functions the same as the Continuous Pulse mode (OCM<2:0> = 0b101). The only differences are:

- OCxR and OCxRS are double-buffered, which means that the new register value would be effective only after a timer rollover or synchronization
- Fault control and pins are used

Note 1: Center alignment does not mean the pulse is exactly aligned to the center of the pulse-width. It only indicates that the on time of the pulse can be positioned anywhere within the period.

13.3.3.6 FAULT INPUT AND CONTROL

When operating in either the Center-Aligned PWM mode or Edge-aligned PWM mode (OCM<2:0> (OCxCON1<2:0>) = 0b111 or 0b110), the Fault pin and its controls can be activated. Three Fault inputs (OCFA, OCFB and OCFC) are available. These Fault inputs are controlled by the associated ENFLTx bit (where 'x' = A, B or C) in the OCxCON1 register. If this bit is '0', the corresponding Fault input pin is ignored. The status of the Fault input can be observed in the associated OCFLTx bit (where 'x' = A, B or C) in the OCxCON1 register.

When a Fault occurs, the OCx pin output level is determined by the FLTOUT (OCxCON2<14>) bit. The tri-stating of the OCx pin during a Fault condition is controlled by FLTTRIEN (OCxCON2<13>).

The Fault control can operate in two modes based on the FLTMD (OCxCON2<15>) bit:

- Inactive mode
- Cycle-by-Cycle mode

13.3.3.6.1 Inactive Mode

When FLTMD (OCxCON2<15>) = 1, the Fault inputs operate in the Inactive mode (see Figure 13-21). If the Fault input goes active, the corresponding OCFLTx bit would be set and the module would be in the Fault condition.

It remains in the Fault condition until:

- The Fault input goes inactive
- The corresponding OCFLTx bit is cleared in software
- A new timer cycle is started (timer goes to 0000h)

13.3.3.6.2 Cycle-by-Cycle Mode

When FLTMD (OCxCON2<15>) = 0, the Fault inputs operate in the Cycle-by-Cycle mode (see Figure 13-22). If a Fault input goes active, the corresponding OCFLTx bit will be set and the module will be in the Fault condition.

It remains in the Fault condition until:

- The Fault input goes inactive
- A new timer cycle is started (timer goes to 0x0000)

Figure 13-21: Fault Input Pin Timing, Inactive Mode (OCFA Pin Example)

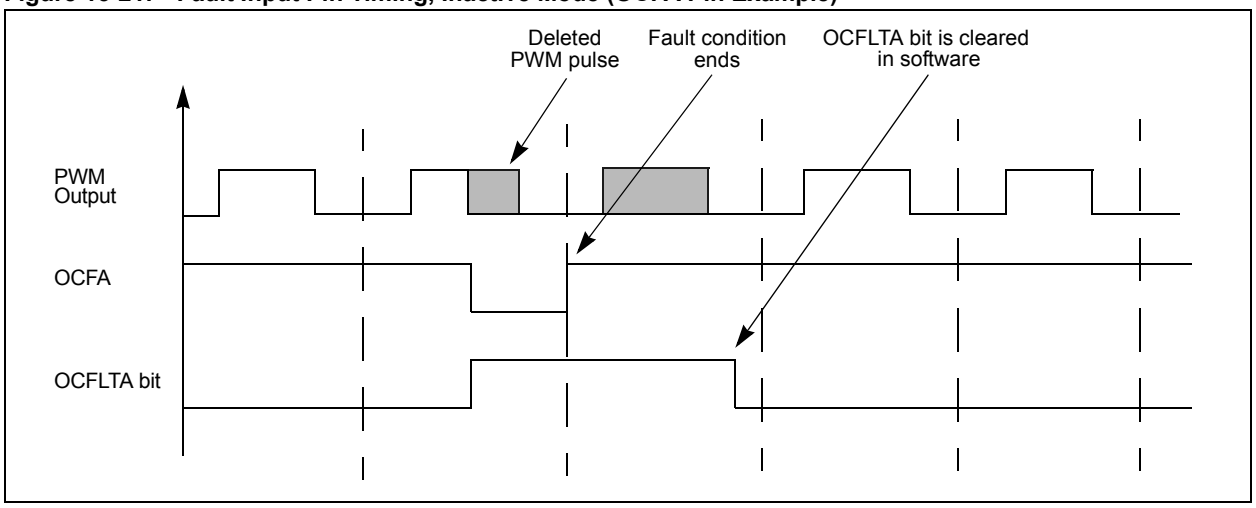
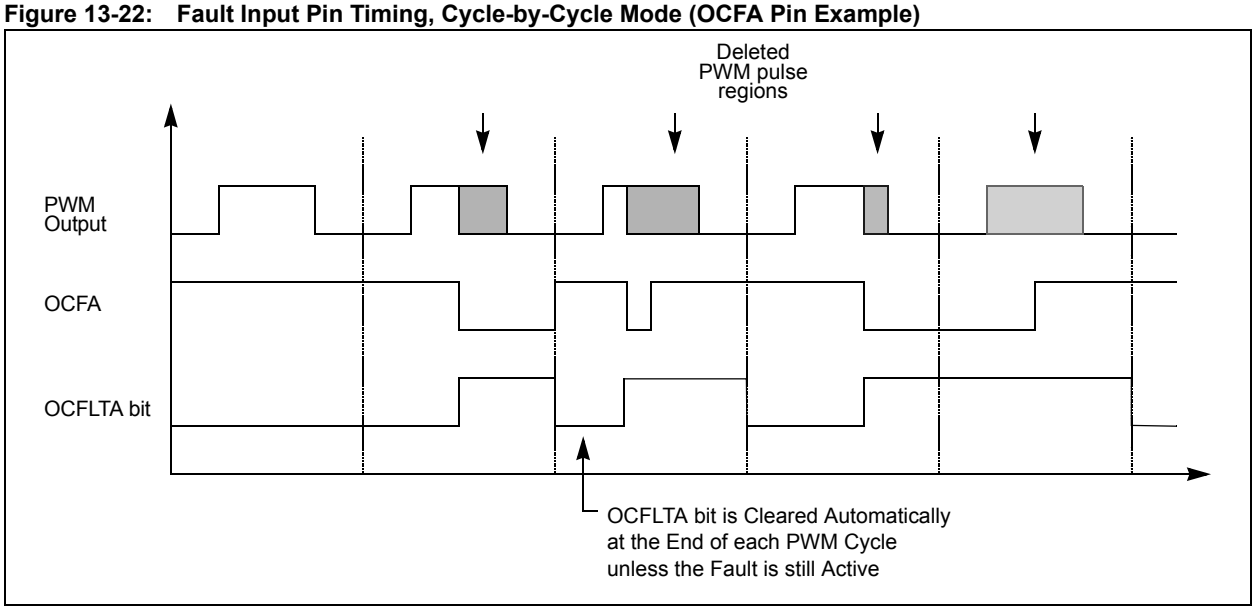


Figure 13-22: Fault Input Pin Timing, Cycle-by-Cycle Mode (OCFA Pin Example)



13.3.3.7 SYNCHRONOUS OPERATION

Synchronous operation of the timer is enabled when the OCTRIG (OCxCON2<7>) = 0.

In synchronous operation, the TRIGSTAT (OCxCON2<6>) bit has no function. The timer can be synchronized with the other modules using the synchronization/trigger inputs (see Register 13-2). Whenever the selected module receives a synchronization signal, the timer would roll over to 0x0000 on the next positive edge of the selected clock.

13.3.3.8 USE OF THE MODULE TIMER IN A SYNCHRONIZED APPLICATION

Figure 13-23 illustrates the connections for synchronization and Figure 13-24 illustrates the timing for multiple modules being synchronized. OC2 is being synchronized to OC1. The synchronization signal from OC1 is selected for synchronization by both OC1 and OC2 using the SYNCSEL<4:0>(OCxCON2<4:0>) bits. The OC1RS register now becomes the Period register for both OC1 and OC2.

When the OC1RS register matches the OC1 timer value, the OC1 module produces the synchronization signal. This causes the timers in both OC1 and OC2 to go to zero on the next positive clock edge.

Note:	Synchronized modules should select the same clock source to ensure proper function.

Figure 13-23: Synchronous Operation Integration

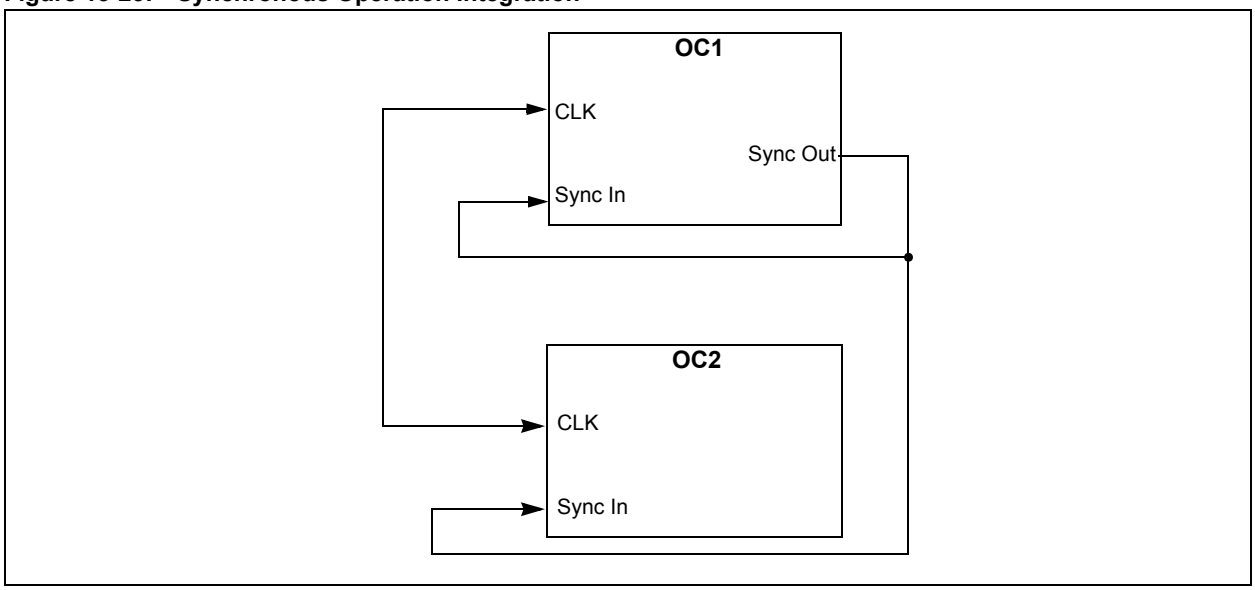
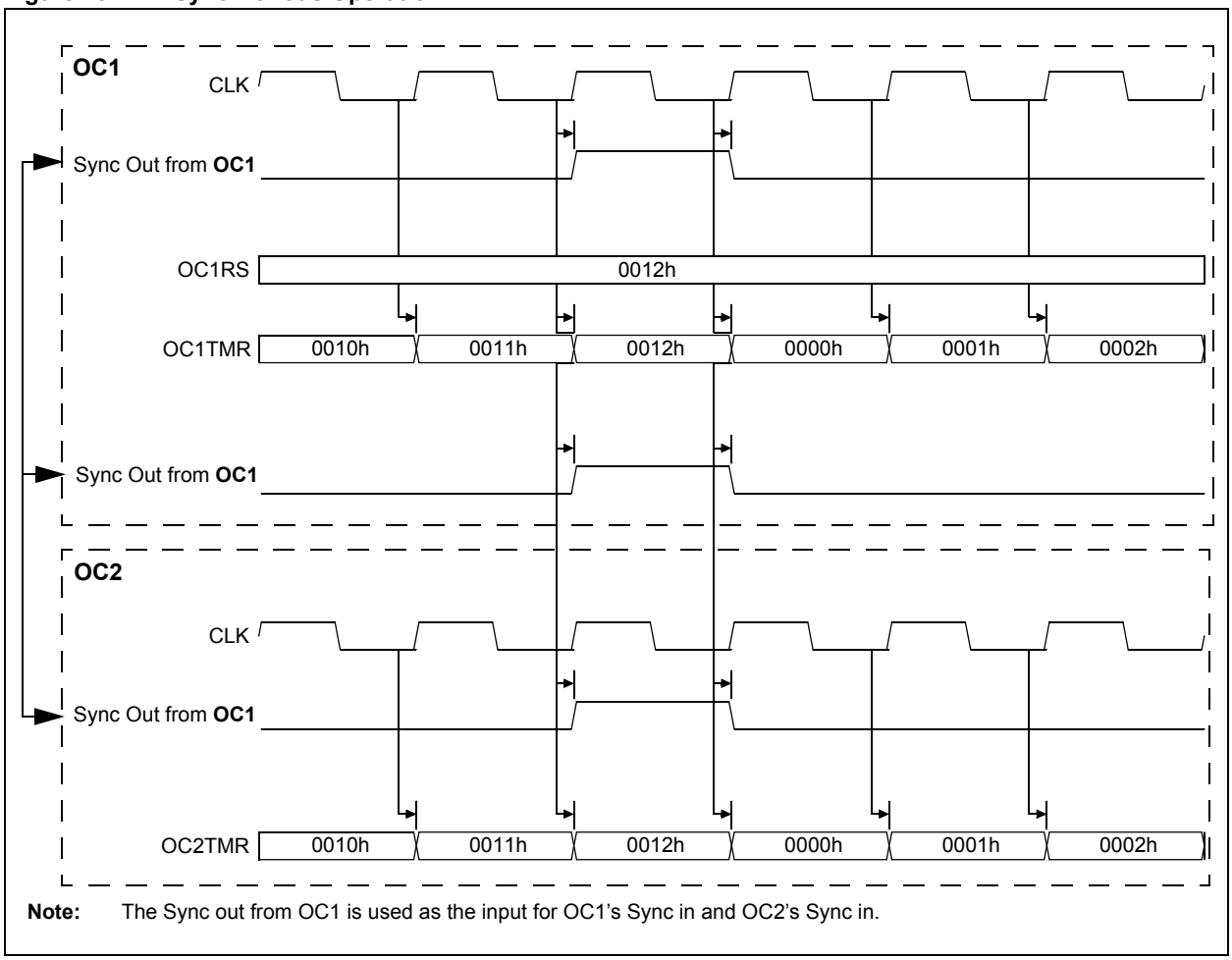


Figure 13-24: Synchronous Operation



Note: The Sync out from OC1 is used as the input for OC1's Sync in and OC2's Sync in.

When initializing synchronized modules, the module is used as the source of synchronization and it should be enabled last. As illustrated in Figure 13-23, OC2 should be initialized first and OC1 should be initialized last. This ensures that the timers of all synchronized modules are maintained in a Reset condition until the last module is initialized.

13.3.3.9 TRIGGER OPERATION

Trigger operation of the timer is enabled when OCTRIG (OCxCON2<7>) = 1. When configured for trigger operation, the module timer is held in Reset until a trigger event occurs. After the trigger event occurs, the timer begins to count. The trigger source is selected by the SYNCSEL bits.

13.3.3.10 OCxCON2 TRIGGER FUNCTION

The TRIGSTAT (OCxCON2<6>) bit holds the timer in Reset or releases it to count. It controls the timer in the following manner:

- TRIGSTAT = 0
  - Timer is held in Reset
- TRIGSTAT = 1
  - Timer released from Reset
  - Timer increments on every positive clock

There are two types of trigger conditions when operating in Trigger mode:

- Hardware/software TRIGSTAT bit set
- Software only TRIGSTAT bit set

In both cases, the trigger is always cleared in software.

13.3.3.10.1 Hardware/Software TRIGSTAT Set

The TRIGSTAT (OCxCON2<6>) bit can be set by hardware or software when:

- The SYNCSEL (OCxCON2<4:0>) bits are not equal to 0b00000 (see **13.3.3.12 "Illegal Settings"**)

When the module is enabled for a triggered response, the timer will be held in a cleared state. It remains in this cleared state until a trigger event occurs, which sets the TRIGSTAT bit. Additionally, the timer can be released from Reset by writing to the TRIGSTAT bit and setting it.

13.3.3.10.2 Software Only TRIGSTAT Set

The TRIGSTAT bit can be set only by software when SYNCSEL<4:0> = 0b00000.

13.3.3.11 CLEARING TRIGSTAT BIT

The TRIGSTAT bit can only be cleared in software by writing a '0' to it. When the TRIGSTAT bit is cleared in software, the timer is reset to 0x0000 on the next timer clock's rising edge and is ready for another trigger.

13.3.3.12 ILLEGAL SETTINGS

It is illegal for the module to select itself as a trigger source. Therefore, two possible values of the SYNCSEL<4:0> in Trigger mode are not allowed:

- SYNCSEL<4:0> = 0x1F
- SYNCSEL<4:0> = N, where N is the second setting that selects the same module (see Register 13-2).

Note 1: TRIGSTAT cannot be changed in software when operating in One-Shot mode. For more information on this mode, see **13.3.3.13.2 "One-Shot Functionality"**.

2: The trigger source will be synchronized with the OCx clock.

3: Preventing these illegal conditions should be taken care of in the user software.

13.3.3.13 USE OF THE OCx MODULE IN A TRIGGERED APPLICATION

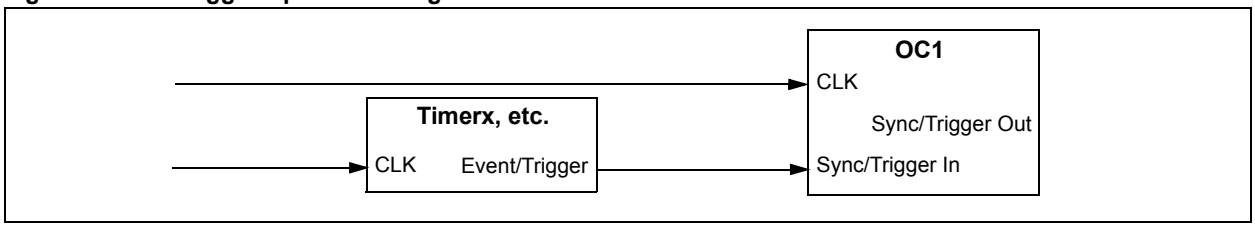
Figure 13-25 illustrates a typical application of the module timer in a triggered application. In this application, a trigger event can be generated by another output compare module, timer module, IC module, analog comparator or other peripheral functions. Refer to the product data sheet for a complete list of trigger sources.

Note:	When OCx is switched off, it sends a trigger out signal. If any other OCy module uses OCx as a trigger source, it must deselect OCx as a trigger source before OCx is switched off.

13.3.3.13.1 Initialization of the OCx Module in a Triggered Application

The user misses any trigger event that occurs before the OCx module is initialized. Therefore, to avoid missing a trigger, it is recommended that the module be enabled before the trigger source.

Figure 13-25: Trigger Operation Integration



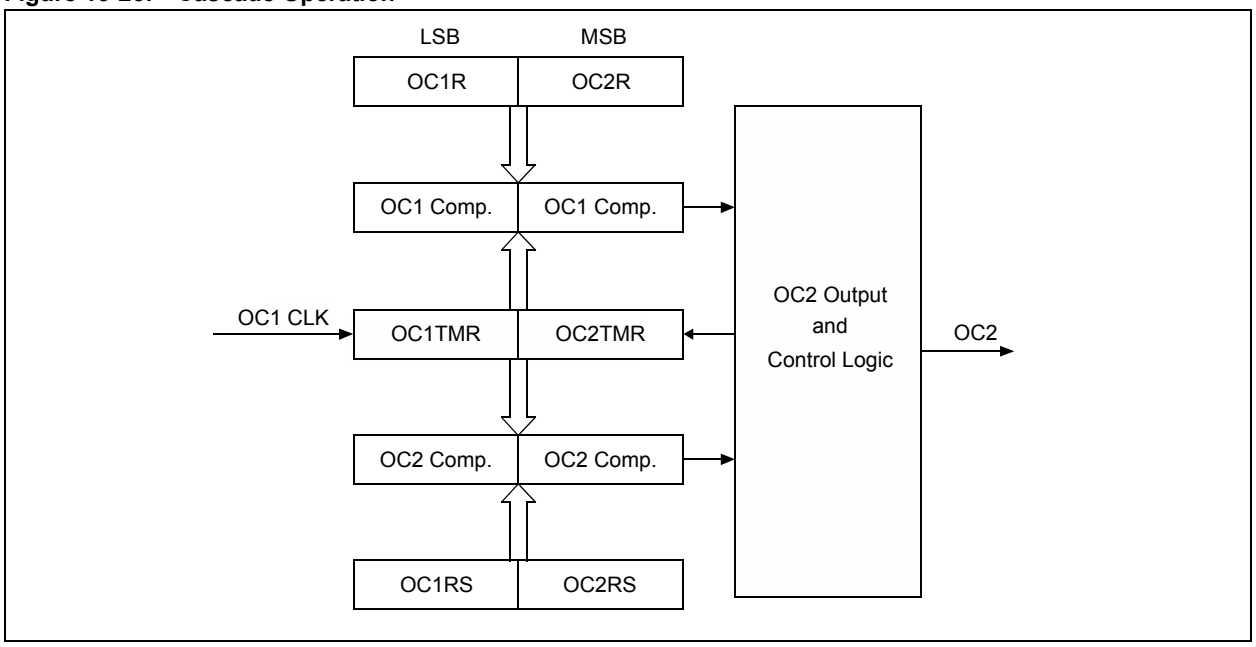
13.3.3.13.2 One-Shot Functionality

While operating as a trigger, the timer can operate in One-Shot mode. This produces one pulse for every trigger. The One-Shot mode is enabled by setting the TRIGMODE (OCxCON1<3>) bit. In One-Shot mode, the timer remains in Reset until a trigger event occurs. This event sets the TRIGSTAT bit and the timer begins to count. When the timer rolls over to 0000h, the TRIGSTAT bit would be cleared by the hardware if TRIGMODE = 1. This holds the timer in Reset until the next trigger event, creating a one-shot timer.

13.3.4 Cascade Mode

When 16-bit timers are not enough, the OCx modules can be grouped in pairs to cascade them into 32-bit timers (see Figure 13-26). They are grouped as odd and even pairs (1-2, 3-4, 5-6, etc.). When cascading, the odd OCx module forms the Least Significant 16 bits of the timer/compare and the even module forms the Most Significant 16 bits. The OCx pin of the even module would be the output of the cascaded timers.

Figure 13-26: Cascade Operation



13.3.5 Setting Up Modules for Cascade

In this section, it is assumed that OC1 is the odd OC module and OC2 is the even.

The odd module is set up as follows:

- OC32 (OC1CON1<8>) = 1
- OCTRIG (OC1CON2<7>) can either be '1' or '0' as the timer can either be synchronized or triggered
- OCTRIS (OC1CON2<5>) = 1 (since the OC1 pin would not be used, the output should be tri-stated)

The even module is set up as follows:

- OC32 (OC2CON1<8>) = 1
- OCTRIG (OC2CON2<7>) = 0 (even timer must be operated in Synchronized mode when cascaded)
- OCTRIS (OC2CON2<5>) = 0 (since OC2 would be used, the output should be enabled)

13.3.5.1 INITIALIZATION OF THE MODULES IN A CASCADE APPLICATION

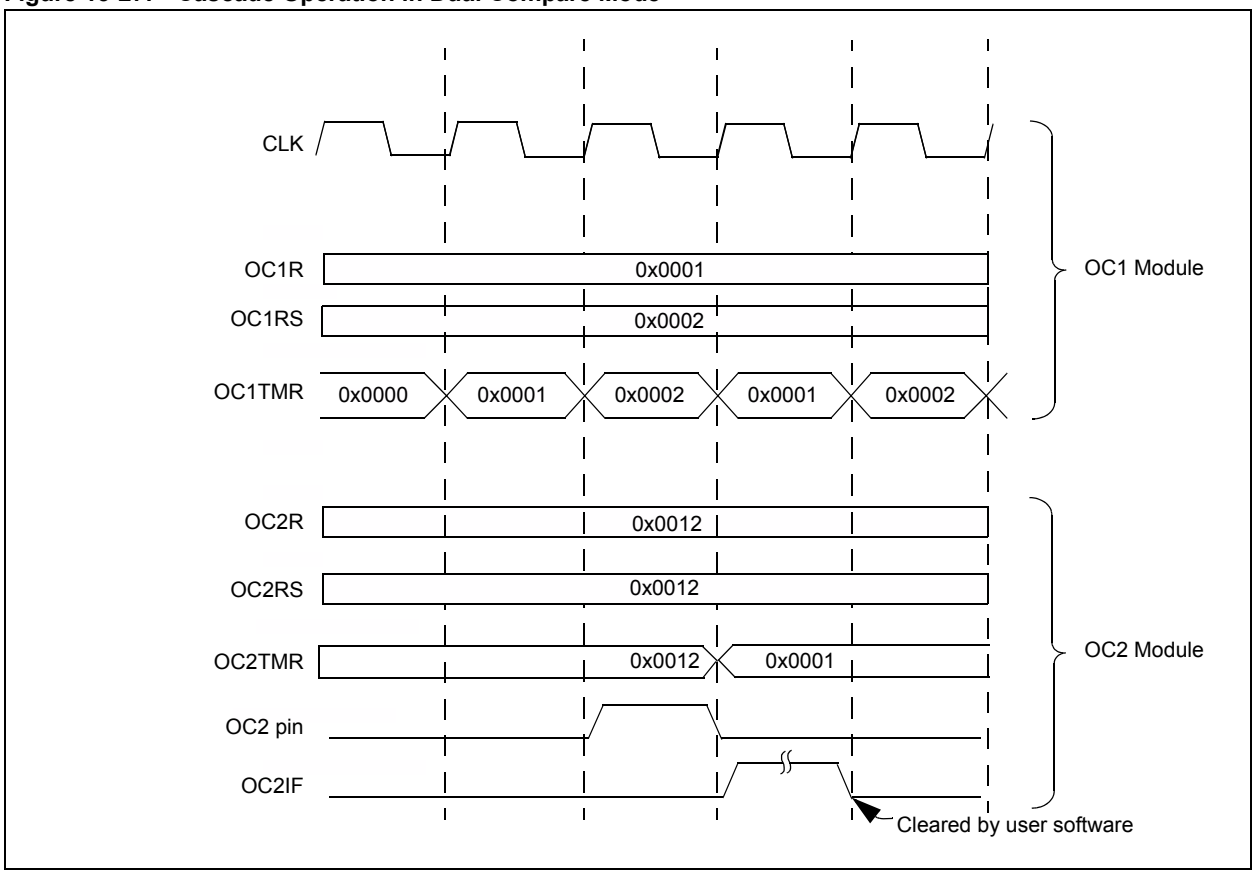
When initializing cascaded modules, the even module should be initialized first and the odd module should be initialized last.

13.3.5.2 TIMER CLOCK SELECTION

This clock should be selected before the module is enabled, and should not be changed during the operation. The waveform for the cascade operation is illustrated in Figure 13-27.

Note:	The even and odd OC modules must have the same clock.

Figure 13-27: Cascade Operation in Dual Compare Mode



13.3.5.3 CASCADE OPERATION WITH THE ODD MODULE TRIGGERED

When two modules are cascaded to form a 32-bit timer, the timer can be triggered by setting the odd module (OCTRIG = 1). The odd module remains in Reset until a trigger event occurs. After a trigger event occurs, the odd and even modules count as usual.

13.3.5.4 SYNCHRONIZING MULTIPLE CASCADED MODULE PAIRS

Multiple 32-bit pairs can also be synchronized, for example:

- To synchronize the OC3 + OC4 pair with the OC1 + OC2 pair:
  - OC1 and OC2 are set up as defined in **13.3.5 "Setting Up Modules for Cascade"**
  - OC3 and OC4 are set up in the same way, but also SYNCSEL = 1 (synchronization out from OC1); this allows the Sync out from OC1 to hold OC3 in Reset

Example 13-5: Output Compare in Cascade Mode

```
OC1CON1 = 0;              /* It is a good practice to clear off the control bits initially */
OC1CON2 = 0;
OC2CON1 = 0;
OC2CON2 = 0;

OC1CON1bits.OCTSEL = 0x07;/* This selects the peripheral clock as the clock input to the OC
                          module */
OC2CON1bits.OCTSEL = 0x07;

OC1R = 0x1000;            /* Determines the On-Time */
OC2R = 0x0002;            /* Determines the On-Time */

OC1RS = 0x2000;           /* Determines the Period */
OC2RS = 0x0003;           /* Determines the Period */

OC1CON2bits.SYNCSEL = 0x1F;
OC2CON2bits.SYNCSEL = 0x1F;

OC1CON2bits.OCTRIS = 1;   /* Odd module's output is not required */


/* Even module must be enabled first */
/* Odd module must be enabled last */

OC2CON2bits.OC32 = 1;
OC1CON2bits.OC32 = 1;

OC2CON1bits.OCM = 6;      /* This selects the Edge Aligned PWM mode */
OC1CON1bits.OCM = 6;
```

13.4 OUTPUT COMPARE OPERATION WITH DMA

Some dsPIC33E/PIC24E family devices include a Direct Memory Access (DMA) module, which allows data transfer from data memory to the Output Compare module without CPU intervention. Refer the specific dsPIC33E/PIC24E device data sheet to see if DMA is present on your device. For more information on the DMA module, refer to **Section 22. Direct Memory Access (DMA)**.

The DMA channel must be initialized with the following:

- Initialize the DMA Channel Peripheral Address (DMAxPAD) register with the address of the Output Compare (OCxR) register or the Secondary Output Compare (OCxRS) register.
- Set the Transfer Direction (DIR) bit in the DMA Control (DMAxCON<13>) register. In this condition, data is read from the dual port DMA memory and written to the peripheral Special Function Register.
- The DMA Request Source Selection (IRQSEL<7:0>) bits in the DMA Request (DMAxREQ<7:0>) register must select the DMA transfer request source.

Example 13-6 provides sample code that modulates the PWM duty cycle without CPU intervention. The duty cycle values stored in an array are transferred to OCxRS register on every timer interrupt.

Example 13-6: Code to Modulate the PWM Duty Cycle without CPU Intervention

```
//Define Buffer in DMA RAM as global variable:
__eds__ unsigned int BufferA[256] __attribute__((space(eds)));

//initialize buffer with duty cycle values
    int i;
    for(i=0;i<256;i++)
    BufferA[i]=i;
//Initialize Output Compare Module in PWM mode
    OC1CON1bits.OCM = 0b000;          // Disable Output Compare Module
    OC1R=100;                         // Write the duty cycle for the PWM pulse
    OC1RS=255;                        // Write the PWM frequency
    OC1CON1bits.OCTSEL = 0;           // Select Timer2 as output compare time base
    OC1CON1bits.OCM = 0b110;          // Select the Output Compare mode
    OC1CON2bits.SYNCSEL=31;           // OC2RS compare event is used for synchronization

// Initialize Timer2
    T2CONbits.TON = 0;                // Disable Timer
    T2CONbits.TCS = 0;                // Select internal instruction cycle clock
    T2CONbits.TGATE = 0;              // Disable Gated Timer mode
    T2CONbits.TCKPS = 0b00;           // Select 1:1 Prescaler
    TMR2 = 0x00;                      // Clear timer register
    PR2 = 500;                        // Load the period value

// Set up and Enable DMA Channel
    DMA0CONbits.AMODE = 0b00;         // Register indirect with post increment
    DMA0CONbits.MODE = 0b00;          // Continuous, Ping-Pong mode Disabled
    DMA0CONbits.DIR = 1;              // Peripheral to RAM
    DMA0PAD = (int)&OC1R;             // Address of the output compare register
    DMA0REQ = 7;                      // Select Timer2 interrupt as DMA request source
    DMA0CNT = 255;                    // Number of words to buffer.

    DMA0STAH = __builtin_dmapage (&BufferA);
    DMA0STAL = __builtin_dmaoffset (&BufferA);

    IFS0bits.DMA0IF = 0;              // Clear the DMA interrupt flag
    IEC0bits.DMA0IE = 1;              // Enable DMA interrupt
    DMA0CONbits.CHEN = 1;             // Enable DMA channel

// Enable Timer
    T2CONbits.TON = 1;                // Start Timer

//Set up DMA Interrupt Handler:

    void __attribute__((__interrupt__,no_auto_psv)) _DMA0Interrupt(void)
    {
    // Process the captured values
    IFS0bits.DMA0IF = 0;              // Clear the DMA0 Interrupt Flag
}
```

13.5 OUTPUT COMPARE OPERATION IN POWER-SAVING STATES

13.5.1 Output Compare Operation in Sleep Mode

When the device enters Sleep mode, the system clock is disabled. During Sleep mode, the output compare channel drives the pin to the same active state as it was driven prior to entering the Sleep state. The module then Halts at this state.

For example:

If the pin was high and the CPU enters the Sleep state, the pin stays high. Similarly, if the pin was low and the CPU enters the Sleep state, the pin stays low. In both the cases, when the device awakes, the output compare module resumes operation.

13.5.2 Sleep with PWM Fault Mode

- When the module is in PWM Fault mode, the asynchronous portions of the Fault circuit remain active.
- If a Fault is detected, the output of the OCx pin is determined by the FLTOUT and the OCTRIS setting of OCxCON2 register.
- The corresponding OCFLTx bit will be set. An interrupt would not be generated at a Fault occurrence. However, the interrupt will be queued and occurs at the time the part wakes up.

13.5.3 Output Compare Operation in Idle Mode

When the device enters Idle mode, the system clock sources remain functional and the CPU stops executing code. The OCSIDL (OCxCON1<13>) bit selects if the output capture module stops in Idle mode or continues operation in Idle mode.

- If OCSIDL = 1, the module discontinues the operation in Idle mode. The module performs the same procedures when stopped in the Idle mode (OCSIDL = 1) as it does for the Sleep mode.
- If OCSIDL = 0, the output compare channel(s) operate during the CPU Idle mode if the OCSIDL bit is a logic '0'. Furthermore, the time base must be enabled with the respective TSIDL bit set to a logic '0'; if internal, the timer is used as the clock source.

Note:	The external Fault pins, if enabled for use, continue to control the associated OCx output pins while the device is in Sleep or Idle mode.

13.5.4 Doze Mode

Output compare operation in Doze mode is the same as in normal mode. When the device enters Doze mode, the system clock sources remain functional and the CPU may run at a slower clock rate.

13.5.5 Selective Peripheral Module Control

The Peripheral Module Disable (PMD) registers provide a method to disable the output compare module by stopping all the clock sources supplied to it. When the module is disabled through the appropriate PMD control bit, it is in minimum power consumption state. The control and status registers associated with the module will also be disabled. Therefore, a write to these registers would have no effect, and the read values would be invalid and return zero.

13.6 I/O PIN CONTROL

When the output compare module is enabled, the I/O pin direction is controlled by the compare module. The compare module returns the I/O pin control back to the appropriate LAT and TRIS control bits when it is disabled. When the Simple PWM with Fault Protection Input mode is enabled, the Fault pins must be configured as an input by setting the respective TRIS bit. Enabling this special PWM mode does not configure the Fault pins as an input.

Note:	Refer to the product data sheet for available output compare pins.

13.7 REGISTER MAPS

A summary of the registers associated with the dsPIC33E/PIC24E Output Compare module is provided in Table 13-7.

Table 13-7: Output Compare Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OCxCON1	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OCxCON2	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	DCB<1:0>		OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OCxRS	Output Compare x Secondary Register																xxxx
OCxR	Output Compare x Register																xxxx
OCxTMR	Timer Value x Register																xxxx

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

13.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33E/PIC24E device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Output Compare module are:

Title	Application Note #
No related application notes are available.	N/A

Note: Visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33E/PIC24E family of devices.

13.9 REVISION HISTORY

Revision A (November 2008)

This is the initial released revision of this document.

Revision B (July 2010)

This revision includes the following updates:

- Updated the bit value definitions for the OCTSEL<2:0> bits in the OCxCON1 register (Register 13-1)
- Updated the bit value definitions for the SYNCSEL<4:0> bits and added Note 1 and the DCB<1:0> bits in the OCxCON2 register (Register 13-2)
- Updated the default reset values to R/W-x for all bits in the OCxR and OCxRS registers (Register 13-3 and Register 13-4)
- Updated the Synchronous Operation Integration diagram (Figure 13-23)
- Added a shaded note to **13.3.3.13 “Use of the OCx Module in a Triggered Application”**
- Updated the Code to Modulate the PWM Duty Cycle without CPU Intervention code example (Example 13-6)
- Updated the All Reset values for the OCxCON2, OCxRS, and OCxR registers in the register map (Table 13-7)
- Removed the “Design Tips” section

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

ISBN: 978-1-60932-402-5

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/05/10