
Section 32. Analog Comparator

HIGHLIGHTS

This section of the manual contains the following major topics:

32.1	Introduction	32-2
32.2	Features Overview	32-2
32.3	Module Description	32-3
32.4	Control Registers	32-4
32.5	Configuring the SMPS Comparator	32-6
32.6	Application Information	32-7
32.7	SMPS Comparator Limitations	32-8
32.8	Related Application Notes	32-10
32.9	Revision History	32-11

32.1 INTRODUCTION

The dsPIC[®] Switch Mode Power Supply (SMPS) Analog Comparator module in the dsPIC30F SMPS and Digital Power Conversion device family provides a way to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC SMPS device processor and/or peripherals without requiring any additional resources, frees the dsPIC SMPS device to perform other tasks.

The SMPS Comparator module contains up to four high-speed analog comparators with dedicated 10-bit digital-to-analog converters (DACs) that provide a programmable reference voltage to one input of the comparator.

32.2 FEATURES OVERVIEW

The following is a list of key features of the SMPS Comparator module:

- Up to 4 analog comparators
- Dedicated 10-bit DAC for each analog comparator
- Programmable output polarity
- Interrupt generation capability
- Up to 16 selectable input sources
- Multiple voltage references for the DAC:
 - $AV_{DD}/2$
 - Internal Reference $1.2V \pm 1\%$
 - External Reference $< (AV_{DD} - 1.6V)$
- ADC sample and convert trigger capability
- Ability to disable the comparator module to reduce power consumption
- Functional support for Power Supply PWM module, which includes:
 - PWM Duty Cycle Control
 - PWM Period Control
 - PWM Fault Detect

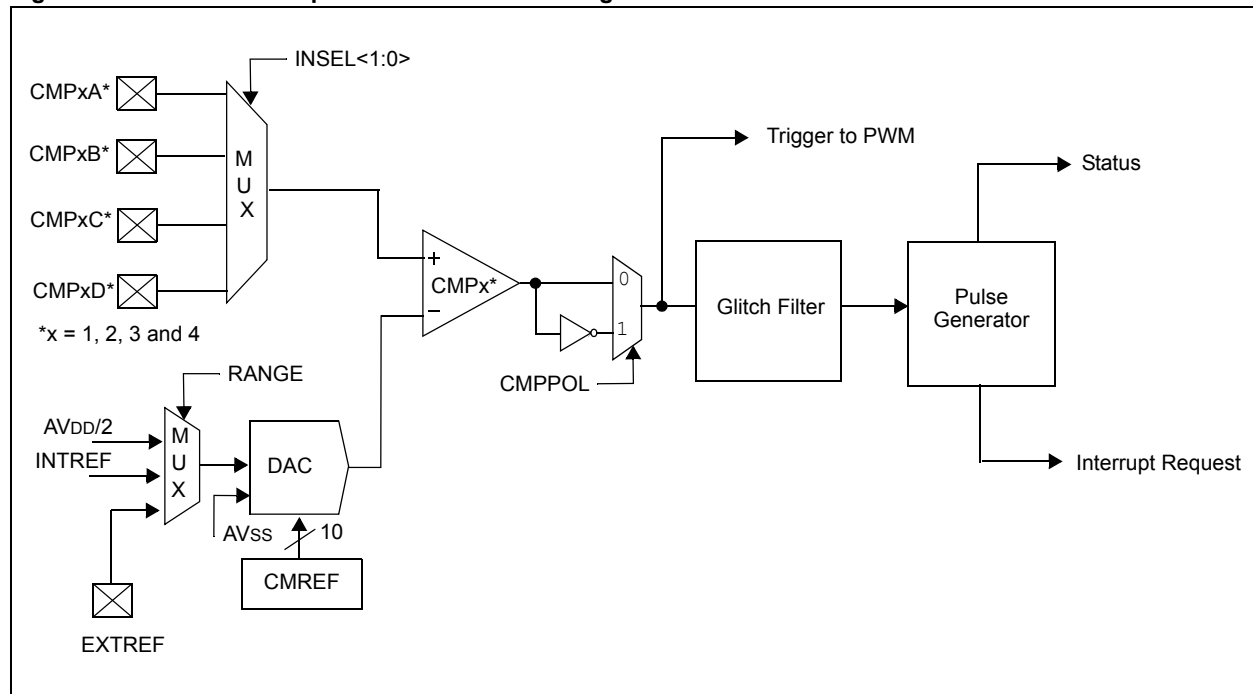
32.3 MODULE DESCRIPTION

Figure 32-1 shows a functional block diagram of one analog comparator from the SMPS Comparator module.

The analog comparator provides high speed operation with a typical delay of 20 ns. The comparator has a typical offset voltage of ± 5 mV. The negative input of the comparator is always connected to the DAC circuit. The positive input of the comparator is connected to an analog multiplexer that selects the desired source pin.

The analog comparator input pins are typically shared with pins used by the analog-to-digital converter (ADC) module. Both the comparator and the ADC can use the same pins at the same time. This capability enables a user to measure an input voltage with the ADC and detect voltage transients with the comparator.

Figure 32-1: SMPS Comparator Module Block Diagram



32.4 CONTROL REGISTERS

The following registers are used to configure the SMPS Comparator module:

- **Comparator Control Register x (CMPCONx)**
This register is used to configure the comparator voltage reference source, input pin and output polarity. Depending on the device variant, there are up to four individual registers (CMPCON1-CMPCON4), which correspond to the respective comparator.
- **Comparator DAC Control Register x (CMPDACx)**
The contents of this register determine the threshold voltage for the comparator. Depending on the device variant, there are up to four individual registers (CMPDAC1-CMPDAC4), which correspond to the respective comparator.

Register 32-1: Comparator Control Register x (CMPCONx)

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
CMPON	—	CMPSIDL	—	—	—	—	—
bit 15				bit 8			

Lower Byte:							
R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
INSEL[1:0]		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE
bit 7				bit 0			

- bit 15 **CMPON:** Comparator A/D Operating Mode bit
1 = Comparator module is enabled
0 = Comparator module is disabled (reduces power consumption)
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CMPSIDL:** Comparator Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode
- If a device has multiple comparators, any CMPSIDL bit set to '1' will disable all comparators while in Idle mode.
- bit 12-8 **Reserved:** Read as '0'
- bit 7-6 **INSEL[1:0]:** Comparator Input Source Select bit
00 = Select CMPxA input pin
01 = Select CMPxB input pin
10 = Select CMPxC input pin
11 = Select CMPxD input pin
- bit 5 **EXTREF:** External Reference Enable bit
1 = External source provides reference to DAC (maximum DAC voltage determined by external voltage source)
0 = Internal reference sources provide reference to DAC (maximum DAC voltage determined by RANGE bit setting)
- bit 4 **Reserved:** Read as '0'
- bit 3 **CMPSTAT:** Current state of comparator output including CMPPOL selection
- bit 2 **Reserved:** Read as '0'
- bit 1 **CMPPOL:** Comparator Output Polarity Control bit
1 = Output is inverted
0 = Output is not inverted
- bit 0 **RANGE:** DAC Output Voltage Range bit
1 = High range: Max DAC value = $AV_{DD}/2$ (2.5V @ 5V V_{DD} , or 1.65V @ 3.3V V_{DD})
0 = Low range: Max DAC value = INTREF (1.2V $\pm 1\%$)

Legend:	HC = Clear by Hardware	HS = Set by Hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared
		x = bit is unknown

Register 32-2: Comparator DAC Control Register x (CMPDACx)

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	CMREF[9:8]	
bit 15						bit 8	

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMREF[7:0]							
bit 7				bit 0			

bit 15-10 **Reserved:** Read as '0'

bit 9-0 **CMREF[9:0]:** Comparator Reference Voltage Select bits

1111111111 = (CMREF * INTREF/1024) or (CMREF * (AVDD/2)/1024) volts depending on RANGE bit, or
(CMREF * EXTREF/1024) if EXTREF bit is set

.
. .
. .

0000000000 = 0.0 volts

Legend:	HC = Clear by Hardware	HS = Set by Hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared x = bit is unknown

32.5 CONFIGURING THE SMPS COMPARATOR

The SMPS Comparator module is configured using the CMPCONx register. The INSEL<1:0> bits are used to select the comparator input pin. The signal to be monitored must be connected to this pin.

The EXTREF bit in the CMPCONx register selects between an external reference source or the internal reference source. If the EXTREF bit is set (CMPCONx<5> = 1), then the voltage applied to the EXTREF pin provides the comparator reference voltage.

If the EXTREF bit is cleared (CMPCONx<5> = 0), the RANGE bit (CMPCONx<0>) in the CMPCONx register determines the comparator reference voltage. If Low Range is selected (CMPCONx<0> = 0), the internal band gap reference (INTREF) provides the comparator reference. If High Range is selected (CMPCONx<0> = 1), AVDD/2 provides the comparator reference.

32.5.1 10-bit DAC

Each analog comparator in the SMPS Comparator module has a dedicated 10-bit DAC that is used to program the comparator threshold voltage.

The full range of the DAC (AVDD/2) will typically be used when the chosen input source pin is shared with an ADC input.

The reduced range option (INTREF) is typically used when monitoring currents via a current sense shunt resistor. Usually, the measured voltages in such applications are small (< 1.25V); therefore, the option of using a reduced reference range for the comparator extends the available DAC resolution in these applications.

The use of an external reference enables the user to connect to a reference that better suits their application.

32.5.2 Interaction with Digital I/O Pin Buffers

If the comparator module is enabled and a pin has been selected as the source for the comparator, then the digital input buffer associated with that pin will be disabled. This is done to prevent excessive currents in the digital buffer due to analog input voltages.

32.5.3 Glitch Filter

The SMPS Comparator module provides a glitch filter for the comparator output to mask transient signals less than two instruction cycles in duration. In Sleep or Idle mode, the glitch filter is bypassed to enable an asynchronous signal from the comparator to the interrupt controller. This asynchronous signal can be used to wake up the processor from Sleep or Idle mode.

32.5.4 Operation in Sleep and Idle Modes

The comparator can be disabled while in Idle mode if the CMPSIDL bit in the CMPCONx register is set (CMPCONx<13> = 1). Setting the CMPSIDL bit for any one of the comparators causes the entire SMPS Comparator module to be disabled while in Idle mode.

If the SMPS Comparator module is disabled (CMPCONx<15> = 0), all of the analog comparators and the DACs are disabled to reduce power consumption.

32.6 APPLICATION INFORMATION

The SMPS Comparator module provides high-speed analog comparators that can be used in many power conversion applications. The outputs of the SMPS Comparator module can be used to perform the following functions:

- Generate an interrupt
- Trigger an ADC sample and convert process
- Truncate the PWM signal (current limit)
- Truncate the PWM period (current reset)
- Disable the PWM outputs (fault – latch)

The output of the SMPS Comparator module can be used in multiple modes at the same time. For example, comparator output can be used to generate an interrupt, have the ADC take a sample and convert it, and truncate the PWM output, all in response to a voltage being detected beyond its expected value.

The comparator can also be used to wake up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

The potential applications of the SMPS Comparator module are numerous and varied. The following sections describe some typical applications in power conversion circuits.

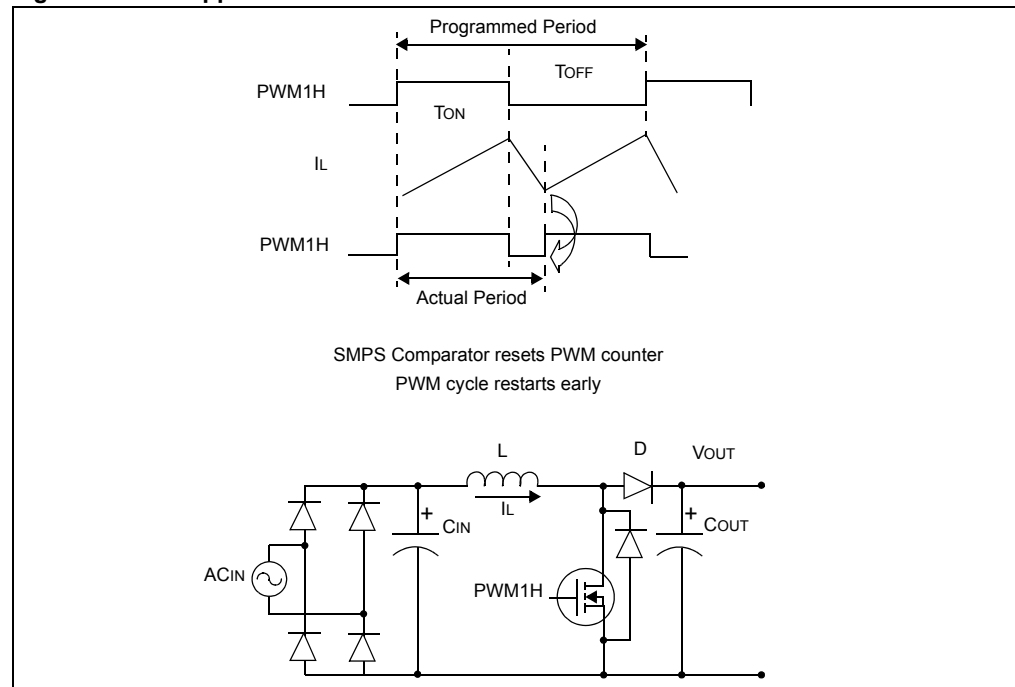
32.6.1 Power Factor Correction Boost Converter: PWM Reset Using SMPS Comparator

Analog comparators are widely used in a Power Factor Correction Boost Converter as shown in Figure 32-2. The SMPS Comparator module can be utilized for this application instead of adding expensive circuitry. The SMPS Comparator is used in conjunction with the Power Supply PWM module to generate the Current Reset mode PWM signal. For more information on this PWM mode of operation, refer to **Section 30: “Power Supply PWM”**.

The SMPS Comparator is configured to reset the PWM module when the measured current through the inductor falls below the minimum acceptable current level. This minimum current level is determined by the application.

Initially, the power semiconductor switch is turned ON. After a constant ON time, the switch is turned OFF and the PWM module waits for the current to decay below the comparator threshold. When the current falls below the threshold, the comparator resets the PWM module, turning the power semiconductor switch back ON and thereby energizing the inductor again.

Figure 32-2: Application of Current Reset PWM Mode



32.7 SMPS COMPARATOR LIMITATIONS

32.7.1 Comparator Input Range

The analog comparator has a limitation for the input Common Mode Range (CMR) of $(AV_{DD} - 1.5V)$ typical. This means that both inputs to the comparator (the chosen CMPx input pin and the selected reference source) should be within this range. As long as one of the inputs is within the Common Mode Range, the comparator output will be correct. However, any input exceeding the CMR limitation will cause the comparator input to be saturated.

If both inputs exceed the CMR, the comparator output will be indeterminate.

32.7.2 DAC Output Range

The maximum reference voltage input to the DAC should not exceed $(AV_{DD} - 1.6V)$. If the external reference voltage input exceeds this value, the reference DAC output will become indeterminate.

32.7.3 EXTREF Range

If EXTREF is selected as the comparator reference source, the voltage at the EXTREF pin should not exceed $(AV_{DD} - 1.5V)$. If the voltage at EXTREF exceeds this value, the comparator output can become unpredictable.

Table 32-1: Analog Comparator Control Register Map

File Name	ADR	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMPCON1	04C0	CMPON	—	CMPSIDL	—	—	—	—	—	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC1	04C2	—	—	—	—	—	—	CMREF<9:0>										0000
CMPCON2	04C4	CMPON	—	CMPSIDL	—	—	—	—	—	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC2	04C6	—	—	—	—	—	—	CMREF<9:0>										0000
CMPCON3	04C8	CMPON	—	CMPSIDL	—	—	—	—	—	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC3	04CA	—	—	—	—	—	—	CMREF<9:0>										0000
CMPCON4	04CC	CMPON	—	CMPSIDL	—	—	—	—	—	INSEL<1:0>		EXTREF	—	CMPSTAT	—	CMPPOL	RANGE	0000
CMPDAC4	04CE	—	—	—	—	—	—	CMREF<9:0>										0000

32.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC SMPS device Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Analog Comparator module include the following:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC SMPS family of devices.

32.9 REVISION HISTORY

Revision A (February 2007)

This is the initial released revision of this document.

Revision B (February 2007)

Minor edits throughout document.

NOTES: