

---

## Section 24. Device Configuration

---

### HIGHLIGHTS

This section of the manual contains the following topics:

24.1	Introduction .....	24-2
24.2	Device Configuration Registers .....	24-2
24.3	Configuration Bit Descriptions.....	24-9
24.4	Device Identification Registers.....	24-10
24.5	Related Application Notes.....	24-11
24.6	Revision History .....	24-12

## 24.1 Introduction

The device Configuration registers allow each user to customize certain aspects of the device to fit the needs of the application. Device Configuration registers are nonvolatile memory locations in the program memory map that hold settings for the dsPIC<sup>®</sup> DSC device during power-down. The Configuration registers hold global setup information for the device, such as the oscillator source, Watchdog Timer mode and code protection settings.

The device Configuration registers are mapped in program memory locations, starting at address 0xF80000 and are accessible during normal device operation. This region is also referred to as “configuration space”.

The Configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’) to select various device configurations.

## 24.2 Device Configuration Registers

Each device Configuration register is a 24-bit register, but only the lower 16 bits of each register are used to hold configuration data. There are seven device Configuration registers available to the user (**Note 1**):

- FOSC: Oscillator Configuration Register (**Note 2**) (0xF80000)
- FWDT: Watchdog Timer Configuration Register (0xF80002)
- FBORPOR: BOR and POR Configuration Register (0xF80004)
- FBS: Boot Segment Configuration Register (0xF80006)
- FSS: Secure Segment Configuration Register (0xF80008)
- FGS: General Segment Configuration Register (0xF8000A)
- FICD: In-Circuit Debugger Configuration Register (0xF8000C)

The device Configuration registers can be programmed using Run-Time Self-Programming (RTSP), In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>), or by a device programmer.

**Note 1:** Not all device Configuration bits shown in the subsequent Configuration register descriptions may be available on a specific device. Refer to the device data sheet for more information.

**2:** dsPIC30F devices in the General Purpose, Sensor and Motor Control families feature one of three versions of the Oscillator system – Version 1, Version 2 and Version 3. For information on the Configuration bits of the FOSC device Configuration register available in each of these versions, please refer to **Section 7. “Oscillator”**.

## Section 24. Device Configuration

**Register 24-1: FWDT: Watchdog Timer Configuration Register**

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
R/P	U	U	U	U	U	U	U
FWDTEN	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:								
U	U	R/P	R/P	R/P	R/P	R/P	R/P	
—	—	FWPSA<1:0>		FWPSB<3:0>				
bit 7								bit 0

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **FWDTEN:** Watchdog Enable Configuration bit

1 = Watchdog Enabled (LPRC oscillator cannot be disabled by clearing the SWDTEN bit in the RCON register. Will have no effect.)

0 = Watchdog Disabled (LPRC oscillator can be disabled by clearing the SWDTEN bit in the RCON register.)

bit 14-6 **Unimplemented:** Read as '0'

bit 5-4: **FWPSA<1:0>:** Prescale Value Selection for Watchdog Timer Prescaler A bits

11 = 1:512

10 = 1:64

01 = 1:8

00 = 1:1

bit 3-0: **FWPSB<3:0>:** Prescale Value Selection for Watchdog Timer Prescaler B bits

1111 = 1:16

1110 = 1:15

•

•

•

0001 = 1:2

0000 = 1:1

**Legend:**

R = Readable bit

W = Writable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

# dsPIC30F Family Reference Manual

**Register 24-2: FBORPOR: BOR and POR Configuration Register**

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23				bit 16			

Middle Byte:							
R/P	U	U	U	U	R/P	R/P	R/P
MCLREN	—	—	—	—	PWMPIN	HPOL	LPOL
bit 15				bit 8			

Lower Byte:							
R/P	U	R/P	R/P	U	U	R/P	R/P
BOREN	—	BORV<1:0>		—	—	FPWRT<1:0>	
bit 7				bit 0			

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **MCLREN:** MCLR Pin Function Enable bit  
1 = Pin function is MCLR (default case)  
0 = Pin is disabled

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **PWMPIN:** Motor Control PWM Module Pin Mode bit  
1 = PWM module pins controlled by PORT register at device Reset (tri-stated)  
0 = PWM module pins controlled by PWM module at device Reset (configured as output pins)

bit 9 **HPOL:** Motor Control PWM Module High Side Polarity bit  
1 = PWM module high-side output pins have active-high output polarity  
0 = PWM module high-side output pins have active-low output polarity

bit 8 **LPOL:** Motor Control PWM Module Low Side Polarity bit  
1 = PWM module low-side output pins have active-high output polarity  
0 = PWM module low-side output pins have active-low output polarity

bit 7 **BOREN:** PBOR Enable bit  
1 = PBOR Enabled  
0 = PBOR Disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **BORV<1:0>:** Brown-out Voltage Select bits  
11 = 2.0V  
10 = 2.7V  
01 = 4.2V  
00 = 4.5V

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **FPWRT<1:0>:** Power-on Reset Timer Value Selection bits  
11 = PWRT = 64 ms  
10 = PWRT = 16 ms  
01 = PWRT = 4 ms  
00 = Power-up timer disabled

**Note:** PWMPIN, HPOL and LPOL Configuration bits are only available on devices that feature a Motor Control PWM module.

Legend:			P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

**Register 24-3: FBS: Boot Segment Configuration Register**

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23				bit 16			

Middle Byte:							
U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
—	—	RBS<1:0>		—	—	—	EBS
bit 15				bit 8			

Lower Byte:							
U-0	U-0	U-0	U-0	R/P	R/P	R/P	R/P
—	—	—	—	BSS<2:0>			BWRP
bit 7				bit 0			

bit 23-14 **Unimplemented:** Read as '0'

bit 13-12 **RBS<1:0>:** Boot Segment RAM Code Protection bits<sup>(1)</sup>

- 11 = No Boot RAM Segment
- 10 = Small Boot RAM Segment
- 01 = Medium Boot RAM Segment
- 00 = Large Boot RAM Segment

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **EBS:** Boot Segment Data EEPROM Code Protection bit

- 1 = No Boot Data EEPROM Segment
  - 0 = Boot Data EEPROM Segment is 256 bytes
- Data EEPROM configuration depends on EBS and ESS<1:0> (FSS<9:8>) bit settings.

bit 7-4 **Unimplemented:** Read as '0'

bit 3-1 **BSS<2:0>:** Boot Segment Program Flash Code Protection bits<sup>(2)</sup>

- ×11 = No Boot program Flash segment
- 110 = Standard security, small Boot Segment
- 010 = High security, small Boot Segment
- 101 = Standard security, medium Boot Segment
- 001 = High security, medium Boot Segment
- 100 = Standard security, large Boot Segment
- 000 = High security, large Boot Segment

bit 0 **BWRP:** Boot Segment Program Flash Write Protection bit

- 1 = Boot segment can be written
- 0 = Boot segment is write-protected

**Note 1:** Not all devices have Boot RAM and Boot Data EEPROM protection. For specific device information, refer to **Section 26. "CodeGuard™ Security"** in this reference manual.

**2:** The exact definitions of Small, Medium, and Large Boot Program Flash and Boot RAM Segments vary from one device to another. For specific device information, refer to **Section 26. "CodeGuard™ Security"** in this reference manual.

<b>Legend:</b>		P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

# dsPIC30F Family Reference Manual

**Register 24-4: FSS: Secure Segment Configuration Register**

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23				bit 16			

Middle Byte:							
U-0	U-0	R/P	R/P	U-0	U-0	R/P	R/P
—	—	RSS<1:0>		—	—	ESS1	ESS0
bit 15				bit 8			

Lower Byte:							
U-0	U-0	U-0	U-0	R/P	R/P	R/P	R/P
—	—	—	—	SSS<2:0>			SWRP
bit 7				bit 0			

bit 23-14 **Unimplemented:** Read as '0'

bit 13-12 **RSS<1:0>:** Secure Segment RAM Code Protection bits<sup>(1)</sup>

Device Secure Segment size depends on RSS<1:0>, RBS<1:0> (FBS<13:12>), RL\_SSR (SSRAM<0>) and RL\_BSR (BSRAM<0>) bit settings.

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **ESS<1:0>:** Secure Segment Data EEPROM Code Protection bits

11 = No Secure Data EEPROM Segment

1x = Reserved

0x = Reserved

00 = Secure Data EEPROM Segment is 2048 bytes

bit 7-4 **Unimplemented:** Read as '0'

bit 3-1 **SSS<2:0>:** Secure Segment Program Flash Code Protection bits<sup>(2)</sup>

x11 = No Secure program Flash segment

110 = Standard security, small Secure Segment

010 = High security, small Secure Segment

101 = Standard security, medium Secure Segment

001 = High security, medium Secure Segment

100 = Standard security, large Secure Segment

000 = High security, large Secure Segment

bit 0 **SWRP:** Secure Segment Program Flash Write Protection bit

1 = Secure segment can be written

0 = Secure segment is write-protected

**Note 1:** Not all devices have Secure RAM and Secure Data EEPROM protection. For specific device information, refer to **Section 26. "CodeGuard™ Security"** in this reference manual.

**2:** The exact definitions of Small, Medium and Large Secure Segment vary from one device to another. For specific device information, refer to **Section 26. "CodeGuard™ Security"** in this reference manual.

Legend:			P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

## Section 24. Device Configuration

**Register 24-5: FGS: General Segment Configuration Register for Devices with Advanced Security**

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23				bit 16			

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

Lower Byte:							
U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P
—	—	—	—	—	GSS<1:0>		GWRP
bit 7				bit 0			

bit 23-3 **Unimplemented:** Read as '0'

bit 2-1 **GSS<1:0>:** General Segment Program Flash Code Protection bits

11 = No Protection

10 = Standard security; general program Flash segment starts at the end of SS and ends at EOM

0X = High security; general program Flash segment starts at the end of SS and ends at EOM

bit 0 **GWRP:** General Segment Program Flash Write-Protection bit

1 = General segment can be written

0 = General segment is write-protected

**Legend:**

R = Readable bit

W = Writable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

# dsPIC30F Family Reference Manual

**Register 24-6: FGS: General Segment Configuration Register for Devices with Basic or Intermediate Security**

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23				bit 16			

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

Lower Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	R/P	R/P
—	—	—	—	—	—	GCP	GWRP
bit 7				bit 0			

bit 23-2 **Unimplemented:** Read as '0'

bit 1 **GCP:** General Segment Program Flash Code Protection bit

1 = General Segment is not code protected

0 = General Segment is code protected

bit 0 **GWRP:** General Segment Program Flash Write-Protection bit

1 = General segment can be written

0 = General segment is write-protected

Legend:				P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	



## Section 24. Device Configuration

**Register 24-7: FICD: In-Circuit Debugger Configuration Register**

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23				bit 16			

Middle Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 15				bit 8			

Lower Byte:							
R/P	R/P	U	U	U	U	R/P	R/P
BKBUG	COE	—	—	—	—	ICS<1:0>	
bit 7				bit 0			

- bit 23-8 **Unimplemented:** Read as '1'
- bit 7 **BKBUG:** Background Debug Enable bit  
 1 = Device will reset in User mode  
 0 = Device will reset in Debug mode
- bit 6 **COE:** Debugger/Emulator Enable bit  
 1 = Device will reset in Operational mode  
 0 = Device will reset in Clip-On Emulation mode
- bit 5-2 **Unimplemented:** Read as '1'
- bit 1-0 **ICS<1:0>:** ICD Communication Channel Select Enable bits  
 11 = Communicate on PGC/EMUC and PGD/EMUD  
 10 = Communicate on EMUC1 and EMUD1  
 01 = Communicate on EMUC2 and EMUD2  
 00 = Communicate on EMUC3 and EMUD3

Legend:				P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

## 24.3 Configuration Bit Descriptions

This section provides specific functional information on each of the device Configuration bits.

### 24.3.1 Code Protection and CodeGuard™ Security

The dsPIC30F product families offer advanced security which protects the Intellectual Property that users invest in collaborative system designs. CodeGuard™ Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip with assurance that their Intellectual Property rights are not at risk.

The code protection features are controlled by the configuration registers (FBS, FSS and FGS) and vary from one dsPIC30F device to another. For further information, refer the device data sheet and **Section 26. “CodeGuard™ Security”** in this reference manual.

### 24.3.2 Oscillator Configuration Bits

dsPIC30F devices in the General Purpose, Sensor and Motor Control families feature one of three versions of the Oscillator system – Version 1, Version 2 and Version 3. For information on the Configuration bits of the FOSC device Configuration register available in each of these versions, please refer to **Section 7. “Oscillator”**.

### 24.3.3 BOR and POR Configuration Bits

The BOR and POR Configuration bits found in the FBORPOR Configuration register are used to set the Brown-out Reset voltage for the device, enable the Brown-out Reset circuit, and set the Power-up Timer delay time. For more information on these Configuration bits, please refer to **Section 8. “Reset”**.

### 24.3.4 Motor Control PWM Module Configuration Bits

The motor control PWM module Configuration bits are located in the FBORPOR Configuration register and are present only on devices that have the PWM module. The Configuration bits associated with the PWM module have two functions:

1. Select the state of the PWM pins at a device Reset (high-Z or output).
2. Select the active signal polarity for the PWM pins. The polarity for the high side and low side PWM pins may be selected independently.

For more information on Configuration bits, refer to **Section 15. “Motor Control PWM”**.

### 24.3.5 Watchdog Timer Configuration Bits

The dsPIC30F Watchdog Timer can be enabled and configured using the Watchdog Timer Configuration Register (FWDTC). **Section 9. “Watchdog Timer and Power Savings Modes”** (DS70196) provides more information on these Configuration bits.

### 24.3.6 In-Circuit Serial Programming (ICSP)

The ICSP capability is Microchip's proprietary process for microcontroller programming in the target application. The ICSP interface uses two pins as its core. The programming data pin (PGD) functions as both an input and an output, allowing programming data to be read in and device information to be read out on command. The programming clock pin (PGC) clocks in data and controls the overall process.

Serial programming allows customers to manufacture boards with unprogrammed devices and then to program the digital signal controller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the “dsPIC30F Flash Programming Specification” (DS70102) for details about ICSP.

### 24.3.7 In-Circuit Debugger

When MPLAB® ICD 2 or MPLAB REAL ICE in-circuit emulator is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging when used with MPLAB IDE. The debugging functionality is controlled through the EMUCx (emulation/debug clock) and EMUDx (emulation/debug data) pin functions.

Any of the four pairs of debugging clock/data pins can be used:

- PGC/EMUC and PGD/EMUD
- EMUC1 and EMUD1
- EMUC2 and EMUD2
- EMUC3 and EMUD3

The debugging clock and data pins must be selected by programming the ICD Communication Channel Select Enable (ICS<1:0>) bits in the In-Circuit Debugger Configuration (FICD<1:0>) register. To use the in-circuit debugger function of the device, the design must implement ICSP connections to MCLR, VDD, VSS, PGCx/EMCx and PGDx/EMUDx pin pairs. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

## 24.4 Device Identification Registers

The dsPIC30F devices have two sets of registers located in configuration space that provide identification information.

### 24.4.1 Device ID (DEVID) Registers

The configuration memory space locations 0xFF0000 and 0xFF0002 are used to store a read-only Device ID number that is set when the device is manufactured. This number identifies the dsPIC30F device type and the silicon revision.

The Device ID registers can be read by the user using table read instructions.

### 24.4.2 Unit ID Field

The Unit ID field is located at configuration memory space locations 0x800600 through 0x80063E. This field consists of 32 program memory locations and can be programmed at the Microchip factory with unique device information. This field cannot be written or erased by the user, but can be read using table read instructions.

Please contact Microchip technical support or your local Microchip representative for further details.

**Table 24-1: Device Configuration Register Map**

File Name	Addr.	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FOSC	F80000	—	FCKSM<1:0>		—	—	—	FOS<2:0>			—	—	—	FPR<4:0>				
FWDΤ	F80002	—	FWDΤEN	—	—	—	—	—	—	—	—	—	FWPSA<1:0>		FWPSB<3:0>			
FBORPOR	F80004	—	MCLREN	—	—	—	—	PWMPIN	HPOL	LPOL	BOREN	—	BORV<1:0>		—	—	FPWRT<1:0>	
FBS	F80006	—	—	—	RBS1	RBS0	—	—	—	EBS	—	—	—	—	BSS<2:0>		BWRP	
FSS	F80008	—	—	—	RSS1	RSS0	—	—	ESS1	ESS0	—	—	—	—	SSS<2:0>		SWRP	
FGS	F8000A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GSS<1:0>		GWRP

**Legend:** u = uninitialized bit

**Note:** Refer to “dsPIC30F Family Reference Manual” (DS70046) for descriptions of register bit fields.

## 24.5 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Device Configuration module are:

Title	Application Note #
<i>Using the dsPIC30F for Sensorless BLDC Control</i>	AN901
<b>Note:</b> Please visit the Microchip web site ( <a href="http://www.microchip.com">www.microchip.com</a> ) for additional Application Notes and code examples for the dsPIC30F Family of devices.	

### 24.6 Revision History

#### Revision A

This is the initial released revision of this document.

#### Revision B

This revision incorporates technical content changes for the dsPIC30F Device Configuration module.

#### Revision C

This revision incorporates all known errata at the time of this document update.

#### Revision D

Descriptions of three versions of the Oscillator Control module have been added. The definition of the FOSC Configuration register was moved to DS70054.

#### Revision E

This revision adds the FBS and FSS Configuration registers and updates the FGS register to incorporate CodeGuard™ Security information.

NOTES: