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## Section 22. Data Converter Interface (DCI)

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### HIGHLIGHTS

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## 22.1 Introduction

The dsPIC Data Converter Interface (DCI) module allows simple interfacing of devices, such as audio coder/decoders (codecs), A/D converters, and D/A converters.

The following interfaces are supported:

- Framed Synchronous Serial Transfer (Single or Multi-Channel)
- Inter-IC Sound (I<sup>2</sup>S) Interface
- AC-Link Compliant mode

Many codecs intended for use in audio applications support sampling rates between 8 kHz and 48 kHz and use one of the interface protocols listed above. The DCI automatically handles the interface timing associated with these codecs. No overhead from the CPU is required until the requested amount of data has been transmitted and/or received by the DCI. Up to four data words may be transferred between CPU interrupts.

The data word length for the DCI is programmable up to 16 bits to match the data size of the dsPIC30F CPU. However, many codecs have data word sizes greater than 16 bits. Long data word lengths can be supported by the DCI. The DCI is configured to transmit/receive the long word in multiple 16-bit time slots. This operation is transparent to the user and the long data word is stored in consecutive register locations.

The DCI can support up to 16 time slots in a data frame, for a maximum frame size of 256 bits. There are control bits for each time slot in the data frame that determine whether the DCI will transmit/receive during the time slot.

## 22.2 Control Register Descriptions

The DCI has five Control registers and one Status register, which are listed below:

- DCICON1: DCI module enable and mode bits.
- DCICON2: DCI module word length, data frame length, and buffer setup.
- DCICON3: DCI module bit clock generator setup.
- DCISTAT: DCI module status information.
- RSCON: Active frame time slot control for data reception.
- TSCON: Active frame time slot control for data transmit.

In addition to these Control and Status registers, there are four Transmit registers, TXBUF0....TXBUF3, and four Receive registers, RXBUF0....RXBUF3.

## Section 22. Data Converter Interface (DCI)

**Register 22-1: DCICON1**

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
DCIEN	—	DCISIDL	—	DLOOP	CSCKD	CSCKE	COFSD
bit 15				bit 8			

Lower Byte:							
R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
UNFM	CSDOM	DJST	—	—	—	COFSM<1:0>	
bit 7			bit 0				

- bit 15 **DCIEN:** DCI Module Enable bit  
1 = Module is enabled  
0 = Module is disabled
- bit 14 **Reserved:** Read as '0'
- bit 13 **DCISIDL:** DCI Stop in Idle Control bit  
1 = Module will halt in CPU Idle mode  
0 = Module will continue to operate in CPU Idle mode
- bit 12 **Reserved:** Read as '0'
- bit 11 **DLOOP:** Digital Loopback Mode Control bit  
1 = Digital Loopback mode is enabled. CSDI and CSDO pins internally connected.  
0 = Digital Loopback mode is disabled
- bit 10 **CSCKD:** Sample Clock Direction Control bit  
1 = CSDK pin is an input when DCI module is enabled  
0 = CSDK pin is an output when DCI module is enabled
- bit 9 **CSCKE:** Sample Clock Edge Control bit  
1 = Data changes on serial clock falling edge, sampled on serial clock rising edge  
0 = Data changes on serial clock rising edge, sampled on serial clock falling edge
- bit 8 **COFSD:** Frame Synchronization Direction Control bit  
1 = COFS pin is an input when DCI module is enabled  
0 = COFS pin is an output when DCI module is enabled
- bit 7 **UNFM:** Underflow Mode bit  
1 = Transmit last value written to the Transmit registers on a transmit underflow  
0 = Transmit '0's on a transmit underflow
- bit 6 **CSDOM:** Serial Data Output Mode bit  
1 = CSDO pin will be tri-stated during disabled transmit time slots  
0 = CSDO pin drives '0's during disabled transmit time slots
- bit 5 **DJST:** DCI Data Justification Control bit  
1 = Data transmission/reception is begun during the same serial clock cycle as the frame synchronization pulse  
0 = Data transmission/reception is begun one serial clock cycle after frame synchronization pulse
- bit 4-2 **Reserved:** Read as '0'
- bit 1-0 **COFSM<1:0>:** Frame Sync Mode bits  
11 = 20-bit AC-Link mode  
10 = 16-bit AC-Link mode  
01 = I<sup>2</sup>S Frame Sync mode  
00 = Multi-Channel Frame Sync mode

**Legend:**

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

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Register 22-2: DCICON2

Upper Byte:							
U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0
—	—	—	—	BLEN<1:0>		—	COFSG3
bit 15				bit 8			

Lower Byte:							
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
COFSG<2:0>			—	WS<3:0>			
bit 7				bit 0			

bit 15-12 **Reserved:** Read as '0'

bit 11-10 **BLEN<1:0>:** Buffer Length control bits

11 = Four data words will be buffered between interrupts  
10 = Three data words will be buffered between interrupts  
01 = Two data words will be buffered between interrupts  
00 = One data word will be buffered between interrupts

bit 9 **Reserved:** Read as '0'

bit 8-5 **COFSG<3:0>:** Frame Sync Generator control bits

1111 = Data frame has 16 words  
||  
0010 = Data frame has 3 words  
0001 = Data frame has 2 words  
0000 = Data frame has 1 word

bit 4 **Reserved:** Read as '0'

bit 3-0 **WS<3:0>:** DCI Data Word Size bits

1111 = Data word size is 16 bits  
||  
0100 = Data word size is 5 bits  
0011 = Data word size is 4 bits  
0010 = **Invalid Selection.** Do not use. Unexpected results may occur.  
0001 = **Invalid Selection.** Do not use. Unexpected results may occur.  
0000 = **Invalid Selection.** Do not use. Unexpected results may occur.

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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Register 22-3: DCICON3

Upper Byte:							
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	BCG<11:8>			
bit 15				bit 8			

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BCG<7:0>							
bit 7				bit 0			

bit 15-12 **Reserved:** Read as '0'.

bit 11-0 **BCG<11:0>:** DCI Bit Clock Generator Control bits

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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## Register 22-4: DCISTAT

Upper Byte:							
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	SLOT<3:0>			
bit 15				bit 8			

Lower Byte:							
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ROV	RFUL	TUNF	TMPTY
bit 7				bit 0			

bit 15-12 **Reserved:** Read as '0'

bit 11-8 **SLOT<3:0>:** DCI Slot Status bits  
1111 = Slot #15 is currently active  
| |  
0010 = Slot #2 is currently active  
0001 = Slot #1 is currently active  
0000 = Slot #0 is currently active

bit 7-4 **Reserved:** Read as '0'

bit 3 **ROV:** Receive Overflow Status bit  
1 = A receive overflow has occurred for at least one receive register  
0 = A receive overflow has not occurred

bit 2 **RFUL:** Receive Buffer Full Status bit  
1 = New data is available in the receive registers  
0 = The receive registers have old data

bit 1 **TUNF:** Transmit Buffer Underflow Status bit  
1 = A transmit underflow has occurred for at least one transmit register  
0 = A transmit underflow has not occurred

bit 0 **TMPTY:** Transmit Buffer Empty Status bit  
1 = The Transmit registers are empty  
0 = The Transmit registers are not empty

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

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**Register 22-5: RSCON**

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE15	RSE14	RSE13	RSE12	RSE11	RSE10	RSE9	RSE8
bit 15							
bit 8							

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE7	RSE6	RSE5	RSE4	RSE3	RSE2	RSE1	RSE0
bit 7							
bit 0							

- bit 11 **RSE<15:0>**: Receive Slot Enable bits  
1 = CSDI data is received during the individual time slot n  
0 = CSDI data is ignored during the individual time slot n

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

**Register 22-6: TSCON**

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE15	TSE14	TSE13	TSE12	TSE11	TSE10	TSE9	TSE8
bit 15							
bit 8							

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE7	TSE6	TSE5	TSE4	TSE3	TSE2	TSE1	TSE0
bit 7							
bit 0							

- bit 11 **TSE<15:0>**: Transmit Slot Enable Control bits  
1 = Transmit buffer contents are sent during the individual time slot n  
0 = CSDO pin is tri-stated or driven to logic '0' during the individual time slot, depending on the state of the CSDOM bit

**Legend:**

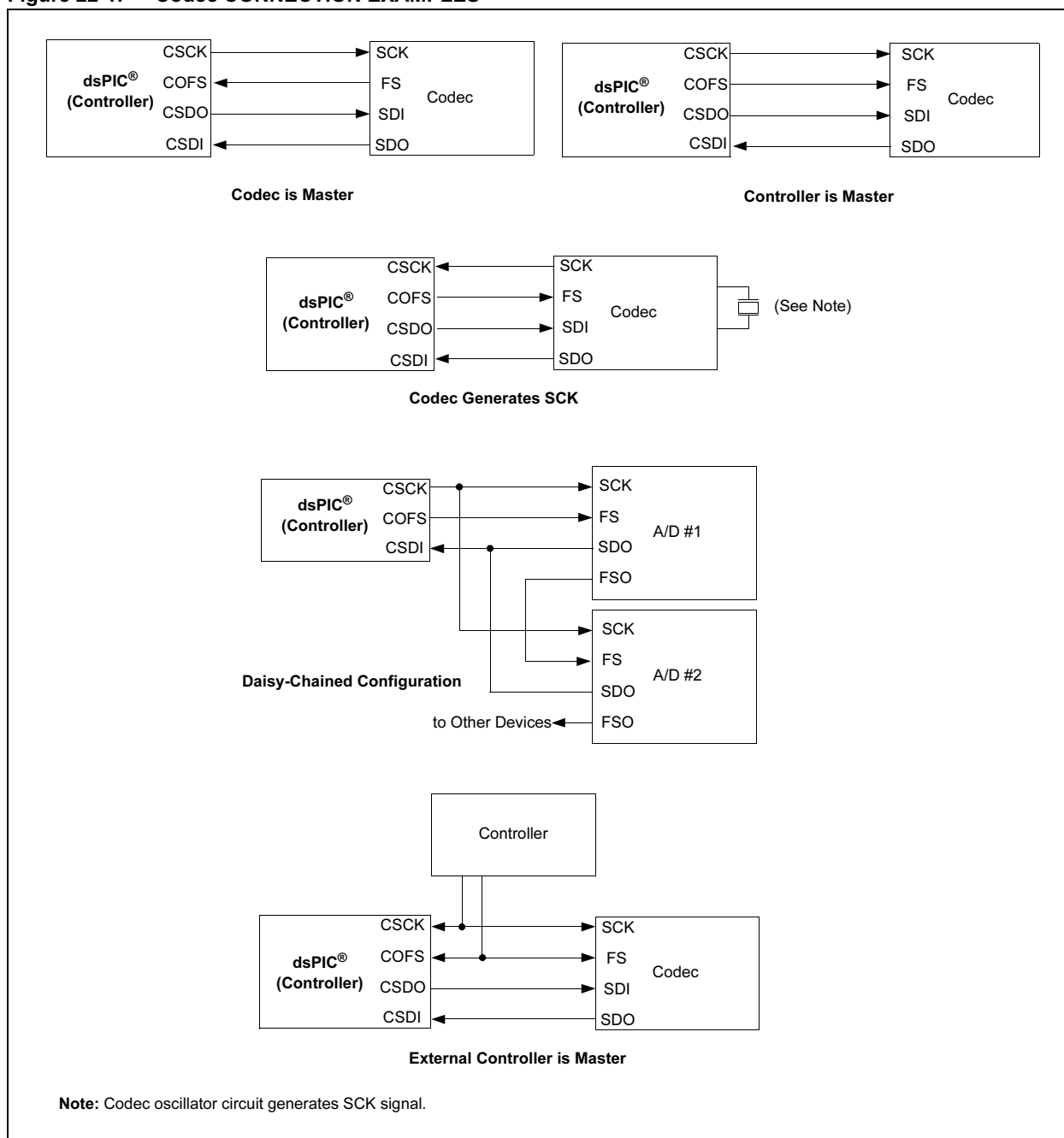
R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

## 22.3 Codec Interface Basics and Terminology

The interface protocols supported by the DCI require the use of a Frame Synchronization (FS) signal to initiate a data transfer between two devices. In most cases, the rising edge of FS starts a new data transfer. In any codec application there is, at a minimum, a controller and a codec device. Either device may produce FS. The device that generates FS is the master device. Conceptually, the master device does not have to be the transmitting or receiving device. Various connection examples are shown in Figure 22-1. The frequency of the FS signal is usually the system sampling rate, fs.

**Note:** The details given in this section are not specific to the DCI module. This discussion is intended to provide the user some background and terminology related to the digital serial interface protocols found in most codec devices.

**Figure 22-1: Codec CONNECTION EXAMPLES**





All interfaces have a serial transfer clock, SCK. The SCK signal may be generated by any of the connected devices or can be provided externally. In some systems, SCK is also referred to as the bit clock. For codecs that offer high signal fidelity, it is common for the SCK signal to be derived from the crystal oscillator on the codec device. The protocol defines the edge of SCK on which data is sampled. The master device generates the FS signal with respect to SCK.

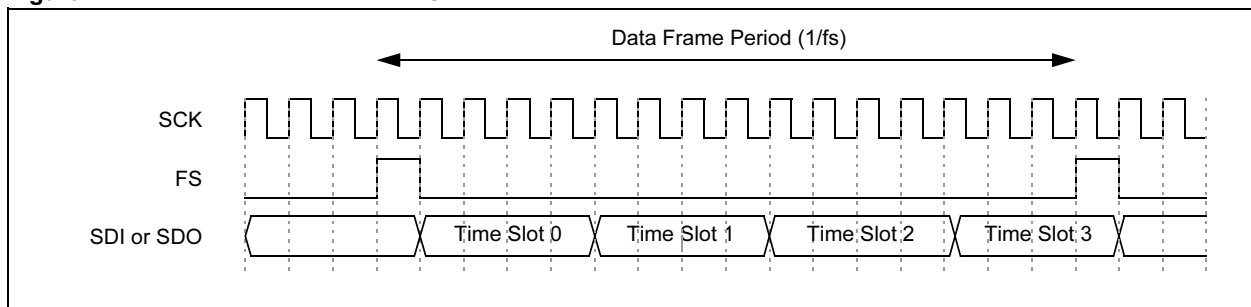
The period of the FS signal delineates one data frame. This period is the same as the data sample period. The number of SCK cycles that occur during the data frame will depend on the type of codec that is selected. The ratio of the SCK frequency to the system sample rate is expressed as a ratio of  $n$ , where  $n$  is the number of SCK periods per data frame.

One advantage of using a framed interface protocol is that multiple data words can be transferred during each sample period, or data frame. Each division of the data frame is referred to as a time slot. The time slots can be used for multiple codec data channels and/or control information. Furthermore, multiple devices can be multiplexed on the same serial data pins. Each slave device is programmed to place its data on the serial data connection during the proper time slot. The output of each slave device is tri-stated at all other times to permit other devices to use the serial bus.

Some devices allow the FS signal to be daisy-chained via Frame Synchronization Output (FSO) pins. A typical daisy-chained configuration is shown in Figure 22-1. When the transfer from the first slave device has completed, a FS pulse is sent to the second device in the chain via its FSO pin. This process continues until the last device in the chain has sent its data. The controller (master) device should be programmed for a data frame size that accommodates all of the data words that will be transferred.

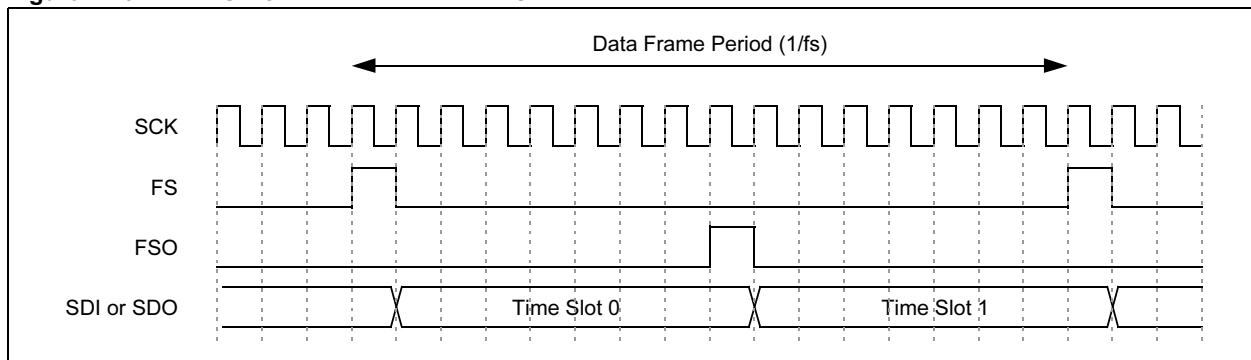
The timing for a typical data transfer is shown in Figure 22-2. Most protocols begin the data transfer one SCK cycle after the FS signal is detected. This example uses a 16 fs clock and transfers four 4-bit data words per frame.

**Figure 22-2: FRAMED DATA TRANSFER EXAMPLE**



The timing for a typical data transfer with daisy-chained devices is shown in Figure 22-3. This example uses a 16 fs SCK frequency and transfers two 8-bit data words per frame. After the FS pulse is detected, the first device in the chain transfers the first 8-bit data word and generates the FSO signal at the end of the transfer. The FSO signal begins the transfer of the second data word from the second device in the chain.

**Figure 22-3: DAISY-CHAINED DATA TRANSFER EXAMPLE**



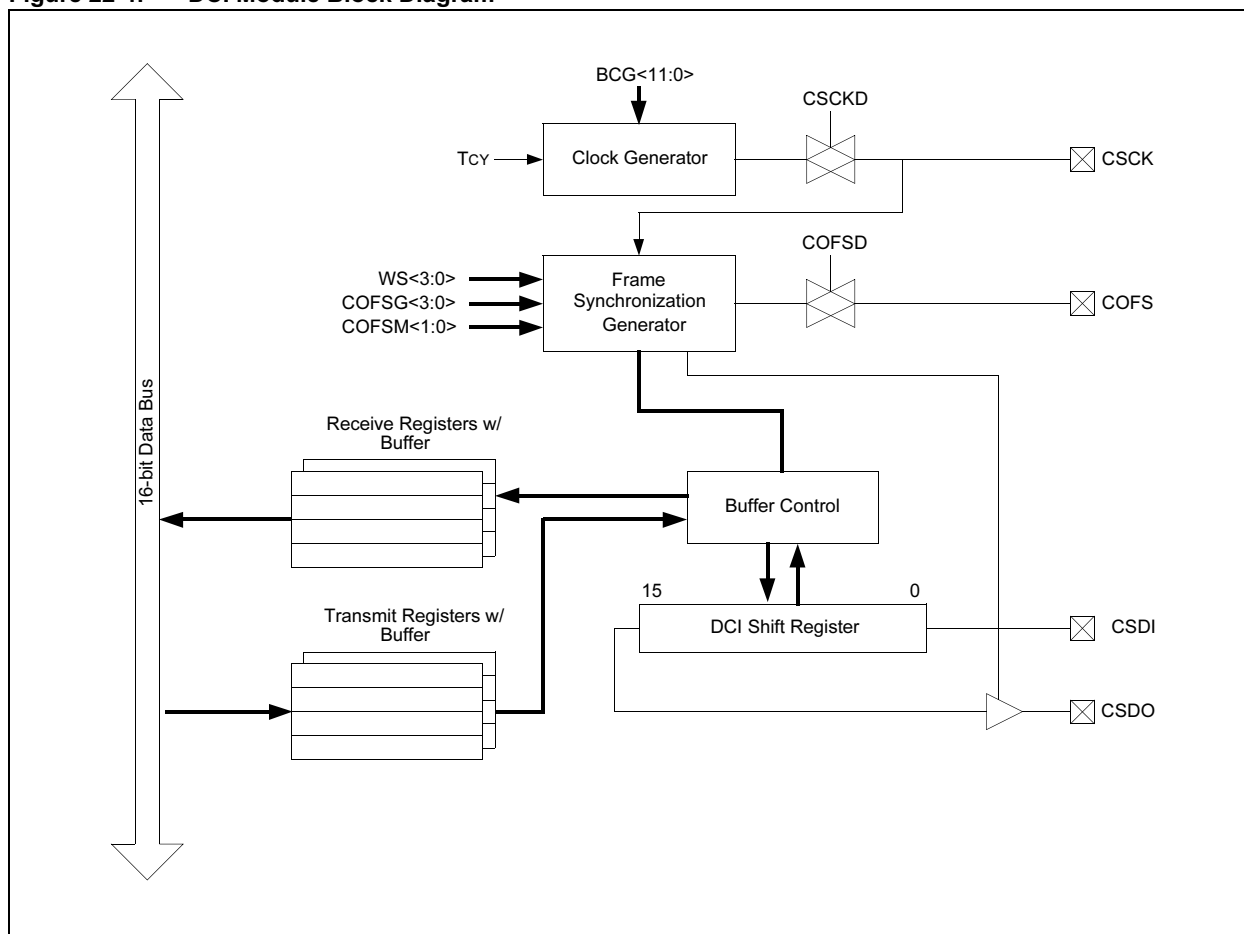
The FS pulse has a minimum active time of one SCK period so the slave device can detect the start of the data frame. The duty cycle of the FS pulse may vary depending on the specific protocol that is used to mark certain boundaries in the data frame. For example, the I<sup>2</sup>S protocol uses a FS signal that has a 50% duty cycle. The I<sup>2</sup>S protocol is optimized for the transfer of two data channels (left and right channel audio information). The edges of the FS signal mark the boundaries of the left and right channel data words. The AC-Link protocol uses a FS signal that is high for 16 SCK periods and low for 240 SCK periods. The edges of the AC-Link FS signal mark the boundaries of control information and data in the frame.

**Note:** Refer to **Section 26. “Appendix”** of this manual for additional information on codec communication protocols.

## 22.4 DCI Operation

A simplified block diagram of the module is shown in Figure 22-4. The module consists of a Transmit/Receive Shift register that is connected to a small range of memory buffers via a buffer control unit. This arrangement allows the DCI to support various codec serial protocols. The DCI Shift register is 16-bits wide. Data is transmitted and received by the DCI MSbit first.

**Figure 22-4: DCI Module Block Diagram**



### 22.4.1 DCI Pins

There are four I/O pins associated with the DCI. The DCI, when enabled, controls the data direction of each of the four pins.

#### 22.4.1.1 CSCK Pin

The CSCK pin provides the serial clock connection for the DCI. The CSCK pin may be configured as an input or output using the CSCKD control bit, DCICON1<10>. When the CSCK pin is configured as an output (CSCKD = 0), the serial clock is derived from the dsPIC30F system clock source and supplied to external devices by the DCI. When the CSCK pin is configured as an input (CSCKD = 1), the serial clock must be provided by an external device.

#### 22.4.1.2 CSDO Pin

The Serial Data Output (CSDO) pin is configured as an output only pin when the module is enabled. The CSDO pin drives the serial bus whenever data is to be transmitted. The CSDO pin can be tri-stated or driven to '0' during serial clock periods when data is not transmitted, depending on the state of the CSDOM control bit (DCICON1<6>). The tri-state option allows other devices to be multiplexed onto the CSDO connection.

#### 22.4.1.3 CSDI Pin

The serial data input (CSDI) pin is configured as an input only pin when the module is enabled.

#### 22.4.1.4 COFS Pin

The frame synchronization (COFS) pin is used to synchronize data transfers that occur on the CSDO and CSDI pins. The COFS pin may be configured as an input or an output. The data direction for the COFS pin is determined by the COFSD control bit (DCICON1<8>). When the COFSD bit is cleared, the COFS pin is an output. The DCI module will generate frame synchronization pulses to initiate a data transfer. The DCI is the master device for this configuration. When the COFSD bit is set, the COFS pin becomes an input. Incoming synchronization signals to the module will initiate data transfers. The DCI is a slave device when the COFSD control bit is set.

### 22.4.2 Module Enable

The DCI module is enabled or disabled by setting/clearing the DCIEN control bit (DCICON1<15>). Clearing the DCIEN control bit has the effect of resetting the module. In particular, all counters associated with serial clock generation, frame sync, and the buffer control logic are reset (see **Section 22.5.1.1 “DCI Start-up and Data Buffering”** and **Section 22.5.1.2 “DCI Disable”** for additional information).

When enabled, the DCI controls the data direction for the CSCK, CSDI, CSDO and COFS I/O pins associated with the module. The PORT, LAT, and TRIS register values for these I/O pins are overridden by the DCI module when the DCIEN bit is set.

It is also possible to override the CSCK pin separately when the bit clock generator is enabled. This permits the bit clock generator to be operated without enabling the rest of the DCI module.

## 22.4.3 Bit Clock Generator

The DCI module has a dedicated 12-bit time base that produces the bit clock. The bit clock rate (period) is set by writing a non-zero 12-bit value to the BCG<11:0> control bits (DCICON3<11:0>). When the BCG<11:0> bits are set to zero, the bit clock will be disabled.

**Note:** The CSMCK I/O pin will be controlled by the DCI module if the DCIEN bit is set **OR** the bit clock generator is enabled by writing a non-zero value to BCG<11:0>. This allows the bit clock generator to be operated independently of the DCI module.

When the CSMCK pin is controlled by the DCI module, the corresponding PORT, LAT and TRIS Control register values for the CSMCK pin will be overridden and the data direction for the CSMCK pin will be controlled by the CSMCKD control bit (DCICON1<10>).

If the serial clock for the DCI is to be provided by an external device, the BCG<11:0> bits should be set to '0' and the CSMCKD bit set to '1'.

If the serial clock is to be generated by the DCI module, the BCG<11:0> control bits should be set to a non-zero value (see Equation 22-1) and the CSMCKD control bit should be set to zero.

The formula for the bit clock frequency is given in Equation 22-1.

### Equation 22-1: DCI Bit Clock Generator Value

$$\text{BCG<11:0>} = \frac{f_{CY}}{2 f_{CSCK}} - 1$$

The required bit clock frequency will be determined by the system sampling rate and frame size. Typical bit clock frequencies range from 16x to 512x the converter sample rate, depending on the data converter and the communication protocol that is used.

**Note:** The BCG<11:0> bits have no effect on the operation of the DCI module when the CSMCK signal is provided externally (CSCKD = 1).

## 22.4.4 Sample Clock Edge Selection

The CSMCKE control bit (DCICON1<9>) determines the sampling edge for the serial clock signal. If the CSMCKE bit is cleared (default), data will be sampled on the falling edge of the CSMCK signal. The AC-Link protocols and most multi-channel formats require that data be sampled on the falling edge of the CSMCK signal. If the CSMCKE bit is set, data will be sampled on the rising edge of CSMCK. The I<sup>2</sup>S protocol requires that data be sampled on the rising edge of the serial clock signal.

## 22.4.5 Frame Sync Mode Control Bits

The type of interface protocol supported by the DCI is selected using the COFSM<1:0> control bits (DCICON1<1:0>). The following Operating modes can be selected:

- Multi-channel Mode
- I<sup>2</sup>S Mode
- AC-Link Mode (16-bit)
- AC-Link Mode (20-bit)

Specific information for each of the protocols is provided in subsequent sections.

## 22.4.6 Word-Size Selection Bits

The WS<3:0> word-size selection bits (DCICON2<3:0>) determine the number of bits in each DCI data word. Any data length from 4 to 16 bits may be selected.

**Note:** The WS control bits are used only in the multi-channel and I<sup>2</sup>S modes. These bits have no effect in AC-Link mode since the data slot sizes are fixed by the protocol.

## 22.4.7 Frame Synchronization Generator

The Frame Sync Generator (FSG) is a 4-bit counter that sets the frame length in data words. The period for the FSG is set by writing the COFSG<3:0> control bits (DCICON2<8:5>). The FSG period (in serial clock cycles) is determined by the following formula:

### Equation 22-2: Frame Length, In CSCK Cycles

$$FrameLength = (WS<3:0> + 1) \cdot (COFSG<3:0> + 1)$$

Frame lengths up to 16 data words may be selected. The frame length in serial clock periods will vary up to a maximum of 256 depending on the word size that is selected.

**Note:** The COFSG control bits will have no effect in AC-Link mode, since the frame length is set to 256 serial clock periods by the protocol.

## 22.4.8 Transmit and Receive Registers

The DCI has four Transmit registers, TXBUF0...TXBUF3, and four Receive registers, RXBUF0..RXBUF3. All of the Transmit and Receive registers are memory mapped.

### 22.4.8.1 Buffer Data Alignment

Data values are always stored left-justified in the DCI registers, since audio PCM data is represented as a signed 2's complement fractional number. If the programmed DCI word size is less than 16 bits, the unused LSbs in the Receive registers are set to '0' by the module. Also, the unused LSbs in the Transmit register are ignored by the module.

### 22.4.8.2 Transmit and Receive Buffers

The Transmit and Receive registers each have a set of buffers that are not accessible by the user. Effectively, each transmit and receive buffer location is double-buffered. The DCI transmits data from the transmit buffers and writes received data to the receive buffers. The buffers allow the user to read and write the RXBUF and TXBUF registers, while the DCI uses data from the buffers.

## 22.4.9 DCI Buffer Control Unit

The DCI module contains a buffer control unit that transfers data between the buffer memory and the Serial Shift register. The buffer control unit also transfers data between the buffer memory and the TXBUF and RXBUF registers. The buffer control unit allows the DCI to queue the transmission and reception of multiple data words without CPU overhead.

The DCI generates an interrupt each time a transfer between the buffer memory and the TXBUF and RXBUF registers takes place. The number of data words buffered between interrupts is determined by the BLEN<1:0> control bits (DCICON2<11:10>). The size of the transmit and receive buffering may be varied from 1 to 4 data words using the BLEN<1:0> bits.

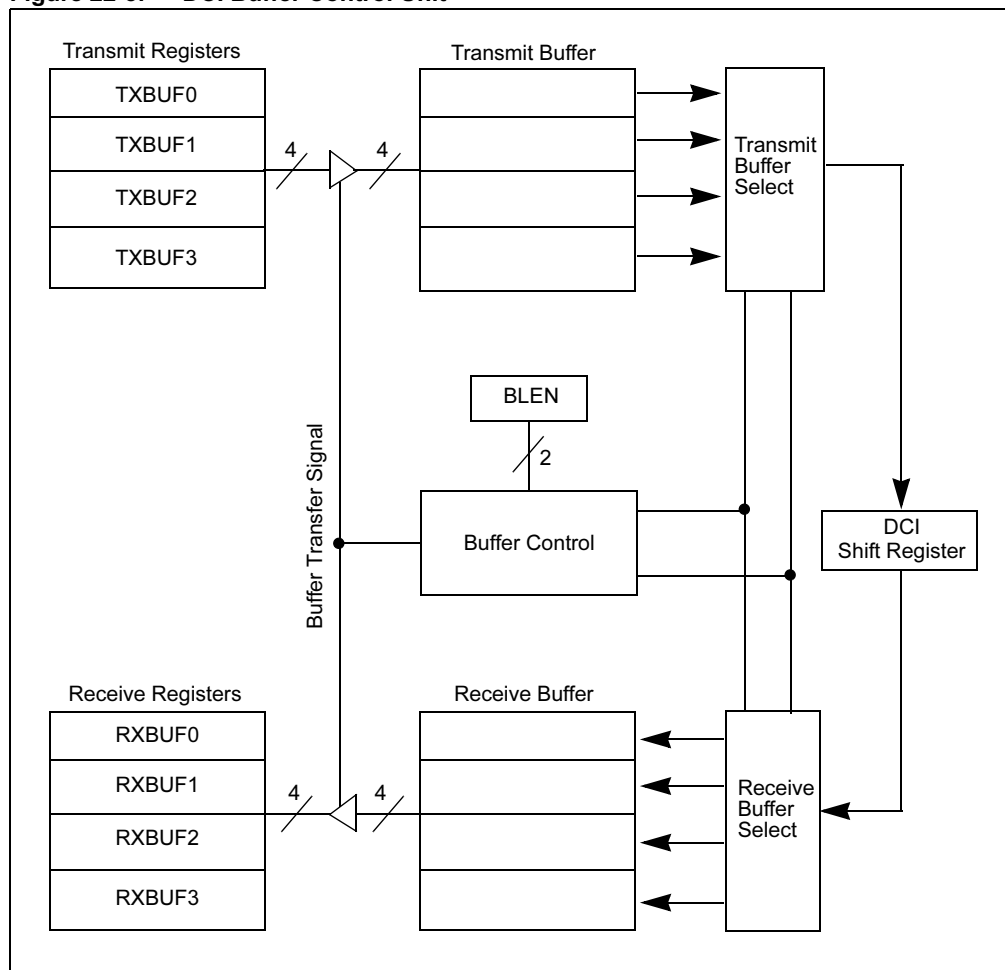
Each time a data transfer takes place between the DCI Shift register and the buffer memory, the DCI buffer control unit is incremented to point to the next buffer location. If the number of transmitted or received data words is equal to the BLEN value + 1, the following will occur:

- The buffer control unit is reset to point to the first buffer location
- The received data held in the buffer is transferred to the RXBUF registers
- The data in the TXBUF registers is transferred to the buffer
- A CPU interrupt is generated

The DCI buffer control unit will also reset the buffer pointer to the first buffer location each time a frame boundary is reached. This action ensures alignment between the buffer locations and the enabled time slots in the data frame.

The DCI buffer control unit always accesses the same relative location in the Transmit and Receive buffers. If the DCI is transmitting data from TXBUF3, for example, then any data received during that time slot will be written to RXBUF3.

**Figure 22-5: DCI Buffer Control Unit**



## 22.4.10 Transmit Slot Enable Bits

The TSCON SFR has control bits that are used to enable up to 16 time slots for transmission. These control bits are the TSE<15:0> bits. The size of each time slot is determined by the WS<3:0> word size selection bits and can vary up to 16 bits.

If a transmit time slot is enabled via one of the TSE bits (TSE<sub>x</sub> = 1), the contents of the current transmit buffer location will be loaded into the CSDO Shift register and the DCI buffer control unit will increment to point to the next buffer location.

Not all TSE control bits will have an effect on the module operation if the selected frame size has less than 16 data slots. The Most Significant TSE control bits are not used. For example, if COFSG<3:0> = 0111 (8 data slots per frame), TSE8 through TSE15 will have no effect on the DCI operation.

### 22.4.10.1 CSDO Mode Control

During disabled transmit time slots, the CSDO pin can drive '0's or can be tri-stated, depending on the state of the CSDOM bit (DCICON1<6>). A given transmit time slot is disabled if its corresponding TSE<sub>x</sub> bit is cleared in the TSCON register.

If the CSDOM bit is cleared (default), the CSDO pin will drive '0's onto the CSDO pin during disabled time slot periods. This mode is used when there are only two devices (1 master and 1 slave) attached to the serial bus.

If the CSDOM bit is set, the CSDO pin will be tri-stated during unused time slot periods. This mode allows multiple dsPIC30F devices to share the same CSDO line in a multiplexed application. Each device on the CSDO line is configured so that it will only transmit data during specific time slots. No two devices should transmit data during the same time slot.

## 22.4.11 Receive Slot Enable Bits

The RSCON SFR contains control bits (RSE<15:0>) that are used to enable up to 16 time slots for reception. The size of each receive time slot is determined by the WS<3:0> control bits and can vary from 4 to 16 bits.

If a receive time slot is enabled via one of the RSE bits (RSE<sub>x</sub> = 1), the Shift register contents will be written to the current DCI receive buffer location and the buffer control logic will advance to the next available buffer location.

Data is not packed in the receive memory buffer locations if the selected word size is less than 16 bits. Each received slot data word is stored in a separate 16-bit buffer location. Data is always stored in a left-justified format in the receive memory buffer.

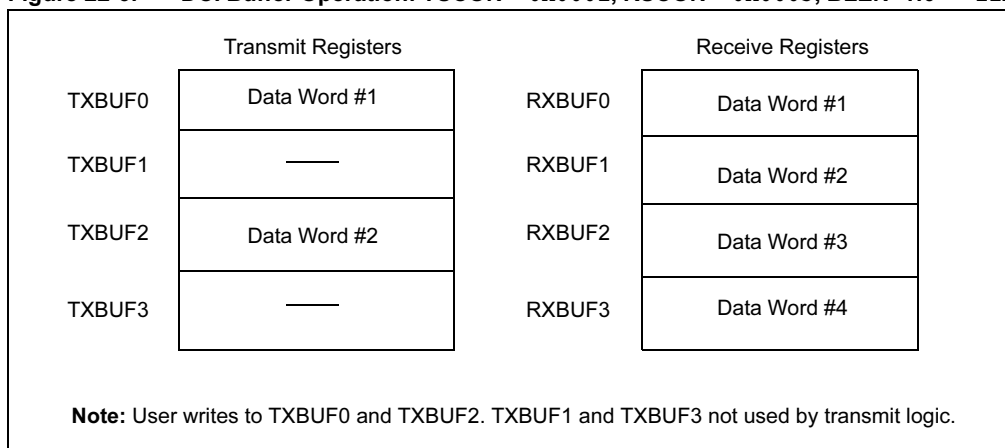
## 22.4.12 TSCON and RSCON Operation with Buffer Control Unit

The slot enable bits in the TSCON and RSCON registers function independently, with the exception of the buffer control logic. For each time slot in a data frame, the buffer location is advanced if either the TSE<sub>x</sub> or the RSE<sub>x</sub> bit is set for the current time slot. That is, the buffer control unit synchronizes the Transmit and Receive buffering so that the Transmit and Receive buffer location will always be the same for each time slot in the data frame.

If the TSE<sub>x</sub> bit and the RSE<sub>x</sub> bit are both set for every time slot that is used in the data frame, the DCI will Transmit and Receive equal amounts of data.

In some applications, the number of data words transmitted during a frame may not equal the number of words received. As an example, assume that the DCI is configured for a 2-word data frame, TSCON = 0x0001 and RSCON = 0x0003. This configuration would allow the DCI to transmit one data word per frame and receive two data words per frame. Since two data words are received for each data word that is transmitted, the user would write every other transmit buffer location. Specifically, only TXBUF0 and TXBUF2 would be used to transmit data.

**Figure 22-6: DCI Buffer Operation: TSCON = 0x0001, RSCON = 0x0003, BLEN<1:0> = 11b**



## 22.4.13 Receive Status Bits

There are two receive status bits, RFUL and ROV.

The receive status bits only indicate status for register locations that are enabled for use by the module. This is a function of the BLEN<1:0> control bits. If the buffer length is set to less than four words, the unused buffer locations will not affect the receive status bits.

The RFUL status bit (DCISTAT<2>) is read only and indicates that new data is available in the Receive registers. The RFUL bit is cleared automatically when all RXBUF registers in use have been read by the user software.

The ROV status bit (DCISTAT<3>) is read only and indicates that a receive overflow has occurred for at least one of the Receive register locations. A receive overflow occurs when the RXBUF register location is not read by the user software before new data is transferred from the buffer memory. When a receive overflow occurs, the old contents of the register are overwritten. The ROV status bit is cleared automatically when the register that caused the overflow is read.

## 22.4.14 Transmit Status Bits

There are two transmit status bits, TMPTY and TUNF.

The transmit status bits only indicate status for register locations that are used by the module. If the buffer length is set to less than four words, for example, the unused register locations will not affect the transmit status bits.

The TMPTY bit (DCISTAT<0>) is read only and is set when the contents of the active TXBUF registers are transferred to the Transmit Buffer registers. The TMPTY bit may be polled in software to determine when the Transmit registers may be written. The TMPTY bit is cleared automatically by the hardware when a write to any of the TXBUF registers in use occurs.

The TUNF bit (DCISTAT<1>) is read only and indicates that a transmit underflow has occurred for at least one of the Transmit registers that is in use. The TUNF bit is set when the TXBUF register contents are transferred to the transmit buffer memory and the user did not write all of the TXBUF registers in use since the last buffer transfer. The TUNF status bit is cleared automatically when the TXBUF register that underflowed is written by the user software.

## 22.4.15 SLOT Status Bits

The SLOT<3:0> status bits (DCISTAT<11:7>) indicate the current active time slot in the data frame and are useful when more than four words per data frame need to be transferred. The user may poll these status bits in software when a DCI interrupt occurs to determine what time slot data was last received and which time slot data should be loaded into the TXBUF registers.

## 22.4.16 Digital Loopback Mode

Digital Loopback mode is enabled by setting the DLOOP control bit (DCICON1<11>). When the DLOOP bit is set, the module internally connects the CSDO signal to CSDI. The actual data input on the CSDI pin will be ignored in Digital Loopback mode.

## 22.4.17 Underflow Mode Control Bit

When a transmit underflow occurs, one of two actions may occur depending on the state of the UNFM control bit (DCICON1<7>). If the UNFM bit is cleared (default), the module will transmit '0's on the CSDO pin during the active time slot for the buffer location. In this Operating mode, the codec device attached to the DCI module will simply be fed digital 'silence'. If the UNFM control bit is set, the module will transmit the last data written to the buffer location. This Operating mode permits the user to send a continuous data value to the codec device without consuming software overhead.

## 22.4.18 Data Justification Control

In most applications, the data transfer begins one serial clock cycle after the FS signal is sampled active. This is the DCI module default. An alternate data alignment can be selected by setting the DJST control bit (DCICON2<5>). When DJST = 1, data transfers will begin during the same serial clock cycle as the FS signal.

## 22.4.19 DCI Module Interrupts

The frequency of DCI module interrupts is dependent on the number of active time slots (TSCON and RSCON registers), length of the data frame (WS and COFSG control bits), and the BLEN control bits. An interrupt is generated at the following times:

- When the buffer length has been reached
- When a frame boundary is reached

A buffer memory transfer takes place each time the above events occur. A buffer memory transfer is defined as the time when the previously written TXBUF values are transferred to the transmit buffer memory and new received values in the receive buffer memory are transferred into the RXBUF registers.



### 22.5 Using the DCI Module

This section explains how to configure and use the DCI with specific kinds of data converters.

#### 22.5.1 How to Transmit and Receive Data Using the DCI Buffers, Status Bits and Interrupts

The DCI can buffer up to four data words between CPU interrupts depending on the setting of the BLEN control bits. The buffered data can be transmitted and received in a single data frame, or across multiple data frames, depending on the TSCON and RSCON register settings. For example, assume  $\text{BLEN}\langle 1:0 \rangle = 00b$  (buffer one data word per interrupt) and  $\text{TSCON} = \text{RSCON} = 0x0001$ . This particular configuration represents the most basic setup and would cause the DCI to transmit/receive one data word at the beginning of every data frame. The CPU would be interrupted after every data word transmitted/received since  $\text{BLEN}\langle 1:0 \rangle = 00b$ .

For a second configuration example, assume  $\text{BLEN}\langle 1:0 \rangle = 11b$  (buffer four data words per interrupt) and  $\text{TSCON} = \text{RSCON} = 0x0001$ . This configuration would cause the DCI to transmit/receive one data word at the beginning of every data frame, but a CPU interrupt would be generated after four data words were transmitted/received. This configuration would be useful for block processing, where multiple data samples are processed at once.

For a third configuration example, assume  $\text{BLEN}\langle 1:0 \rangle = 11b$  (buffer four data words per interrupt) and  $\text{TSCON} = \text{RSCON} = 0x000F$ . This configuration would cause the DCI to transmit/receive four data words at the beginning of every data frame. A CPU interrupt would be generated every data frame in this case because the DCI was setup to buffer four data words in a data frame. This configuration represents a typical multi-channel buffering setup.

The DCI can also be configured to buffer more than four data words per frame. For example, assume  $\text{BLEN}\langle 1:0 \rangle = 11b$  (buffer four data words per interrupt) and  $\text{TSCON} = \text{RSCON} = 0x00FF$ . In this configuration, the DCI will transmit/receive 8 data words per data frame. An interrupt will be generated twice per data frame. To determine which portion of the data is in the Transmit/Receive registers at each interrupt, the user will need to check the SLOT status bits ( $\text{DCISTAT}\langle 11:7 \rangle$ ) in the Interrupt Service Routine to determine the current data frame position.

The Transmit and Receive registers are double-buffered, so the DCI module can work on one set of Transmit and Receive data while the user software is manipulating the other set of data. Because of the double-buffers, it will take three interrupt periods to receive the data, process that data, and transmit the processed data. For each DCI interrupt, the CPU will process a data word that was received during a prior interrupt period and generate a data word that will be transmitted during the next interrupt period. The buffering and data processing time of the dsPIC device will insert a two-interrupt period delay into the processed data. This data delay is negligible, in most cases.

The DCI status flags and CPU interrupt indicate that a buffer transfer has taken place and that it is time for the CPU to process more data. In a typical application, the following steps will occur each time the DCI data is processed:

1. The RXBUF registers are read by the user software. The RFUL status bit ( $\text{DCISTAT}\langle 2 \rangle$ ) will have been set by the module to indicate the Receive registers contain new data. The RFUL bit is cleared automatically after all the active Receive registers have been read.
2. The user software will process the received data.
3. The processed data is written to the TXBUF registers. The TMPTY status bit ( $\text{DCISTAT}\langle 0 \rangle$ ) will have been previously set to indicate that the Transmit registers are ready for more data to be written.

For applications that are configured to Transmit and Receive data ( $\text{TSCON}$  and  $\text{RSCON}$  are non-zero), the RFUL and TMPTY status bits can be polled in user software to determine when a DCI buffer transfer takes place. If the DCI is only used to transmit data ( $\text{RSCON} = 0$ ), then the TMPTY bit can be polled to indicate a buffer transfer. If the DCI is configured to only receive data ( $\text{TSCON} = 0$ ), then the RFUL bit can be polled to indicate a buffer transfer.

The DCIIF status bit ( $\text{IFS2}\langle 9 \rangle$ ) is set each time a DCI buffer transfer takes place and generates a CPU interrupt, if enabled. The DCIIF status bit is generated by the logical ORing of the RFUL and TMPTY status bits.

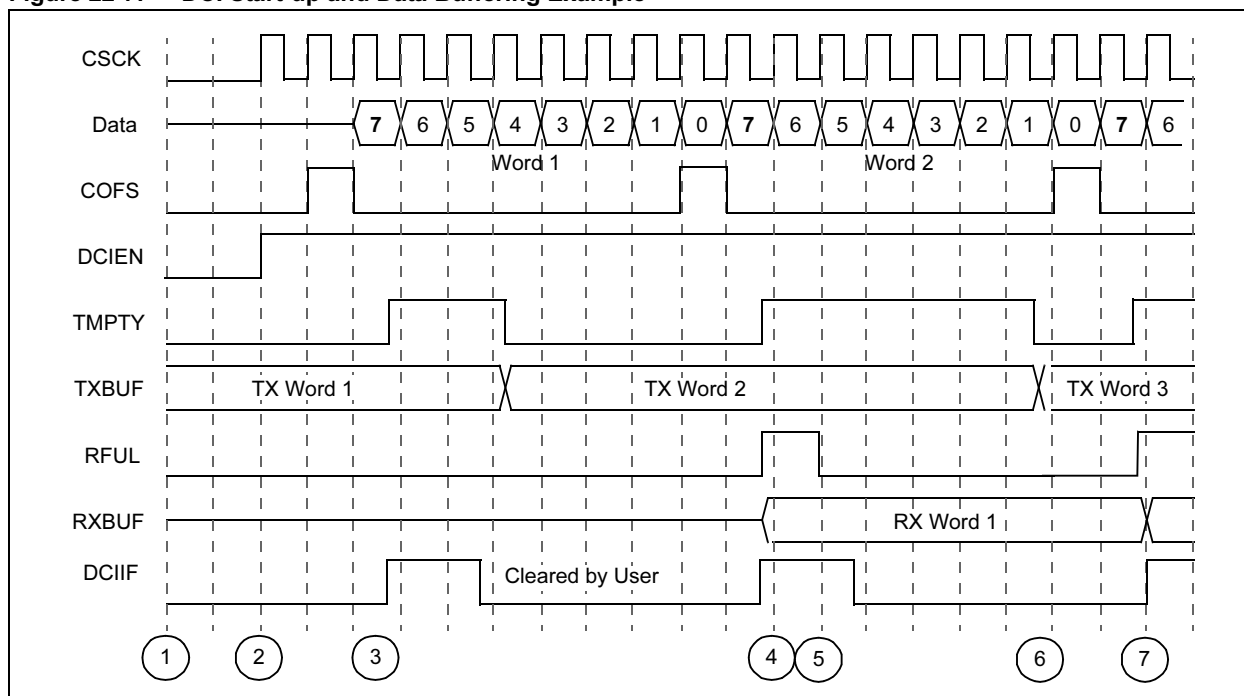
## 22.5.1.1 DCI Start-up and Data Buffering

Data transfers are begun by setting the DCIEN control bit (DCICON1<15>). Prior to this, the DCI Control registers should have been initialized for the desired operating mode. (See **Section 22.5.4 “Multi-Channel Operation”**, **Section 22.5.5 “I<sup>2</sup>S Operation”**, and **Section 22.5.6 “AC-Link Operation”**)

A timing diagram for DCI startup is shown in Figure 22-7. In this example, the DCI is configured for an 8-bit data word (WS<3:0> = 0111b) and an 8-bit data frame (COFSG<3:0> = 0000b). The Multi-Channel mode (COFSM<1:0> = 00b) is used. The steps required to transmit and receive data are described below.

1. The TXBUF registers should be pre-loaded with the first data to be transmitted before the module is enabled. If the transmit data will be based on data received from the codec, then the user can simply clear the TXBUF registers. This will transmit digital ‘silence’ until data is first received into the RXBUF registers from the codec.
2. Enable the DCI module by setting the DCIEN bit (DCICON1<15>). If the DCI is the master device, the data in the TXBUF registers will be transferred to the transmit buffers and transmission of the first data frame will commence. Otherwise, the TXBUF data will be held in the transmit buffers until a frame sync signal is received from the master device.
3. The TMPTY bit will be set immediately after the module is enabled and a DCI interrupt will be generated, if enabled. At this time, the module is ready for the TXBUF registers to be reloaded with data to be transferred on the second data frame. No data has been received by the module at this time, so the TXBUF registers should be cleared again if the transmitted data is calculated from the received data. The DCIIF status bit should be cleared by the user in software if interrupts are enabled.
4. After the first data frame is transferred, the TMPTY bit will set, the RFUL status bit will be set, and a DCI interrupt will occur, if enabled. This is the first data word received from the device connected to the DCI.
5. The user reads the Receive register(s), automatically clearing the RFUL status bit. The user software processes the received data at this time.
6. The Transmit register(s) is written with data to be transmitted during the next data frame. The TMPTY status bit is cleared automatically when the write occurs. The write data may be calculated from data that was received at the prior interrupt.
7. The next DCI interrupt occurs and the cycle repeats.

**Figure 22-7: DCI Start-up and Data Buffering Example**



## 22.5.1.2 DCI Disable

The DCI module is disabled by clearing the DCIEN control bit (DCICON1<15>). When the DCIEN bit is cleared, the module will finish the current data frame transfer that is in progress. An interrupt will be generated if the transmit/receive buffers need to be written/read before the end of the frame.

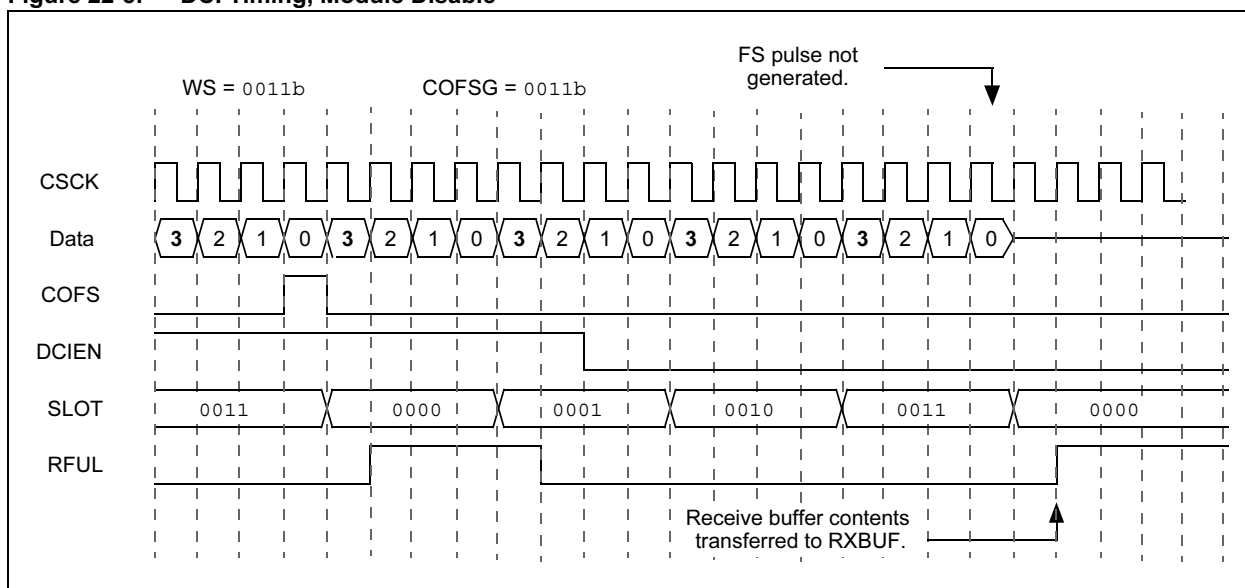
The DCIEN bit must be cleared at least 3 CSCK cycles before the end of the frame disables the module at that frame. If not, the module will disable on the next frame.

The DCI will not generate any further frame sync pulses after the DCIEN bit is cleared, nor will it respond to an incoming frame sync pulse.

When the frame sync generator has reached the final time slot in the data frame, all state machines associated with the DCI will be reset to their Idle state and control of the I/O pins associated with the module will be released. The user may poll the SLOT<3:0> status bits (DCISTAT<11:7>) after the DCIEN bit is cleared to determine when the module is Idle. The DCI is Idle when SLOT<3:0> = 0000b and DCIEN = 0.

When the module enters the Idle state, any data in the Receive Shadow registers will be transferred to the RXBUF registers, and the RFUL and ROV status bits will be affected accordingly.

**Figure 22-8: DCI Timing, Module Disable**



22.5.2 Master vs. Slave Operation

The DCI can be configured for master or slave operation. The master device generates the frame sync signal to initiate a data transfer. The Operating mode (master or slave) is selected by the COFSD control bit (DCICON1<8>).

When the DCI module is operating as a master device (COFSD = 0), the COFSM mode bits determine the type of frame sync pulse that is generated by the frame sync generator logic. A new frame synchronization signal is generated when the frame sync generator resets and is output on the COFS pin.

When the DCI module is operating as a frame sync slave (COFSD = 1), data transfers are controlled by the device attached to the DCI module. The COFSM control bits control how the DCI module responds to incoming FS signals.

In the Multi-Channel mode, a new data frame transfer will begin one serial clock cycle after the COFS pin is sampled high. The pulse on the COFS pin resets the frame sync generator logic.

In the I<sup>2</sup>S mode, a new data word will be transferred one serial clock cycle after a low-to-high or a high-to-low transition is sampled on the COFS pin. A rising or falling edge on the COFS pin resets the frame sync generator logic.

In the AC-Link mode, the tag slot and subsequent data slots for the next frame will be transferred one serial clock cycle after the COFS pin is sampled high.

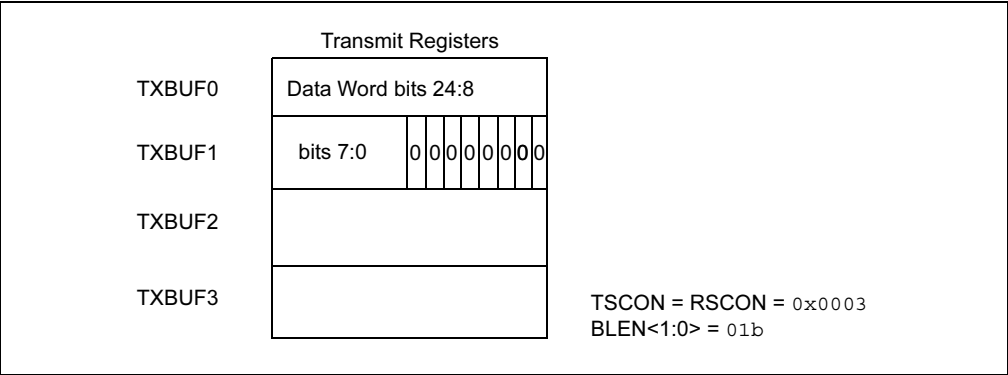
The COFSG and WS bits must be configured to provide the expected frame length when the module is operating in the Slave mode. Once a valid frame sync pulse has been sampled by the module on the COFS pin, an entire data frame transfer will take place. The module will not respond to further frame sync pulses until the current data frame transfer has fully completed.

22.5.3 Data Packing for Long Data Word Support

Many codecs have data word lengths in excess of 16 bits. The DCI natively supports word lengths up to 16 bits, but longer word lengths can be supported by enabling multiple Transmit and Receive slots and packing data into multiple transmit and receive buffer locations. For example, assume that a particular codec transmits/receives 24-bit data words. This data could be transmitted and received by setting BLEN<1:0> = 01b (two data words per interrupt) and setting TSCON = RSCON = 0x0003. This will enable transmission and reception during the first two time slots of the data frame. The 16 MSBs of the transmit data are written to TXBUF0. The 8 LSbs of the transmit data are written left-justified to TXBUF1 as shown in Figure 22-9. The 8 LSbs of TXBUF1 can be written to '0'. The 24-bit data received from the codec will be loaded into RXBUF0 and RXBUF1 with the same format as the transmit data.

Any combination of word size and enabled time slots may be used to transmit and receive long data words in multiple Transmit and Receive registers. For example, the 24 bit data word example shown in Figure 22-9 could be transmitted/received in three consecutive registers by setting WS<3:0> = 0111 (word size = 8 bits), BLEN<1:0> = 10 (buffer three words between interrupts), and TSCON = RSCON = 0x0007 (transmit/receive during the first three time slots of the data frame). Each Transmit and Receive register would contain 8 bits of the data word.

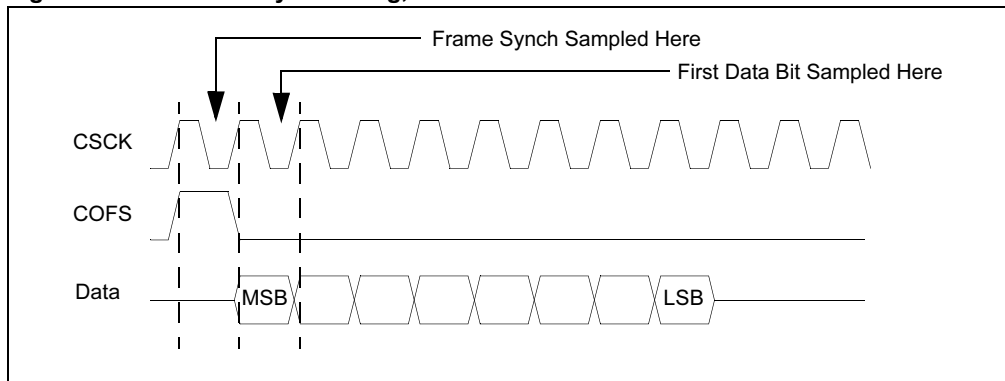
Figure 22-9: Data Packing Example for Long Data Words



## 22.5.4 Multi-Channel Operation

The Multi-Channel mode ( $\text{COFSM}\langle 1:0 \rangle = 00$ ) is used for codecs that require a frame sync pulse that is driven high for one serial clock period to initiate a data transfer. One or more data words can be transferred in the data frame. The number of clock cycles between successive frame sync pulses will depend on the device connected to the DCI module. A timing diagram for the frame sync signal in Multi-Channel mode is shown in Figure 22-10. A timing example, indicating a four-word data transfer is also shown in Figure 22-2.

**Figure 22-10: Frame Sync Timing, Multi-Channel Mode**



### 22.5.4.1 Multi-Channel Setup Details

The steps required to configure the DCI for a codec using the Multi-Channel mode are provided in this section. This Operating mode can be used for codecs with one or more data channels. The setup is similar regardless of the number of channels.

For this setup example, a hypothetical codec will be considered. The single channel codec used for this setup example will use a 256 fs serial clock frequency with a 16-bit data word transmitted at the beginning of each frame.

The steps required for setup and operation are described below.

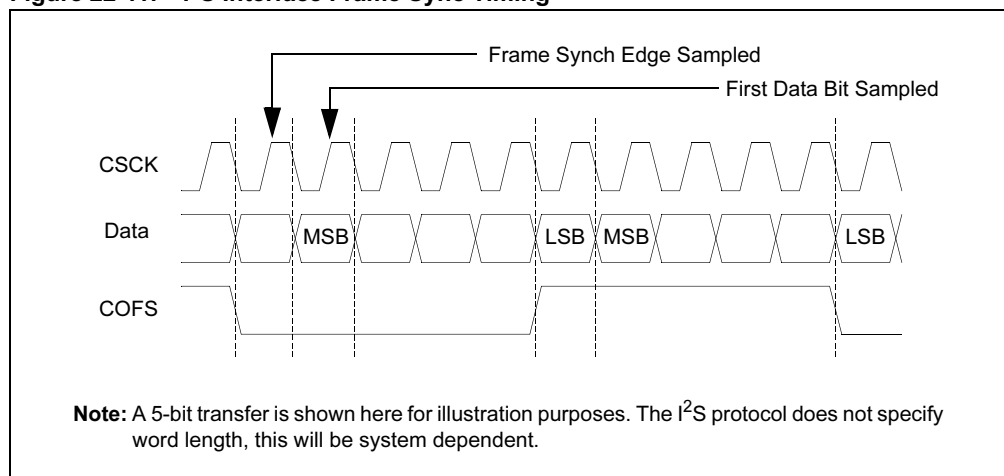
1. Determine the sample rate and data word size required by the codec. An 8 kHz sampling rate is assumed for this example.
2. Determine the serial transfer clock frequency required by the codec. Most codecs require a serial clock signal that is some multiple of the sampling frequency. The example codec requires a frequency that is 256 fs, or 1.024 MHz. Therefore, a frame sync pulse must be generated every 256 serial clock cycles to start a data transfer.
3. The DCI must be configured for the serial transfer clock. If the CSCK signal will be generated by the DCI, clear the CSCKD control bit ( $\text{DCICON1}\langle 10 \rangle$ ) and write a value to  $\text{DCICON3}$  that will produce the correct clock frequency (See **Section 22.4.3 “Bit Clock Generator”**). If the CSCK signal is generated by the codec or other external source, set the CSCKD control bit and clear the  $\text{DCICON3}$  register.
4. Clear the  $\text{COFSM}\langle 1:0 \rangle$  control bits ( $\text{DCICON1}\langle 1:0 \rangle$ ) to set the frame synchronization signal to Multi-Channel mode.
5. If the DCI will generate the frame sync signal (master), then clear the COFSD control bit ( $\text{DCICON1}\langle 8 \rangle$ ). If the DCI will receive the frame sync signal (slave), then set the COFSD control bit.
6. Clear the CSCKE control bit ( $\text{DCICON1}\langle 9 \rangle$ ) to sample incoming data on the falling edge of CSCK. This is the typical configuration for most codecs. Refer to the codec data sheet to ensure the correct sampling edge is used.
7. Write the  $\text{WS}\langle 3:0 \rangle$  control bits ( $\text{DCICON2}\langle 3:0 \rangle$ ) for the desired data word size. The example codec requires  $\text{WS}\langle 3:0 \rangle = 1111\text{b}$  for a 16-bit data word size.

8. Write the COFSG<3:0> control bits (DCICON2<8:5>) for the desired number of data words per frame. The WS and COFSG control bits will determine the length of the data frame in CCLK cycles (see **Section 22.4.7 “Frame Synchronization Generator”**) COFSG<3:0> = 1111b is used for this codec to provide the 256-bit data frame required by the example codec.
9. Set the Output mode for the CSDO pin using the CSDOM control bit (DCICON1<6>). If a single device is attached to the DCI, CSDOM can be cleared. This will force the CSDO pin to '0' during unused data time slots. You may need to set CSDOM if multiple devices are attached to the CSDO pin.
10. Write the TSCON and RSCON registers to determine which data time slots in the frame are to be transmitted and received, respectively. For this single channel codec, use TSCON = RSCON = 0x0001 to enable transmission and reception during the first 16-bit time slot of the data frame.
11. Set the BLEN control bits (DCICON2<11:10>) to buffer the desired amount of data words. For the single channel codec, BLEN = 00 will provide an interrupt at each data frame. A higher value of BLEN could be used for this codec to buffer multiple samples between interrupts.
12. If interrupts are to be used, clear the DCIIF status bit (IFS2<9>) and set the DCIIE control bit (IEC2<9>).
13. Begin operation as described in **Section 22.5.1.1 “DCI Start-up and Data Buffering”**.

## 22.5.5 I<sup>2</sup>S Operation

The I<sup>2</sup>S Operating mode is used for codecs that require a frame sync signal that has a 50% duty cycle. The period of the I<sup>2</sup>S frame sync signal in serial clock cycles is determined by the word size of the codec that is connected to the DCI module. The start of a new word boundary is marked by a high-to-low or a low-to-high transition edge on the COFS pin as shown in Figure 22-11. I<sup>2</sup>S codecs are generally stereo or two-channel devices, with one data word transferred during the low time of the frame sync signal and the other data word transmitted during the high time.

**Figure 22-11: I<sup>2</sup>S Interface Frame Sync Timing**



The DCI module is configured for I<sup>2</sup>S mode by writing a value of 01h to the COFSM<1:0> control bits in the DCICON1 SFR. When operating in the I<sup>2</sup>S mode, the DCI module will generate frame synchronization signals with a 50% duty cycle. Each edge of the frame synchronization signal marks the boundary of a new data word transfer. Refer to the Appendix of this manual for more information about the I<sup>2</sup>S protocol. The user must also select the frame length and data word size using the COFSG and WS control bits in the DCICON2 SFR.

### 22.5.5.1 I<sup>2</sup>S Setup Details

The steps required to configure the DCI for an I<sup>2</sup>S codec are provided in this section. For this setup example, a hypothetical I<sup>2</sup>S codec will be considered.

The I<sup>2</sup>S codec in this setup example will use a 64 fs serial clock frequency, with two 16 bit data words during the data frame. Therefore, the frame length will be 64 CSCK cycles, with the COFS signal high for 32 cycles and low for 32 cycles. The first data word will be transmitted one CSCK cycle after the falling edge of COFS, and the second data word will be transmitted one CSCK cycle after the rising edge of COFS as shown in Figure 22-11.

1. Determine the sample rate used by the codec to determine the CSCK frequency. It is assumed in this example that fs is 48 kHz.
2. Determine the serial transfer clock frequency required by the codec. The example codec requires a frequency that is 64 fs, or 3.072 MHz.
3. The DCI must be configured for the serial transfer clock. If the CSCK signal will be generated by the DCI, clear the CSCKD control bit (DCICON1<10>) and write a value to DCICON3 that will produce the correct clock frequency (see **Section 22.4.3 “Bit Clock Generator”**). If the CSCK signal is generated by the codec or other external source, set the CSCKD control bit and clear the DCICON3 register.
4. Next, set COFSM<1:0> = 01b to set the frame synchronization signal to I<sup>2</sup>S mode.
5. If the DCI will generate the frame sync signal (master), then clear the COFSD control bit (DCICON1<8>). If the DCI will receive the frame sync signal (slave), then set the COFSD control bit.
6. Set the CSCKE control bit (DCICON1<9>) to sample incoming data on the rising edge of CSCK. This is the typical configuration for most I<sup>2</sup>S codecs.
7. Write the WS<3:0> control bits (DCICON2<3:0>) for the desired data word size. For the example codec, use WS<3:0> = 1111b for a 16-bit data word size.
8. Write the COFSG<3:0> control bits (DCICON2<8:5>) for the desired number of data words per frame. The WS and COFSG control bits will determine the length of the data frame in CSCK cycles (see **Section 22.4.7 “Frame Synchronization Generator”**). For this example codec, set COFSG<3:0> = 0001b.

**Note:** In the I<sup>2</sup>S mode, the COFSG bits are set to the length of 1/2 of the data frame. For this example codec, set COFSG<3:0> = 0001b (two data words per frame) to produce a 32-bit frame. This will produce an I<sup>2</sup>S data frame that is 64 bits in length.

9. Set the Output mode for the CSDO pin using the CSDOM control bit (DCICON1<6>). If a single device is attached to the DCI, CSDOM can be cleared. You may need to set CSDOM if multiple devices are attached to the CSDO pin.
10. Write the TSCON and RSCON registers to determine which data time slots in the frame are to be transmitted and received, respectively. For this codec, set TSCON = 0x0001 and RSCON = 0x0001 to enable transmission and reception during the first 16-bit time slot of the 32-bit data frame. Adjacent time slots can be enabled to buffer data words longer than 16 bits.
11. Set the BLEN<1:0> control bits (DCICON2<11:10>) to buffer the desired amount of data words. For a two-channel I<sup>2</sup>S codec, BLEN<1:0> = 01b will generate an interrupt after transferring two data words.
12. If interrupts are to be used, clear the DCIIF status bit (IFS2<9>) and set the DCIIE control bit (IEC2<9>).
13. Begin operation as described in **Section 22.5.1.1 “DCI Start-up and Data Buffering”**. In the I<sup>2</sup>S Master mode, the COFS pin will be driven high after the module is enabled and begin transmitting the data loaded in TXBUF0.

## 22.5.5.2 How to Determine the I<sup>2</sup>S Channel Alignment

Most I<sup>2</sup>S codecs support two channels of data and the level of the frame sync signal indicates the channel that is transferred during that half of the data frame. The COFS pin can be polled in software using its associated Port register to determine the present level on the pin in the DCI Interrupt Service Routine. This will indicate which data is in the Receive register and which data should be written to the Transmit registers for transfer on the next frame.

## 22.5.5.3 I<sup>2</sup>S Data Justification

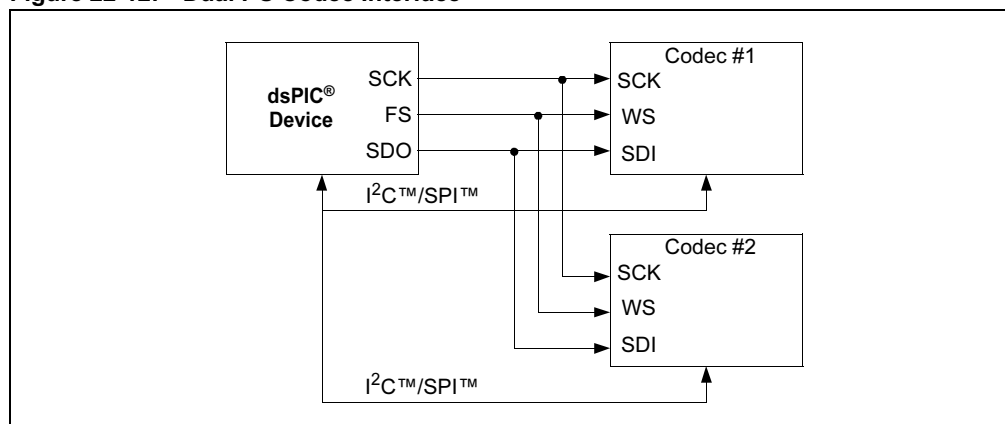
As per the I<sup>2</sup>S specification, a data word transfer will by default begin one serial clock cycle following a transition of the frame sync signal. An 'MSb left-justified' option can be selected using the DJST control bit (DCICON1<5>).

If DJST = 1, the I<sup>2</sup>S data transfers will be MSb left justified. The MSb of the data word will be presented on the CSDO pin during the same serial clock cycle as the rising or falling edge of the FS signal. After the data word has been transmitted, the state of the CSDO pin is dictated by the CSDOM (DCICON1<6>) bit.

The left-justified data option allows two stereo codecs to be connected to the same serial bus. Many I<sup>2</sup>S compatible devices have configuration options for left-justified or right-justified data. The word size selection bits are set to twice the codec word length and data is read/written to the DCI memory in a packed format. The connection details for a dual I<sup>2</sup>S codec system are shown in Figure 22-12.

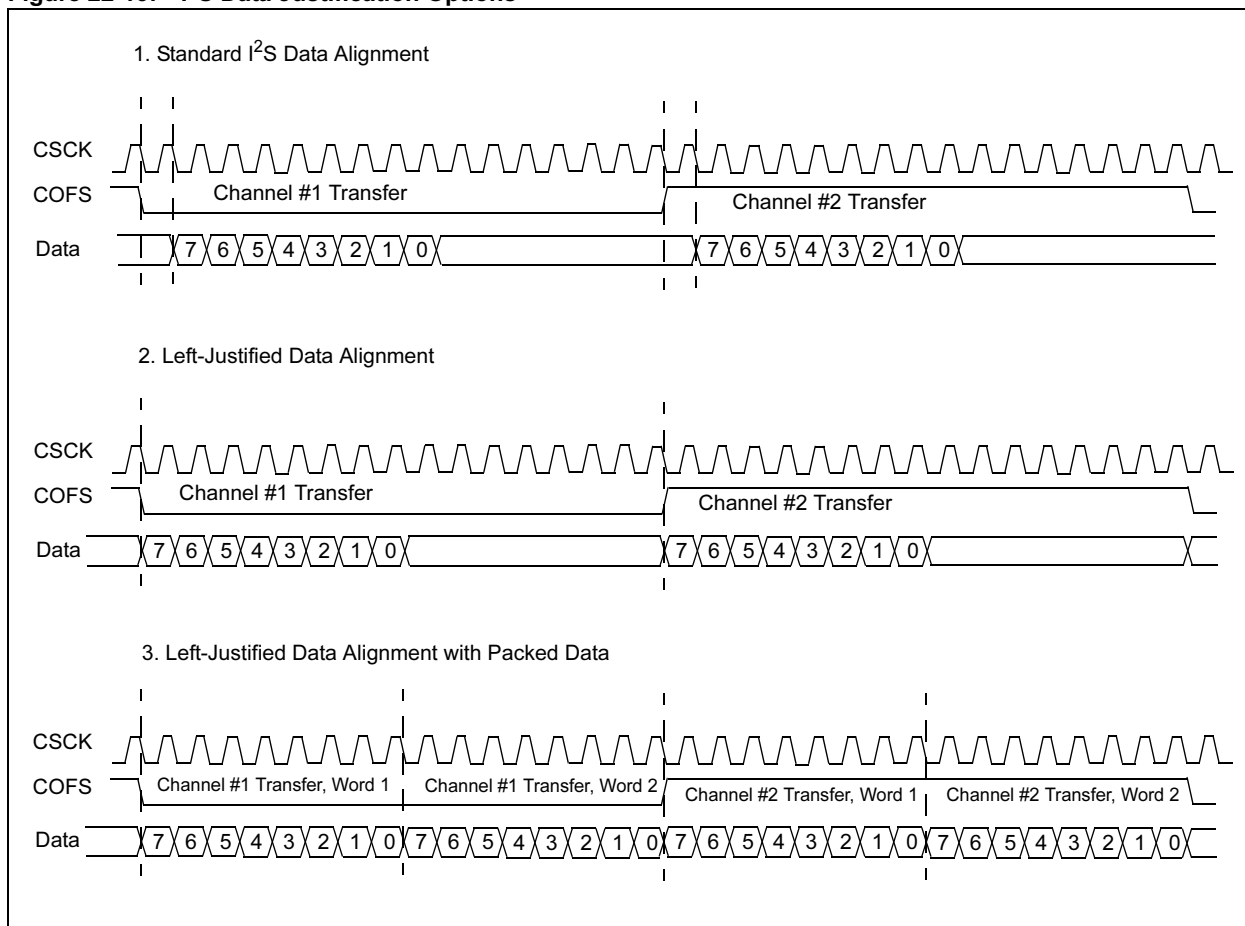
Timing diagrams for I<sup>2</sup>S mode are shown in Figure 22-13. For reference, these diagrams assume an 8-bit word size (WS<3:0> = 0111b). Two data words per frame would be required to achieve a 16-bit sub-frame (COFSG<3:0> = 0001b). The 3rd timing diagram in Figure 22-13 uses packed data to read/write from two codecs. For this example, the DCI module is configured for a 16-bit data word (WS<3:0> = 1111b). Two packed 8-bit words are written to each 16-bit location in the DCI memory buffer.

**Figure 22-12: Dual I<sup>2</sup>S Codec Interface**





**Figure 22-13: I<sup>2</sup>S Data Justification Options**



## 22.5.6 AC-Link Operation

This section describes how to use the DCI in the AC-Link modes. The AC-Link modes are used to communicate with AC-'97 compliant codec devices.

### 22.5.6.1 AC-Link Data Frame

The AC-Link data frame is 256 bits subdivided into one 16-bit control slot, followed by twelve 20-bit data slots. The AC-'97 codec usually provides the serial transfer clock signal which is derived from a crystal oscillator as shown in Figure 22-14. The controller receives the serial clock and generates the frame sync signal. The default data frame rate is 48 kHz. The frame sync signal used for AC-Link systems is high for 16 CCLK periods at the beginning of the data frame and low for 240 CCLK periods. The data transfer begins one CCLK period after the rising edge of the frame sync signal as shown in Figure 22-16. Data is sampled by the receiving device on the falling edge of CCLK. The control and data time slots in the AC-Link have defined uses in the protocol as shown in Figure 22-15. Refer to the Appendix of this manual or the Intel® AC '97 Codec Specification, Rev 2.2 for a complete definition of the AC-Link protocol.

Figure 22-14: AC-Link Signal Connections

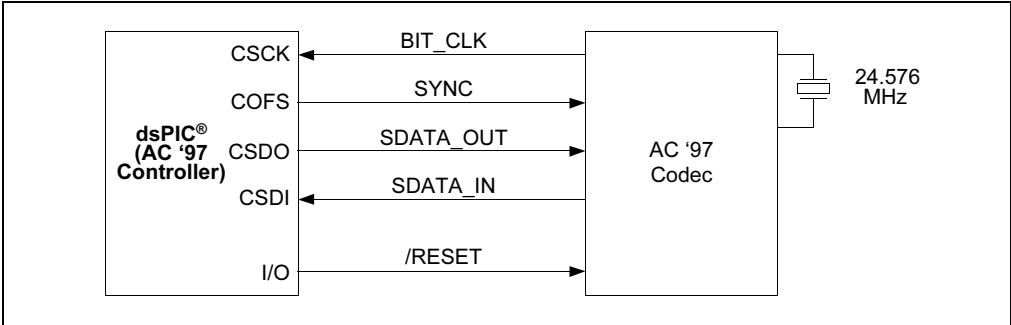


Figure 22-15: AC-Link Data Frame

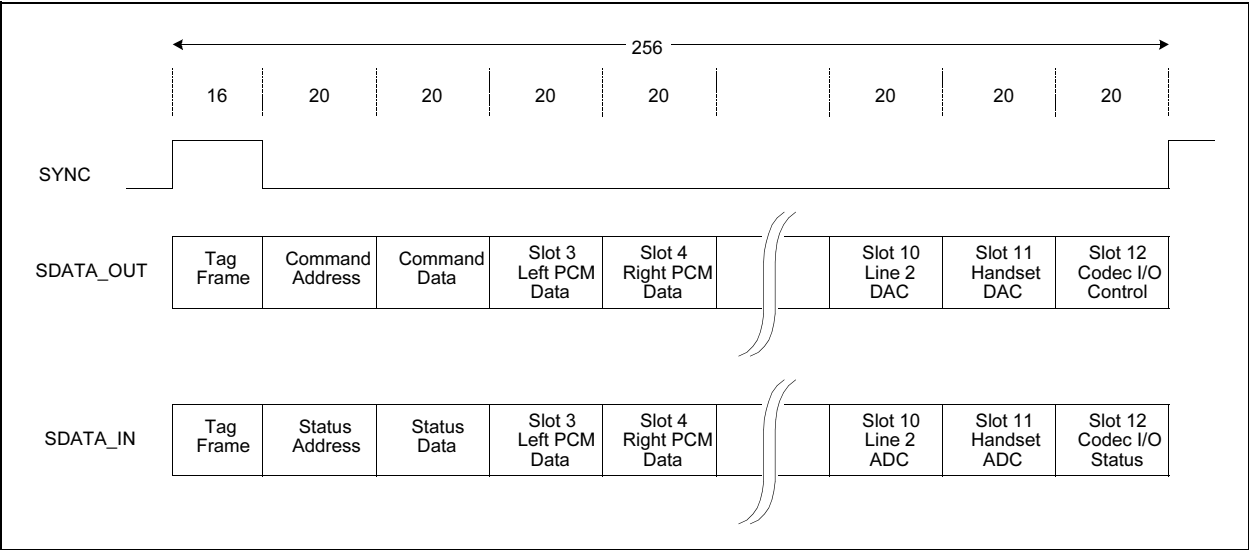
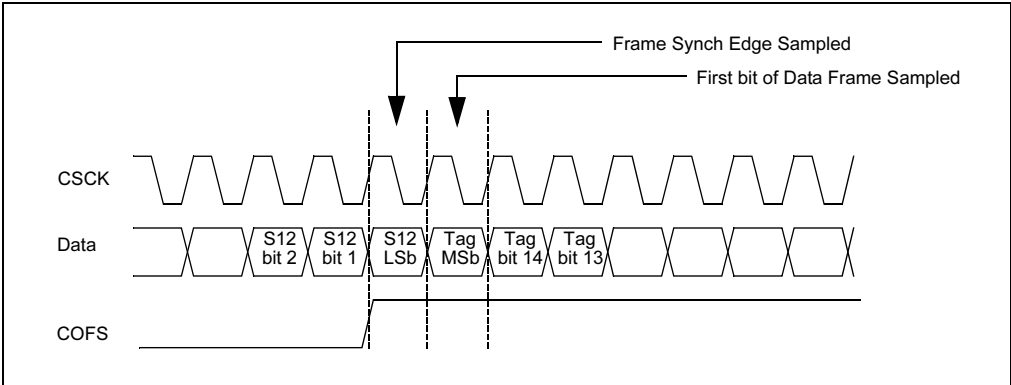


Figure 22-16: Frame Sync Timing, AC-Link Start of Frame



The DCI module has two Operating modes for the AC-Link protocol to accommodate the 20-bit data time slots. These Operating modes are selected by the COFSM<1:0> control bits (DCICON1<1:0>). The first AC-Link mode is called '16-bit AC-Link mode' and is selected by setting COFSM<1:0> = 10b. The second AC-Link mode is called '20-bit AC-Link mode' and is selected by setting COFSM<1:0> = 11b.

### 22.5.6.2 16-bit AC-Link Mode

In the 16-bit AC-Link mode, transmit and receive data word lengths are restricted to 16 bits to fit the DCI Transmit and Receive registers. Note that this restriction only affects the 20-bit data time slots of the AC-Link protocol. For received time slots, the incoming data will be truncated to 16 bits. For outgoing time slots, the 4 LSBs of the data word are set to '0' by the module. This Operating mode simplifies the AC-Link data frame by treating every time slot as a 16-bit time slot. The frame sync generator maintains alignment to the time slot boundaries.

### 22.5.6.3 20-bit AC-Link Mode

The 20-bit AC-Link mode allows all bits in the data time slots to be transmitted and received, but does not maintain data alignment to the specific time slot boundaries defined in the AC-Link protocol.

The 20-bit AC-Link mode functions similarly to the Multi-Channel mode of the DCI module, except for the duty cycle of the frame synchronization signal that is produced. The AC-Link frame synchronization signal should remain high for 16 clock cycles and should be low for the following 240 cycles.

The 20-bit mode treats each 256-bit AC-Link frame as sixteen 16-bit time slots. In the 20-bit AC-Link mode, the module operates as if COFSG<3:0> = 1111b and WS<3:0> = 1111b. The data alignment for 20-bit data slots is not maintained in this Operating mode. For example, an entire 256-bit AC-Link data frame can be transmitted and received in a packed fashion by setting all bits in the TSCON and RSCON registers. Since the total available buffer length is 64 bits, it would take 4 consecutive interrupts to transfer the AC-Link frame. The application software must keep track of the current AC-Link frame segment by monitoring the SLOT<3:0> status bits (DCISTAT<11:7>).

### 22.5.6.4 AC-Link Setup Details

The module is enabled for AC-Link mode by writing 10h or 11h to the COFSM<1:0> control bits in the DCICON1 SFR. The word size selection bits (WS<3:0>) and the frame synchronization generator bits (COFSG<3:0>) have no effect for the 16 and 20-bit AC-Link modes since the frame and word sizes are set by the protocol.

Most AC '97 codecs generate the clock signal that controls data transfers. Therefore, the CSECKD control bit is set in software. The COFSD control bit is cleared because the DCI will generate the FS signal from the incoming clock signal. The CSCKE bit is cleared so that data is sampled on the rising edge.

The user must decide which time slots in the AC-Link data frame are to be buffered and set the TSE and RSE control bits accordingly. At a minimum, it will be necessary to buffer the transmit and receive TAG slots, so the TSCON<0> and RSCON<1> control bits should be set in software.

**Note:** Only the TSCON<12:0> control bits and the RSCON<12:0> control bits will have an effect in the 16-bit AC-Link mode, since an AC-Link frame has 13 time slots.

1. The DCI must be configured to accept the serial transfer clock from the AC '97 codec. Set the CSECKD control bit and clear the DCICON3 register.
2. Next, set the COFSM<1:0> control bits (DCICON1<1:0>) to 10b or 11b to set the desired AC-Link Frame Synchronization mode.
3. Clear the COFSD control bit (DCICON1<8>), so the DCI will output the frame sync signal.
4. Clear the CSCKE control bit (DCICON1<9>) to sample incoming data on the falling edge of CSCK.

**Note:** The word size selection bits (WS<3:0>) and the frame synchronization generator bits (COFSG<3:0>) have no effect for the 16- and 20-bit AC-Link modes, since the frame and word sizes are set by the protocol.

5. Clear the CSDOM control bit (DCICON1<6>).
6. Write the TSCON and RSCON registers to determine which data time slots in the frame are to be transmitted and received, respectively. This will depend on which data time slots in the AC-Link protocol will be used. At a minimum, communication on slot #0 (Tag Slot) is required. Refer to the discussion in **Section 22.5.6.2 “16-bit AC-Link Mode”**, **Section 22.5.6.3 “20-bit AC-Link Mode”** and **Section 26. “Appendix”** of this manual for additional information.
7. Set the BLEN control bits (DCICON2<11:10>) to buffer the desired amount of data words. For the single channel codec, BLEN = 00 will provide an interrupt at each data frame. A higher value of BLEN could be used for this codec to buffer multiple samples between interrupts.
8. If interrupts are to be used, clear the DCIIF status bit (IFS2<9>) and set the DCIIE control bit (IEC2<9>).
9. Begin operation as described in **Section 22.5.1.1 “DCI Start-up and Data Buffering”**.

## 22.6 Operation in Power Saving Modes

### 22.6.1 CPU Idle Mode

The DCI module may optionally continue to operate while the CPU is in Idle mode. The DCISIDL control bit (DCICON1<13>) determines whether the DCI module will operate when the CPU is in Idle mode. If the DCISIDL control bit is cleared (default), the module will continue to operate normally in Idle mode. If the DCISIDL bit is set, the module will halt when the CPU enters Idle mode.

### 22.6.2 Sleep Mode

The DCI will not operate while the device is in Sleep mode if the CSCK signal is derived from the device instruction clock, Tcy.

However, the DCI module has the ability to operate while in Sleep mode and wake the CPU when the CSCK signal is supplied by an external device (CSCKD = 1). The DCI interrupt enable bit, DCIIE, must be set to allow a wake-up event from Sleep mode. When the DCI interrupt flag, DCIIF is set, the device will wake from Sleep mode. If the DCI interrupt priority level is greater than the current CPU priority, program execution will resume from the DCI ISR. Otherwise, execution will resume with the instruction following the PWRSAV instruction that previously entered Sleep mode.

## 22.7 Registers Associated with DCI

Table 22-1 lists the registers associated with the DCI module.

Table 22-1: DCI Register Map

Name	Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on all Resets
IFS2	0088	—	—	—	FLTBIF	FLTAIF	LVDIF	DCIIF	QEIIIF	PWMIF	C2IF	INT4IF	INT3IF	OC8IF	OC7IF	OC6IF	OC5IF	0000 0000 0000 0000
IEC2	0090	—	—	—	FLTBIE	FLTAIE	LVDIE	DCIIE	QEIIIE	PWMIIE	C2IE	INT4IE	INT3IE	OC8IE	OC7IE	OC6IE	OC5IE	0000 0000 0000 0000
IPC10	00A8	—	—	FLTAIP<2:0>	—	—	LVDIP<2:0>	—	—	—	—	DCIIP<2:0>	—	—	—	—	—	0100 0100 0100 0100
DCICON1	240	DCIEN	—	DCISIDL	—	DLOOP	CSCKD	CSCKE	COFSD	UNFM	SDOM	DJST	—	—	—	COFSM<1:0>	—	000- -000 000- -000
DCICON2	242	—	—	—	—	—	—	—	—	COFSG<3:0>	—	—	—	—	—	WS<3:0>	—	---- 00-0 000- 0000
DCICON3	244	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	---- 0000 0000 0000
DCISTAT	246	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	---- 0000 0000 0000
TSCON	248	TSE15	TSE14	TSE13	TSE12	TSE11	TSE10	TSE9	TSE8	TSE7	TSE6	TSE5	TSE4	TSE3	TSE2	TSE1	TSE0	0000 0000 0000 0000
RSCON	24C	RSE15	RSE14	RSE13	RSE12	RSE11	RSE10	RSE9	RSE8	RSE7	RSE6	RSE5	RSE4	RSE3	RSE2	RSE1	RSE0	0000 0000 0000 0000
RXBUF0	250	Receive #0 Data Register																uuuu uuuu uuuu uuuu
RXBUF1	252	Receive #1 Data Register																uuuu uuuu uuuu uuuu
RXBUF2	254	Receive #2 Data Register																uuuu uuuu uuuu uuuu
RXBUF3	256	Receive #3 Data Register																uuuu uuuu uuuu uuuu
TXBUF0	258	Transmit #0 Data Register																0000 0000 0000 0000
TXBUF1	25A	Transmit #1 Data Register																0000 0000 0000 0000
TXBUF2	25C	Transmit #2 Data Register																0000 0000 0000 0000
TXBUF3	25E	Transmit #3 Data Register																0000 0000 0000 0000

Legend: r = Reserved, x = Unknown, u = Unchanged.

Note: Grayed locations indicate reserved space in SFR map for future module expansion. Read reserved locations as '0's.

## 22.8 Design Tips

**Question 1:** *Can the DCI support data word lengths greater than 16-bits?*

**Answer:** Yes. A long data word can be transmitted and received using multiple Transmit and Receive registers. See **Section 22.5.3 “Data Packing for Long Data Word Support”** for details.

### 22.9 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Data Converter Interface (DCI) module are:

Title	Application Note #
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No related application notes at this time.

<b>Note:</b> Please visit the Microchip web site ( <a href="http://www.microchip.com">www.microchip.com</a> ) for additional Application Notes and code examples for the dsPIC30F Family of devices.
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## 22.10 Revision History

### **Revision A**

This is the initial released revision of this document.

### **Revision B**

This revision incorporates additional technical content and changes for the dsPIC30F Data Converter Interface (DCI) module.

### **Revision C**

This revision incorporates all known errata at the time of this document update.