Section 16. Quadrature Encoder Interface (QEI)

HIGHLIGHTS

This section of the manual contains the following topics:

> **Note:**   This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC30F devices.
>
> Please consult the note at the beginning of the **"Quadrature Encoder Interface (QEI)"** chapter in the current device data sheet to check whether this document supports the device you are using.
>
> Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

16.1   Introduction

16.1.1   Features Overview

Quadrature encoders, also known as incremental encoders or optical encoders, are used in the position and speed detection of rotating motion systems. Quadrature encoders enable closed-loop control of many motor control applications, such as Switched Reluctance (SR) motors and AC Induction Motors (ACIMs).

A typical incremental encoder includes a slotted wheel attached to the shaft of the motor and an emitter/detector module sensing the slots in the wheel. Typically, three output channels, Phase A, Phase B and Index pulse, provide the information on the movement of the motor shaft, including distance and direction.

The two channels, Phase A (QEA) and Phase B (QEB), have a unique relationship. If Phase A leads Phase B, the direction (of the motor) is deemed positive or forward. If Phase A lags Phase B, the direction (of the motor) is deemed negative or reverse. A third channel, termed Index (INDX) pulse, occurs once per revolution and is used as a reference to establish an absolute position. See Figure 16-1 for a relative timing diagram of these three signals.

The quadrature signals produced by the encoder can have four unique states. These states are indicated for one count cycle in Figure 16-1. The order of the states are reversed when the direction of travel is changed.

A quadrature decoder captures the phase signals and the index pulse, and converts the information into a numeric count of the position pulses. Generally, the count will increment when the shaft is rotating one direction and decrement when the shaft is rotating in the other direction.

**Figure 16-1: Quadrature Encoder Interface Signals**
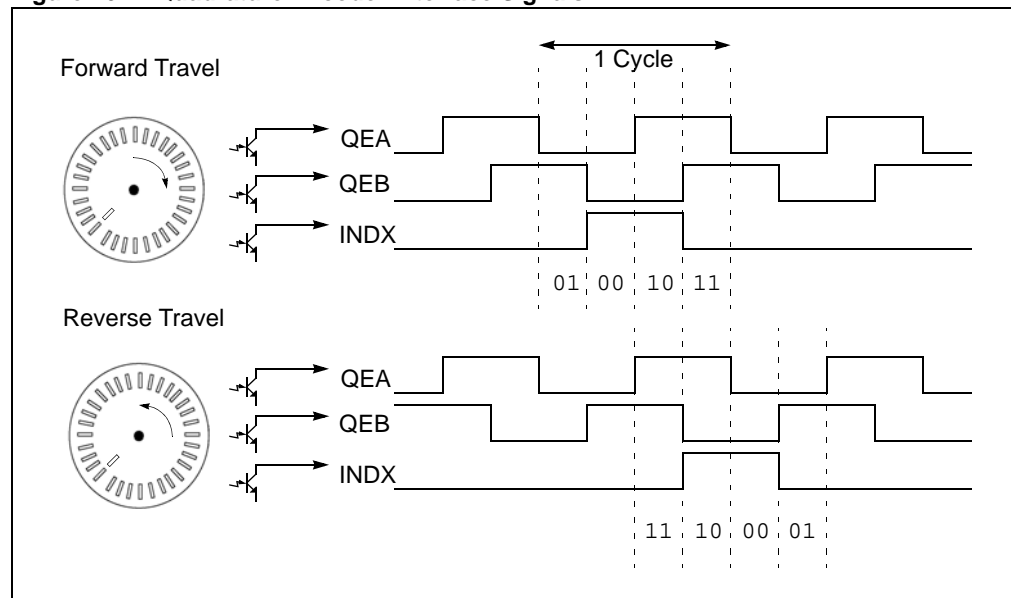
Section 16. Quadrature Encoder Interface (QEI)

The Quadrature Encoder Interface (QEI) module provides an interface to incremental encoders. The QEI module consists of quadrature decoder logic to interpret the Phase A and Phase B signals and an up/down counter to accumulate the count. The digital filters on the inputs, conditions the input signal. The QEI module also contains the UPDN signal, which represents the QEA and QEB time relationship. Figure 16-2 is a simplified block diagram of the QEI module.

The QEI module includes:

- Three input pins for two phase signals and index pulse
- Programmable digital noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- 16-bit up/down position counter
- Count direction status
- x2 and x4 count resolution
- Two modes of position counter reset
- General Purpose 16-bit Timer mode/Counter mode
- Interrupts generated by QEI or counter events

Figure 16-2:   Quadrature Encoder Interface Module Simplified Block Diagram
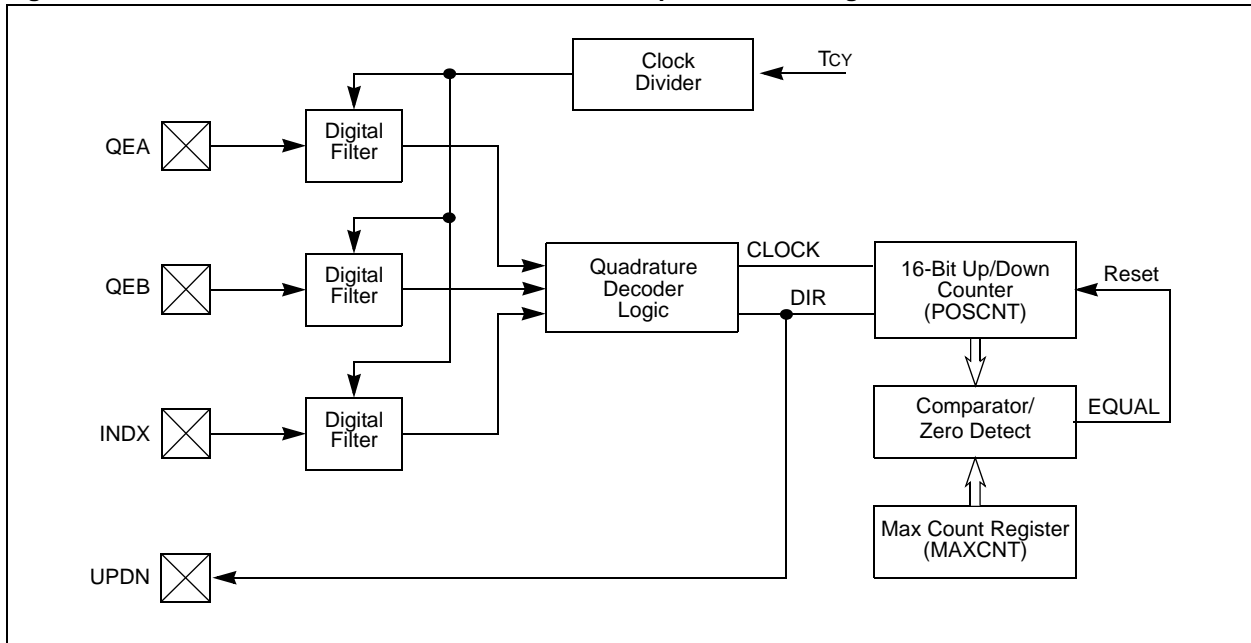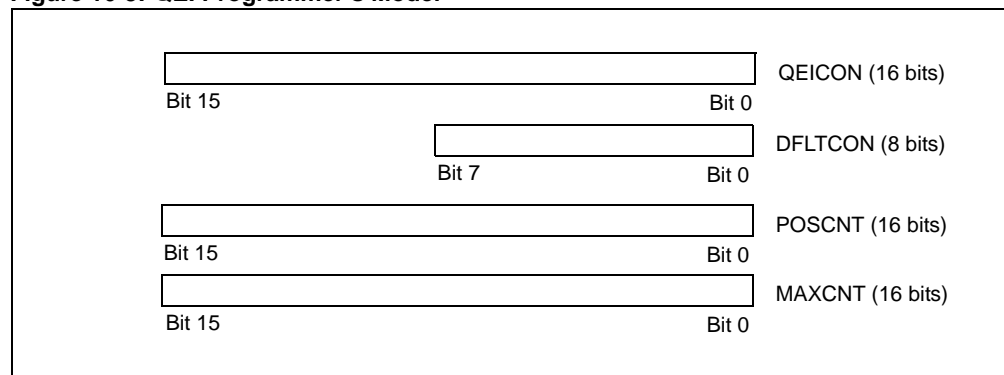
16.2   Control and Status Registers

The QEI module has the following four user-accessible registers. Figure 16-3 illustrates the registers that are accessible in either Byte mode or Word mode.

- Control/Status Register (QEICON) – Allows control of the QEI operation and status flags indicating the module state.
- Digital Filter Control Register (DFLTCON) – Allows control of the digital input filter operation.
- Position Count Register (POSCNT) – Allows reading and writing of the 16-bit position counter.
- Maximum Count Register (MAXCNT) – Holds a value that will be compared to the POSCNT counter in some operations.

> **Note:** The POSCNT register allows byte access. However, reading the register in Byte mode may result in partially updated values in subsequent reads. Either use Word mode reads/writes or ensure that the counter is not counting during byte operations.

Figure 16-3: QEI Programmer's Model

	QEICON (16 bits)
Bit 15 .... Bit 0	
	DFLTCON (8 bits)
Bit 7 ...... Bit 0	
	POSCNT (16 bits)
Bit 15 .... Bit 0	
	MAXCNT (16 bits)
Bit 15 .... Bit 0	

Section 16. Quadrature Encoder Interface (QEI)

Register 16-1: QEICON: QEI Control Register

Upper Byte:

R/W-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
CNTERR	—	QEISIDL	INDEX	UPDN		QEIM<2:0>	

bit 15   bit 8

Lower Byte:

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SWPAB	PCDOUT	TQGATE	TQCKPS<1:0>		POSRES	TQCS	UDSRC

bit 7   bit 0

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Quadrature Encoder Interface (QEI)

bit 15 **CNTERR:** Count Error Status Flag bit
`1` = Position count error is occurred
`0` = Position count error is not occurred
(CNTERR flag only applies when QEIM<2:0> = `110` or `100`)

bit 14 **Unimplemented:** Read as '`0`'

bit 13 **QEISIDL:** Stop in Idle Mode bit
`1` = Discontinue module operation when device enters Idle mode
`0` = Continue module operation in Idle mode

bit 12 **INDEX:** Index Pin State Status bit (read-only)
`1` = Index pin is high
`0` = Index pin is low

bit 11 **UPDN:** Position Counter Direction Status bit
`1` = Position counter direction is positive (+)
`0` = Position counter direction is negative (-)
    (Read-only bit when QEIM<2:0> = `1xx`)
    (Read/Write bit when QEIM<2:0> = `001`)

bit 10-8 **QEIM<2:0>:** Quadrature Encoder Interface Mode Select bits
`111` = Quadrature Encoder Interface enabled (x4 mode) with position counter reset by match (MAXCNT)
`110` = Quadrature Encoder Interface enabled (x4 mode) with index pulse reset of position counter
`101` = Quadrature Encoder Interface enabled (x2 mode) with position counter reset by match (MAXCNT)
`100` = Quadrature Encoder Interface enabled (x2 mode) with index pulse reset of position counter
`011` = Unused (module disabled)
`010` = Unused (module disabled)
`001` = Starts 16-bit Timer
`000` = Quadrature Encoder Interface/Timer off

bit 7 **SWPAB:** Phase A and Phase B Input Swap Select bit
`1` = Phase A and Phase B inputs are swapped
`0` = Phase A and Phase B inputs are not swapped

bit 6 **PCDOUT:** Position Counter Direction State Output Enable bit
`1` = Position counter direction status output is enabled (QEI logic controls state of I/O pin)
`0` = Position counter direction status output is disabled (Normal I/O pin operation)

bit 5 **TQGATE:** Timer Gated Time Accumulation Enable bit
`1` = Timer gated time accumulation is enabled
`0` = Timer gated time accumulation is disabled

bit 4-3 **TQCKPS<1:0>:** Timer Input Clock Prescale Select bits
`11` = 1:256 prescale value
`10` = 1:64 prescale value
`01` = 1:8 prescale value
`00` = 1:1 prescale value
(Prescaler utilized for 16-bit Timer mode only)

Register 16-1:   QEICON: QEI Control Register (Continued)

bit 2   **POSRES:** Position Counter Reset Enable bit
            1 = Index pulse resets position counter
            0 = Index pulse does not reset position counter
            (Bit only applies when QEIM<2:0> = 100 or 110)

bit 1   **TQCS:** Timer Clock Source Select bit
            1 = External clock from pin QEA (on the rising edge)
            0 = Internal clock (T$_{CY}$)

bit 0   **UDSRC:** Position Counter Direction Selection Control bit
            1 = QEB pin state defines position counter direction
            0 = Control/Status bit, UPDN (QEICON<11>), defines timer counter (POSCNT) direction

      Note: When configured for QEI mode, this control bit is a 'don't care'.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

Register 16-2:   DFLTCON: Digital Filter Control Register (dsPIC30F6010 Only)

Upper Byte:

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	CEID

bit 15   bit 8

Lower Byte:

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEOUT	QECK<2:0>			INDOUT	INDCK<2:0>		

bit 7   bit 0

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Quadrature Encoder Interface (QEI)

bit 15-9   **Unimplemented:** Read as '0'

bit 8   **CEID:** Count Error Interrupt Disable bit
1 = Interrupts due to position count errors are disabled
0 = Interrupts due to position count errors are enabled

bit 7   **QEOUT:** QEA/QEB Digital Filter Output Enable bit
1 = Digital filter outputs are enabled
0 = Digital filter outputs are disabled (normal pin operation)

bit 6-4   **QECK<2:0>:** QEA/QEB Digital Filter Clock Divide Select bits
111 = 1:256 clock divide
110 = 1:128 clock divide
101 = 1:64 clock divide
100 = 1:32 clock divide
011 = 1:16 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 3   **INDOUT:** Index Channel Digital Filter Output Enable bit
1 = Digital filter output is enabled
0 = Digital filter output is disabled (normal pin operation)

bit 2-0   **INDCK<2:0>:** Index Channel Digital Filter Clock Divide Select bits
111 = 1:256 clock divide
110 = 1:128 clock divide
101 = 1:64 clock divide
100 = 1:32 clock divide
011 = 1:16 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

Note: The available control bits in the DFLTCON register may vary depending on the dsPIC30F device that is used. For more information see Register 16-2 and Register 16-3.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

Register 16-3: DFLTCON: Digital Filter Control Register (All dsPIC30F devices except dsPIC30F6010)

Upper Byte:

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IMV<1:0>		CEID
bit 15							bit 8

Lower Byte:

R/W-0	R/W-0	U-0	U-0	U-0	U-0
QEOUT	QECK<2:0>	—	—	—	—
bit 7					bit 0

bit 15-11   **Unimplemented:** Read as '0'

bit 10-9   **IMV<1:0>:** Index Match Value bits

These bits allow the user to specify the state of the QEA and QEB input pins during an Index pulse when the POSCNT register is to be reset.

In x4 Quadrature Count Mode:
IMV1 = Required State of Phase B input signal for match on index pulse
IMV0 = Required State of Phase A input signal for match on index pulse

In x2 Quadrature Count Mode:
IMV1 = Selects Phase input signal for Index state match (0 = Phase A, 1 = Phase B)
IMV0 = Required State of the selected Phase input signal for match on index pulse

bit 8   **CEID:** Count Error Interrupt Disable bit
1 = Interrupts due to count errors are disabled
0 = Interrupts due to count errors are enabled

bit 7   **QEOUT:** QEA/QEB/INDX Pin Digital Filter Output Enable bit
1 = Digital filter outputs are enabled
0 = Digital filter outputs are disabled (normal pin operation)

bit 6-4   **QECK<2:0>:** QEA/QEB/INDX Digital Filter Clock Divide Select bits
111 = 1:256 clock divide
110 = 1:128 clock divide
101 = 1:64 clock divide
100 = 1:32 clock divide
011 = 1:16 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 3-0   **Unimplemented:** Read as '0'

Note: The available control bits in the DFLTCON register may vary depending on the dsPIC30F device that is used. For more information see Register 16-2 and Register 16-3.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown
y = Value set from configuration bits on POR or BOR		

16.3 Programmable Digital Noise Filters

The QEI module uses digital noise filters to reject noise on the incoming index pulse and quadrature phase signals. Schmitt Trigger inputs and a three-clock cycle delay filter combine to reject low-level noise and large, short duration noise spikes that typically occur in noise-prone applications such as motor system applications.

The filter ensures that the filtered output signals are not permitted to change until a stable value is registered for three consecutive filter cycles.

The rate of the filter clocks determines the low passband of the filter. A slower filter clock results in a passband rejecting lower frequencies than a faster filter clock. The filter clock is the device F_{CY} clock divided by a programmable divisor.

Setting the QEOUT bit (DFLTCON<7>) enables the filter for channels QEA and QEB. The QECK<2:0> bits (DFLTCON<6:4>), specify the filter clock divisor used for channels QEA and QEB. Setting the INDOUT bit (DFLTCON<3>) enables the filter for the index channel. The INDCK<2:0> bits (DFLTCON<2:0>) specify the filter clock divisor used for the index channel. At reset, the filters for all channels are disabled.

Some devices do not have separate control bits for the QEx input digital filters and the INDX input digital filter. For these devices, the QEOUT and QECK<2:0> control bits set the digital filter characteristics for both the QEA/QEB and INDX pins. For more information see Register 16-2 and Register 16-3.

Figure 16-4 illustrates a simplified block diagram of the digital noise filter.

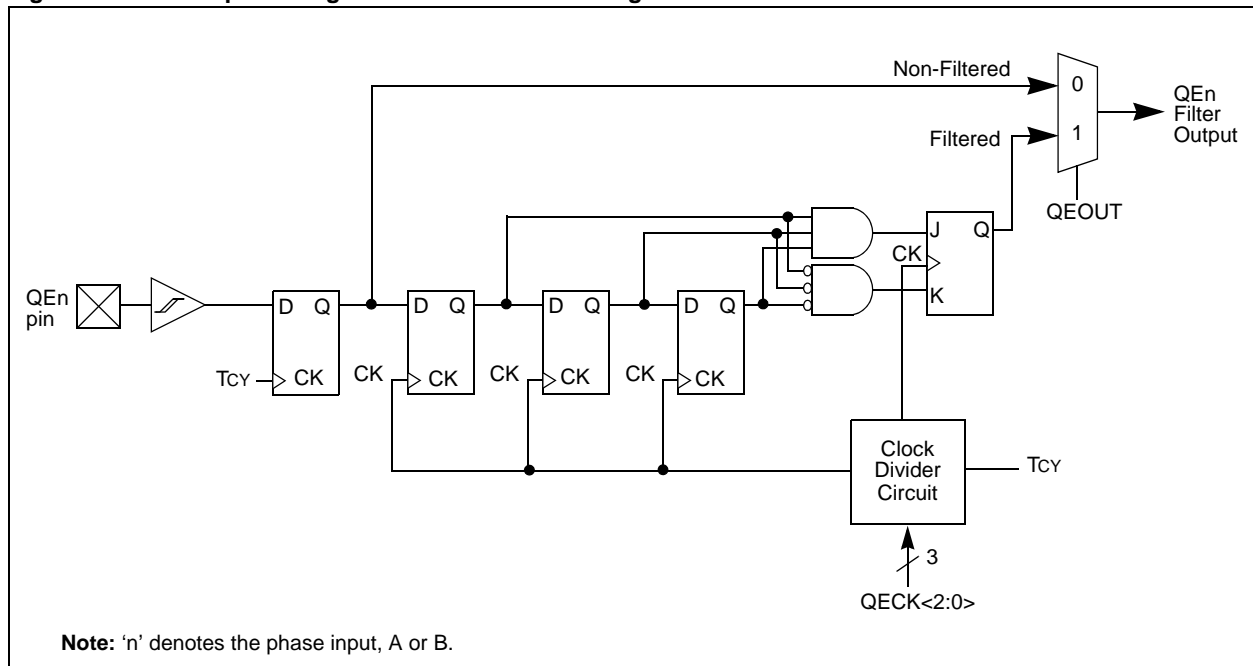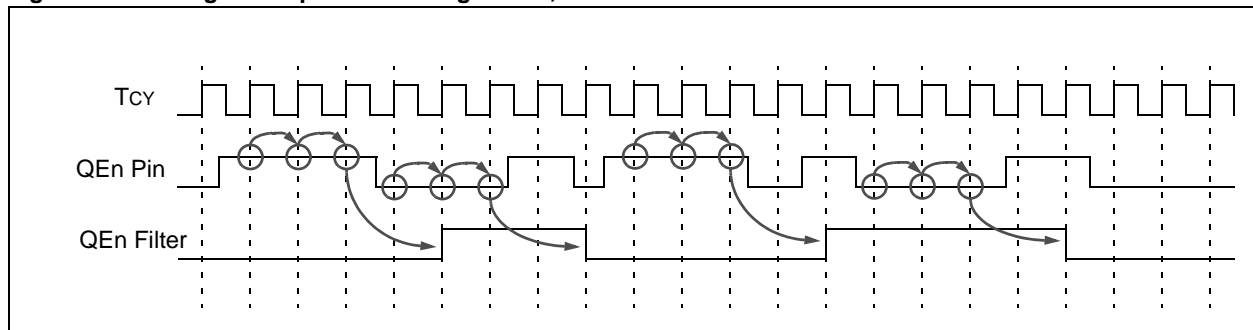**Figure 16-4:   Simplified Digital Noise Filter Block Diagram**

Note: 'n' denotes the phase input, A or B.

Figure 16-5:   Signal Proportion Through Filter, 1:1 Filter Clock Divide

16.4   Quadrature Decoder

When QEIM<2:0> = `1xx`, the Position measurement modes are selected.

When QEIM<2:0> = `x1x`, the x4 measurement mode is selected, and the QEI logic clocks the position counter on both edges of the Phase A and Phase B input signals. The x4 measurement mode provides finer resolution data (more position counts) to determine the encoder position.

Figure 16-6:   Quadrature Decoder Signals in x4 Mode
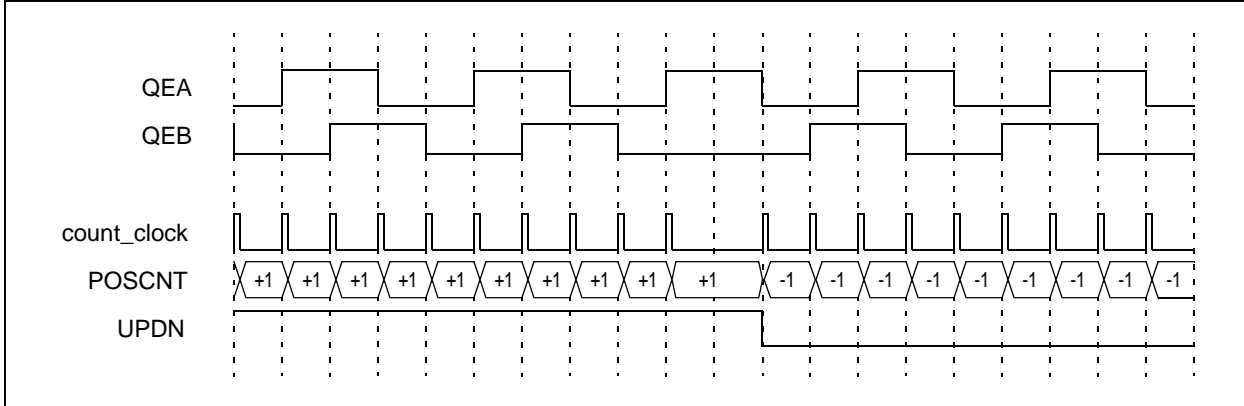
When QEIM<2:0> = `10x`, the x2 measurement mode is selected and the QEI logic looks only at the rising and falling edge of the Phase A input for the position counter increment rate. Every rising and falling edge of the Phase A signal causes the position counter to increment or decrement. The Phase B signal is utilized for the determination of the counter direction like the x4 measurement mode.

Figure 16-7:   Quadrature Decoder Signals in x2 Mode
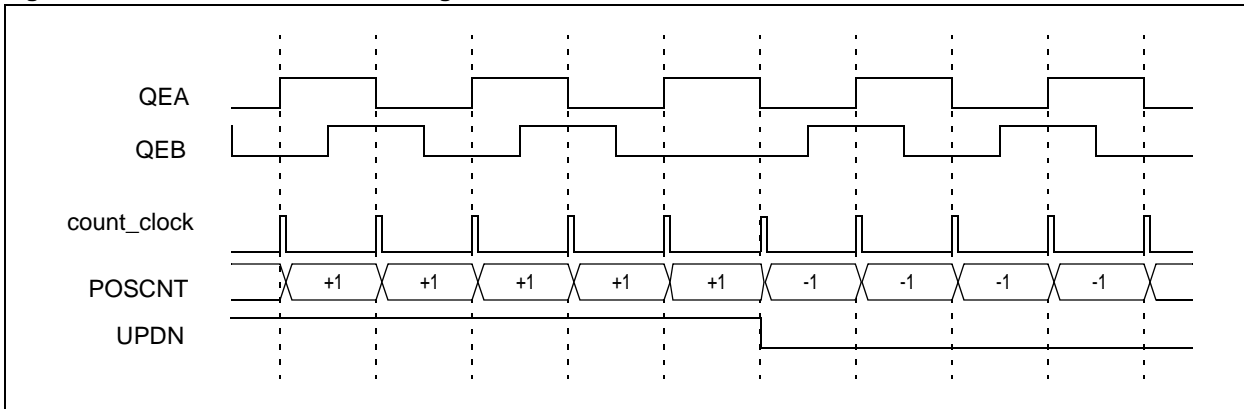
16.4.1 Explanation of Lead/Lag Test

The lead/lag test is performed by the quadrature decoder logic to determine the phase relationship of the QEA and QEB signals, and whether to increment or decrement the POSCNT register. Table 16-1 provides the lead/lag test details.

Table 16-1:   Lead/Lag Test Description

Present Transition	Previous Transition	Condition	Action	
QEA↑	QEB↓	QEA leads QEB channel	Set UPDN	Increment POSCNT
	QEB↑	QEA lags QEB channel	Clear UPDN	Decrement POSCNT
	QEA↓	Direction Change	Toggle UPDN	Increment or Decrement POSCNT
QEA↓	QEB↓	QEA lags QEB channel	Clear UPDN	Decrement POSCNT
	QEB↑	QEA leads QEB channel	Set UPDN	Increment POSCNT
	QEA↑	Direction Change	Toggle UPDN	Increment or Decrement POSCNT
QEB↑	QEA↓	QEA lags QEB channel	Clear UPDN	Decrement POSCNT
	QEA↑	QEA leads QEB channel	Set UPDN	Increment POSCNT
	QEB↓	Direction Change	Toggle UPDN	Increment or Decrement POSCNT
QEB↓	QEA↓	QEA leads QEB channel	Set UPDN	Increment POSCNT
	QEA↑	QEA lags QEB channel	Clear UPDN	Decrement POSCNT
	QEB↑	Direction Change	Toggle UPDN	Increment or Decrement POSCNT

16.4.2 Count Direction Status

As specified earlier, the QEI logic generates an UPDN signal based on the Phase A and Phase B time relationship. An I/O pin can be used to output the UPDN signal. Setting the PCDOUT bit (QEICON<6>) and clearing the appropriate TRIS bit associated with the pin, will cause the UPDN signal to drive the output pin. In addition to the output pin, the state of this internal UPDN signal is supplied to a SFR bit (QEICON<11>) as a read-only bit, UPDN.

16.4.3 Encoder Count Direction

The direction of quadrature counting is determined by the SWPAB bit (QEICON<7>). If the SWPAB = 0, the Phase A input is fed to the A input of the quadrature counter and the Phase B input is fed to the B input of the quadrature counter. Therefore, as the Phase A signal leads the Phase B signal, the quadrature counter is incremented on each edge. This condition (A signal leads the B signal) is defined as the forward direction of motion.

Setting the SWPAB bit (QEICON<7>) to a logic '1' causes the Phase A input to be fed to the B input of the quadrature counter, and the Phase B signal to be fed to the A input of the quadrature counter. Therefore, if the Phase A signal leads the Phase B signal at the dsPIC30F device pins, the Phase A input to the quadrature counter will lag the Phase B input. This condition is recognized as rotation in the reverse direction, and the counter is decremented on each quadrature pulse.

16.4.4 Quadrature Rate

The revolutions per minute (RPM) of the position control system will vary. The RPM along with the quadrature encoder line count determines the frequency of the QEA and QEB input signals. The quadrature encoder signals can be decoded such that a count pulse is generated for every quadrature signal edge. This allows an angular position measurement resolution of up to four times the encoder line count.

For example, a 6,000 RPM motor utilizing a 4096 line encoder yields a quadrature count rate of: [(6000/60) * (4096 * 4)] = 1.6384 MHz.

Similarly, a 10,000 RPM motor utilizing a 8,192 line encoder yields a quadrature count rate of: [(10000/60) * (8192 * 4)] = 5.46 MHz.

The QEI module allows a quadrature frequency of up to $F_{CY}/3$. For example, if F_{CY} = 30 MHz, the QEA and QEB signals may have a maximum frequency of 10 MHz. For more information, refer to the **"Electrical Characteristics"** section in the specific device data sheet.

16.5   16-Bit Up/Down Position Counter

The 16-bit Up/Down Counter counts up or down on every count pulse generated by the quadrature decoder logic. The counter acts as an integrator and its count value is proportional to the position. The direction of the count is determined by the quadrature decoder.

The user software may examine the contents of the count by reading the POSCNT register. The user software may also write to the POSCNT register to initialize a count.

Changing the QEIM<2:0> bits do not affect the position counter register contents.

16.5.1   Using the Position Counter (PC)

The system may utilize position counter data in one of several methods. In some systems, the position count is accumulated consistently and taken as an absolute value representing the total position of the system.

For example, assume that a quadrature encoder is affixed to a motor that is controlling the print head in a printer. In operation, the system is initialized by moving the print head to the maximum left position and resetting the POSCNT register. As the print head moves to the right, the quadrature encoder will begin to accumulate counts in the POSCNT register. As the print head moves to the left, the accumulated count will decrease. As the print head reaches the right most position, the maximum position count should be reached. If the maximum count is less than 2^{16}, the QEI module can encode the entire range of motion.

If, however, the maximum count is more than 2^{16}, the additional count precision must be captured by the user software. Generally, to accomplish this, the module is set into a mode where it resets the counter at match of a maximum count. QEIM<2:0> = 1x1 enables modes where the MAXCNT register is used to reset the position counter. When the counter reaches a pre-determined maximum count while incrementing or reaches zero while decrementing, the count is reset and an interrupt is generated to allow the user software to increment or decrement a software counter containing the Most Significant bits (MSbs) of the position count. The maximum count can be 0xFFFF to enable a full range of the QEI counter and software counter or some smaller value of significance like the number of counts for one encoder revolution.

In other systems, the position count may be cyclic. The position count is used only to reference the position of the wheel within number of rotations determined by the index pulse. For example, a tool platform moved by a screw rod uses a quadrature encoder attached to the screw rod. In operation, the screw may require five and a half rotations to achieve the desired position. The user software detects five index pulses to count the full rotations and use the position count to measure the remaining half rotation. In this method, the index pulse resets the position counter to initialize the counter at each rotation and generates an interrupt for each rotation. QEIM<2:0> = 1x0 enables these modes.

16.5.2   Using MAXCNT to Reset the Position Counter

When the QEIM<2:0> bit is '1x1', the position counter will reset on a match of the position count with predetermined high values and low values. The index pulse reset mechanism is not utilized.
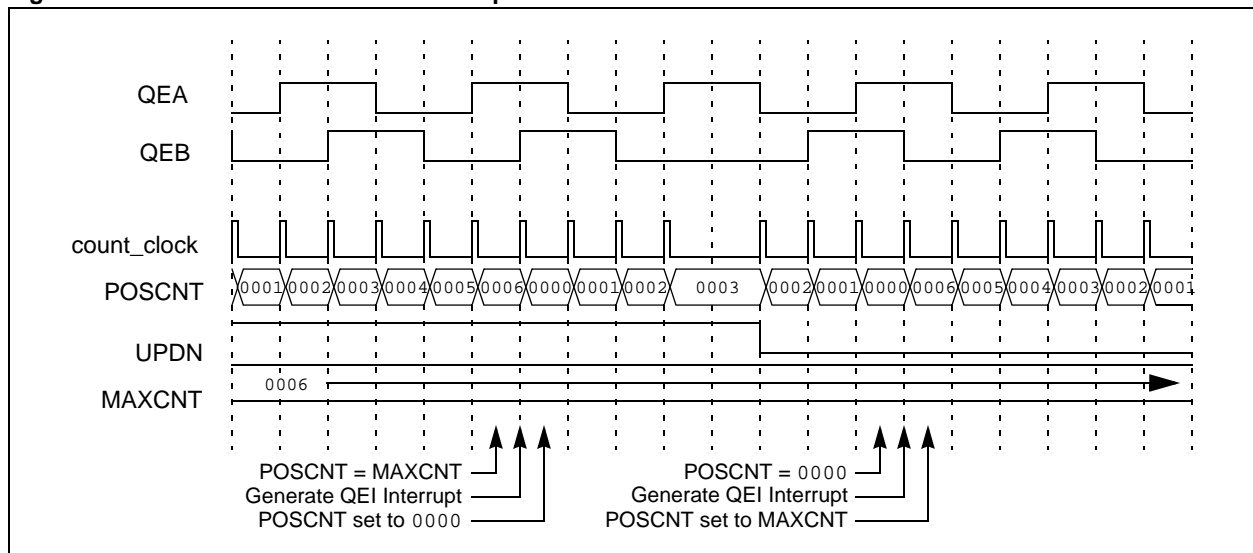
For this mode, the position counter reset mechanism operates as follows (see Figure 16-8 for related timing details):

- If the encoder is travelling in the forward direction for example, QEA leads QEB, and the value in the POSCNT register matches the value in the MAXCNT register, POSCNT will reset to zero on the next occurring quadrature pulse edge that increments POSCNT. An interrupt event is generated on this rollover event.
- If the encoder is travelling in the reverse direction for example, QEB leads QEA, and the value in the POSCNT register counts down to '0', the POSCNT is loaded with the value in the MAXCNT register on the next occurring quadrature pulse edge that decrements POSCNT. An interrupt event is generated on this underflow event.

When using MAXCNT as a position limit, the position counter will count at either x2 or x4 of the encoder counts. For standard rotary encoders, the appropriate value to write to MAXCNT would be 4N – 1 for x4 position mode and 2N – 1 for x2 position mode, where N is the number of counts per revolution of the encoder.

For absolute position information, where the range of the system exceeds 2^{16}, it is also appropriate to load a value of 0xFFFF into the MAXCNT register. The module generates an interrupt on rollover or underflow of the position counter.

**Figure 16-8:   Rollover/Rollunder Reset-Up/Down Position Counter**

16.5.3   Using Index to Reset Position Counter

When QEIM<2:0> = 1x0, the index pulse is utilized for resetting the position counter. For this mode, the position counter reset mechanism operates as follows (see Figure 16-9 for related timing details):

- The position count is reset each time an index pulse is received on the INDX pin.
- If the encoder is travelling in the forward direction (i.e., QEA leads QEB), POSCNT is reset to '0'.
- If the encoder is travelling in the reverse direction (i.e., QEB leads QEA), the value in the MAXCNT register is loaded into POSCNT.

Figure 16-9:   Reset by Index Mode-Up/Down Position Counter
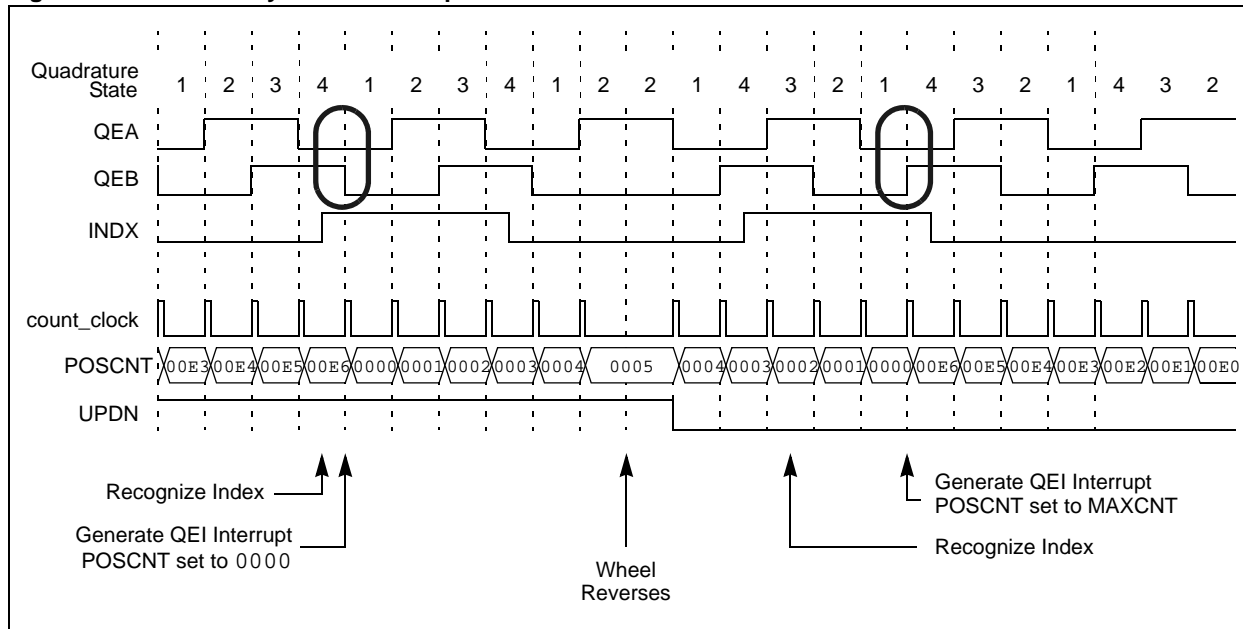
16.5.3.1   Index Pulse Detection Criteria

Incremental encoders from different manufacturers use differing timing for the index pulse. The index pulse may be aligned to any of the four quadrature states and may have a pulse width of either a full cycle (four quadrature states), a half cycle (two quadrature states) or a quarter cycle (one quadrature state). Index pulses of a full cycle width or a half cycle width are normally termed "ungated" and index pulses of a quarter cycle width are normally termed "gated".

Regardless of the type of index pulse provided, the QEI module maintains symmetry of the count as the wheel reverses direction. This means the index pulse must reset the position counter at the same relative quadrature state transition as the wheel rotates in the forward or reverse direction.

For example, in Figure 16-9, the first index pulse is recognized and resets POSCNT as the quadrature state changes from 4 to1 as highlighted in the diagram. The QEI module latches the state of this transition. Any subsequent index pulse detection will use that state transition for the reset.

As the wheel reverses, the index pulse again occurs; however, the reset of the position counter cannot occur until the quadrature state changes from 1 to 4 as highlighted in the diagram.

Note:	The QEI index logic ensures that the POSCNT register is always adjusted at the same position relative to the index pulse, regardless of the direction of travel.

16.5.3.2 IMV Control Bits

The IMV<2:0> control bits are available on some dsPIC30F devices that have the QEI module (see Register 16-3). These control bits allow the user to select the state of the QEA and QEB signals for which an index pulse reset will occur.

Devices that do not have these control bits will select the QEA and QEB states automatically during the first occurrence of an index pulse.

16.5.3.3 Index Pulse Status

The INDEX bit (QEICON<12>) provides status of the logic state on the index pin. This status bit is useful in position control systems during the "homing" sequence, where the system searches for a reference position. The INDEX bit indicates the status of the index pin after being processed by the digital filter, if it is enabled.

16.5.3.4 Using the Index Pin and MAXCNT for Error Checking

When the counter operates in Reset mode on Index Pulse mode, the QEI module will also detect POSCNT register boundary conditions. This operation can detect system errors in the incremental encoder system.

For example, assume a wheel encoder has 100 lines. When utilized in x4 measurement mode and reset on the index pulse, the counter should count from 0 to 399 (0x018E) and reset. If the POSCNT register achieves the values of 0xFFFF or 0x0190, a system error occurs.

The content of the POSCNT register is compared with MAXCNT + 1, if counting up, and with 0xFFFF, if counting down. If the QEI module detects one of these values, a position count error condition is generated by setting the CNTERR bit (QEICON<15>) and optionally generating a QEI interrupt.

If the Counter Error Interrupt Disable (CEID) Control bit (DFLTCON<8>) is cleared (by default), a QEI interrupt will be generated when a position count error is detected. If the CEID control bit is set, an interrupt does not occur.

The position counter continues to count encoder edges after detecting a position count error. No interrupt is generated for subsequent position count error events until CNTERR is cleared by the user application.

16.5.3.5 Position Counter Reset Enable (POSRES)

The Position Counter Reset Enable (POSRES) bit (QEICON<2>) enables reset of the position counter when the index pulse is detected. This bit applies only when the QEI module is configured for modes, QEIM<2:0> = 100 or 110.

If the POSRES bit is set to a logic '1', the position counter is reset when the index pulse is detected as described in this section.

If the POSRES bit is set to a logic '0', the position counter is not reset when the index pulse is detected. The position counter will continue counting up or down and be reset on the rollover or underflow condition. The QEI module continues to generate interrupts on the detection of the index pulse.

16.6   Using QEI as an Alternate 16-Bit Timer/Counter

When the QEI module is configured with QEIM<2:0> = 001, the QEI function is disabled and the QEI module is configured as a 16-bit timer/counter. Figure 16-10 illustrates the setup and control for the auxiliary timer, which is accomplished through the QEICON register.

> **Note:** The digital filter is not active when the QEI module is configured as a general-purpose counter.

The QEI timer functions similar to the other dsPIC30F timers. For more information on timers, refer to **Section 12. "Timers"** (DS70059) in the *"dsPIC30F Family Reference Manual"* (DS70046E).

When configured as a timer, the POSCNT register serves as a timer register similar to the TMRn registers of the General Purpose (GP) timers. The MAXCNT register serves as a period register similar to the PRn registers of the GP timers. When a timer/period register match occurs, the QEIF flag asserts.

> **Note:** Changing operational modes, for example, from QEI to Timer or Timer to QEI does not affect the Timer/Position Count Register contents.

Figure 16-10:   QEI as Timer/Counter Block Diagram
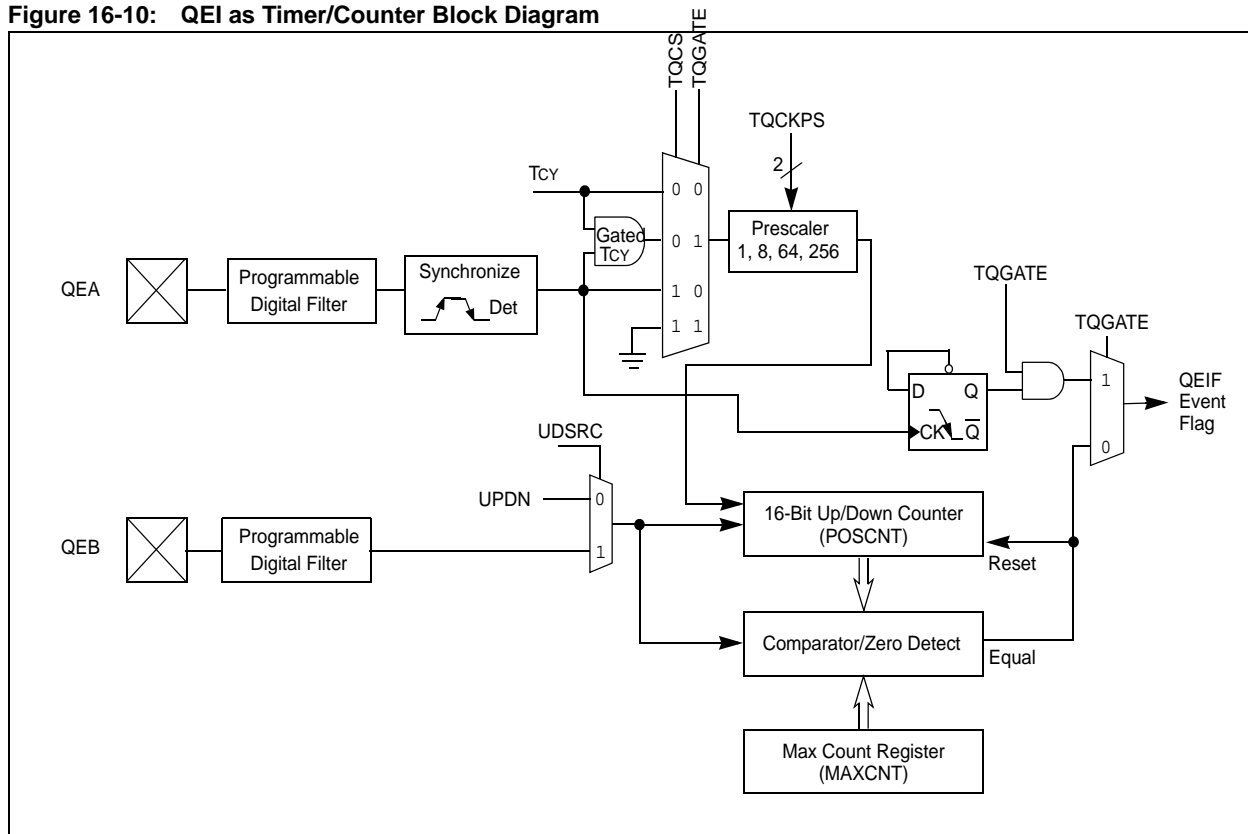
16.6.1 Up/Down Timer Operation

The QEI timer can increment or decrement. This is a unique feature over most other timers.

When the timer is configured to count up, the timer (POSCNT) will increment until the count matches the period register (MAXCNT). The timer resets to zero and restarts incrementing.

When the timer is configured to count down, the timer (POSCNT) will decrement until the count matches the period register (MAXCNT). The timer resets to zero and restarts decrementing. When the timer is configured to count down, the following general operation guidelines must be followed for correct operation:

- The MAXCNT register will serve as the period match register; however, since the counter is decrementing, the desired match value is two count. For example, to count 0x1000 clocks, the period register must be loaded with 0xF000.
- On a match condition, the timer resets to zero.

Either an I/O pin or a SFR control bit specify the count direction control. Control bit UDSRC (QEICON<0>) determines what controls the timer count direction state.

When UDSRC = 1, the timer count direction is controlled from the QEB pin. If the QEB pin is '1', the count direction will be incrementing. If the QEB pin is '0', the count direction will be decrementing.

When UDSRC = 0, the timer count direction is controlled from the UPDN bit (QEICON<11>). When UPDN = 1, the timer increments. When UPDN = 0, the timer decrements.

16.6.2 Timer External Clock

The TQCS bit (QEICON<1>) selects the internal clock or external clock. The QEI timer can use the QEA pin as an external clock input when TQCS is set. The QEI timer does not support the External Asynchronous Counter mode. If an external clock source is used, the clock is automatically synchronized to the internal instruction cycle (TCY).

16.6.3 Timer Gate Operation

The QEA pin functions as a timer gate when the TQGATE bit (QEICON<5>) is set and the TQCS is cleared.

In the event, the TQCS and TQGATE are concurrently set, the timer does not increment and generates an interrupt.

16.7 Quadrature Encoder Interface Interrupts

Depending on the operating mode of the QEI module, it generates interrupts for the following events:

- When operating in Reset On Match mode, QEIM<2:0> = 111 and 101, an interrupt occurs on position counter rollover/underflow.
- When operating in Reset On Index mode, QEIM<2:0> = 110 and 100, an interrupt occurs on detection of index pulse and optionally when CNTERR bit is set.
  - When operating as a Timer/Counter, QEIM<2:0> = 001, an interrupt occurs on a period match event or a timer gate falling edge event when TQGATE = 1.

When a QEI interrupt event occurs, the QEIIF bit (IFS2<8>) is set and an interrupt is generated if enabled. The QEIIF bit must be cleared in the software.

Enabling the QEI interrupt is accomplished through the respective enable bit, QEIIE (IEC2<8>).

16.8 I/O Pin Control

Enabling the QEI module causes the associated I/O pins to come under the control of the QEI module and prevents lower priority I/O functions such as ports from affecting the I/O pin.

Depending on the mode specified by QEIM<2:0> and other control bits, the I/O pins may assume differing functions, as shown in Table 16-2 and Table 16-3.

Table 16-2: Quadrature Encoder Module Pinout I/O Descriptions

Pin Name	Pin Type	Buffer Type	Description
QEA	I I I	ST ST ST	Quadrature Encoder Phase A Input, or Auxiliary Timer External Clock Input, or Auxiliary Timer External Gate Input
QEB	I I	ST ST	Quadrature Encoder Phase B Input, or Auxiliary Timer Up/Down Select Input
INDX	I	ST	Quadrature Encoder Index Pulse Input
UPDN	O	—	Position Up/Down Counter Direction Status, QEI mode

Legend: I = Input, O = Output, ST = Schmitt Trigger

Table 16-3: Module I/O Mode Functions

QEIM<2:0>	PCDOUT	UDSRC	TQGATE	TQCS	QEA Pin	QEB Pin	INDX Pin	UPDN Pin
000, 010, 011 Module Off	N/A	N/A	N/A	N/A	—	—	—	—
001 Timer Mode	N/A	0	0	0	—	—	—	—
		1	0	0	—	Input (UPDN)	—	—
		0	1	0	Input (TQGATE) Port not disabled	—	—	—
		1	1	0	Input (TQGATE) Port not disabled	Input (UPDN)	—	—
		0	N/A	1	Input (TQCKI) Port not disabled	—	—	—
		1	N/A	1	Input (TQCKI) Port not disabled	Input (UPDN)	—	—
101, 111 QEI Reset by count	0	N/A	N/A	N/A	Input (QEA)	Input (QEB)	—	—
	1	N/A	N/A	N/A	Input (QEA)	Input (QEB)	—	Output (UPDN)
100, 110 QEI Reset by Index	0	N/A	N/A	N/A	Input (QEA)	Input (QEB)	Input (INDX)	—
	1	N/A	N/A	N/A	Input (QEA)	Input (QEB)	Input (INDX)	Output (UPDN)

Legend: A '—' indicates that the pin is not used by the QEI module in this configuration. Instead, the pin is controlled by I/O port logic.

16.9 QEI Operation During Power-Saving Modes

16.9.1 When the Device Enters Sleep Mode

When the device enters Sleep mode, the QEI module stops all operations. POSCNT will stop at the current value. The QEI module will not respond to active signals on the QEA, QEB, INDX or UPDN pins. The QEICON register remains unchanged.

If the QEI module is configured as a timer/counter, QEIM<2:0> = 001, and the clock is provided externally, TQCS = 1, the module will also cease operation during Sleep mode.

When the QEI module wakes up, the quadrature decoder will accept the next transition on the QEA or QEB signals, and compare that transition to the last transition before Sleep mode to determine the next action.

16.9.2 When the Device Enters Idle Mode

The QEI module can enter a power-saving state in Idle mode depending on the QEISIDL bit (QEICON<13>).

If QEICSIDL = 1, then the QEI module enters the Power-Saving mode, similar to the actions while entering Sleep mode.

If QEICSIDL = 0, then the QEI module enters a Power-Saving mode. The QEI module continues to operate normally while the device is in Idle mode.

16.10 Effects of a Reset

A Reset forces the module registers to their initial Reset state. See Register 16-1 for all initialization and reset conditions for QEI module related registers. The quadrature decoder and the POSCNT counter are reset to an initial state.

16.11   Register Map

Table 16-4 maps the bit function for the special function registers (SFRs) associated with the QEI module.

Table 16-4:   **Special Function Registers Associated with QEI**

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QEICON	CNTERR	—	QEISIDL	INDEX	UPDN	QEIM<2:0>			SWPAB	PCDOUT	TQGATE	TQCKPS1	TQCKPS0	POSRES	TQCS	UDSRC	0000 0000 0000 0000
DFLTCON[1]	—	—	—	—	—	—	—	CEID	QEOUT	QECK2	QECK1	QECK0	INDOUT	INDCK2	INDCK1	INDCK0	---- ---- ---- ----
POSCNT	Position Count Register																0000 0000 0000 0000
MAXCNT	Maximum Count Register																1111 1111 1111 1111
ADPCFG[2]	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000 0000 0000
INTCON1	NSTDIS	—	—	—	—	OVATE	OVBTE	COVTE	—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000 0000 0000 0000
INTCON2	ALTIVT	—	—	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000 0000 0000 0000
IFS2	—	—	—	FLTBIF	FLTAIF	LVDIF	DCIIF	QEIIF	PWMIF	C2IF	INT4IF	INT3IF	OC8IF	OC7IF	OC6IF	OC5IF	0000 0000 0000 0000
IEC2	—	—	—	FLTBIE	FLTAIE	LVDIE	DCIIE	QEIIE	PWMIE	C2IE	INT4IE	INT3IE	OC8IE	OC7IE	OC6IE	OC5IE	0000 0000 0000 0000
IPC10	—	FLTAIP<2:0>			—	LVDIP<2:0>			—	DCIIP<2:0>			—	QEIIP<2:0>			0100 0100 0100 0100

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1:   The available control bits in the DFLTCON register may vary depending on the dsPIC30F device that is used. For more information see Register 16-2 and Register 16-3.
2:   On many devices, the QEI pins are multiplexed with analog input pins. Ensure that the QEI pins are configured as digital pins using the ADPCFG control register.

16.12   Design Tips

Question 1:   **I have initialized the QEI module, but the POSCNT Register does not seem to change when quadrature signals are applied to the QEA/QEB pins.**

Answer: On many devices, the QEI pins are multiplexed with analog input pins. You will need to ensure that the QEI pins are configured as digital pins using the ADPCFG control register.

Question 2:   **How fast may my quadrature signals be?**

Answer: The answer depends on the setting of the filter parameters for the quadrature signals. QEI requires that quadrature signals frequency must be less than $F_{CY}/3$ when no filter is used, and Filter Frequency/6 when a filter is used.

Question 3:   **My encoder has a 90° Index Pulse and the count does not reset properly.**

Answer: Depending on how the count clock is generated and which quadrature state transition is used for the index pulse, a 1/4 cycle index pulse may not be recognized before the required transition. To fix this, use a filter on the quadrature clocks which has a higher filter prescaler than that of the index pulse. This has the effect of delaying the quadrature clocks somewhat, allowing for proper detection of the index pulse.

Figure 16-11:   Reset by Index Mode (90° Index Pulse) – Up/Down Position Counter
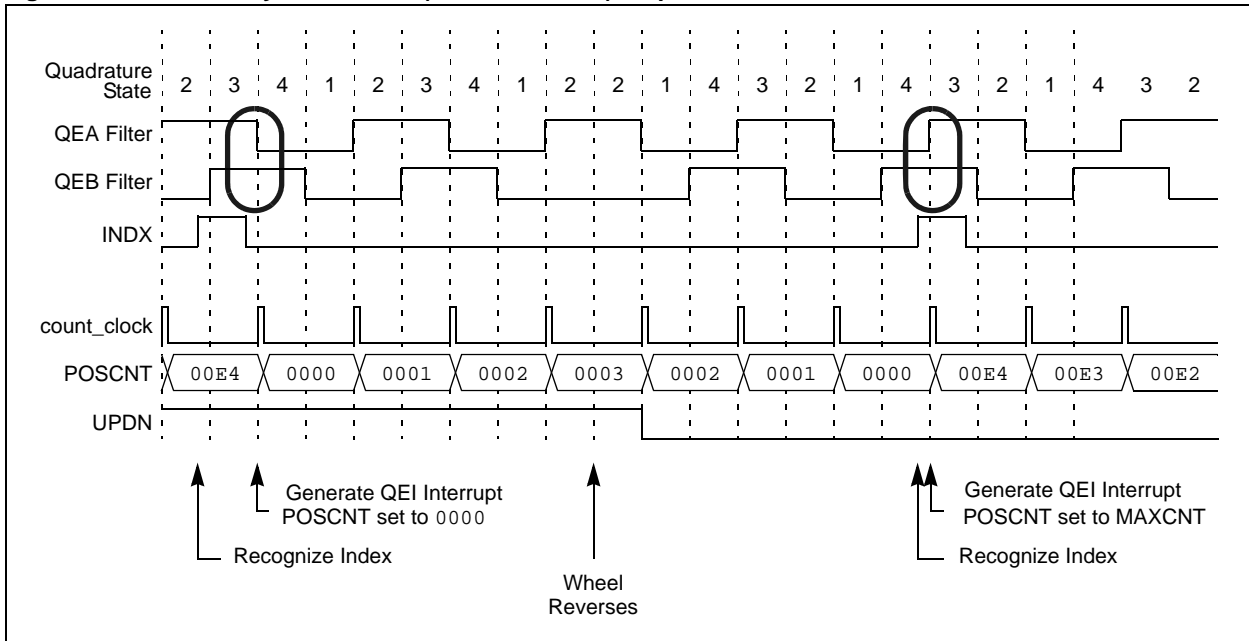
16.13   Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Quadrature Encoder Interface (QEI) module are:

Title	Application Note #
Servo Control of a DC-Brush Motor	AN532
PIC18CXXX/PIC16CXXX DC Servomotor Application	AN696
Using the dsPIC30F for Vector Control of an ACIM	AN908

> **Note:** Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F Family of devices.

16.14 Revision History

Revision A

This is the initial released revision of this document.

Revision B

This revision provides expanded information for the dsPIC30F Quadrature Encoder Interface (QEI) module.

Revision C

This revision incorporates all known errata at the time of this document update.

Revision D (January 2010)

This revision incorporates the following updates:

- Added a note on the QEI module configured as a general purpose timer/counter. See **16.6 "Using QEI as an Alternate 16-Bit Timer/Counter"** .
- Additional minor corrections such as language and formatting updates are incorporated throughout the document.

16

Quadrature Encoder Interface (QEI)

NOTES: