# Section 13. Input Capture

## HIGHLIGHTS

This section of the manual contains the following major topics:

## 13.1 Introduction

This section describes the Input Capture module and its associated Operational modes. The Input Capture module is used to capture a timer value from one of two selectable time bases, upon an event on an input pin. The Input Capture features are quite useful in applications requiring frequency (Time Period) and pulse measurement. Figure 13-1 depicts a simplified block diagram of the Input Capture module.

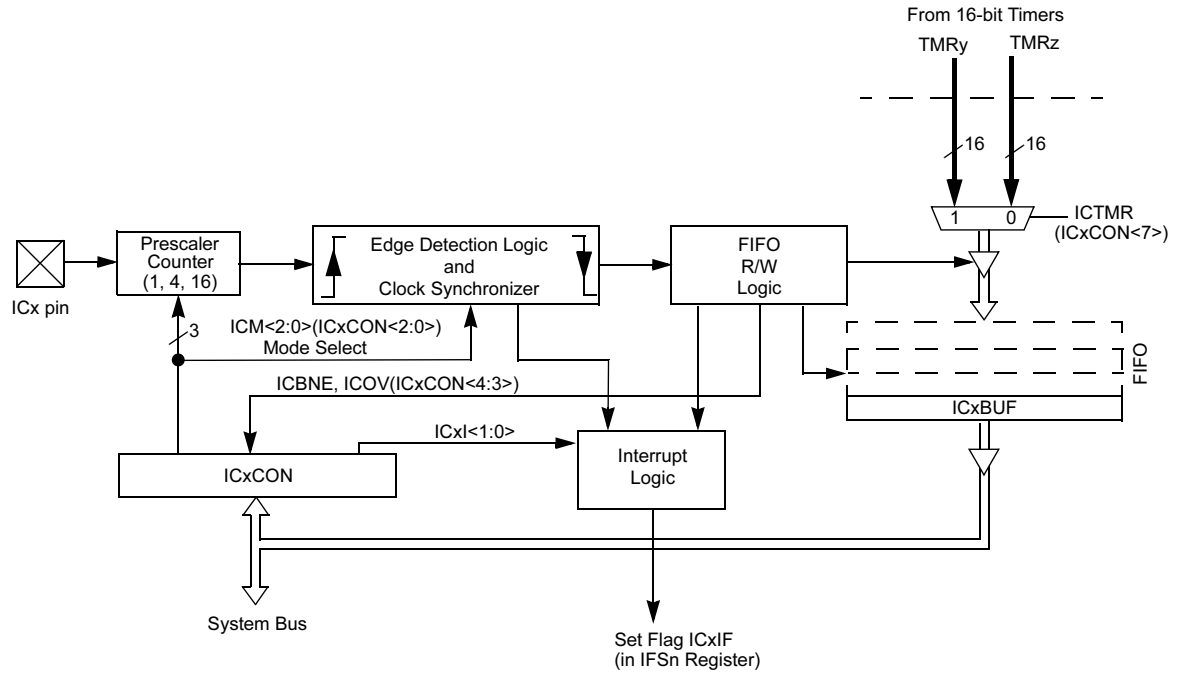
Refer to the specific device data sheet for further information on the number of channels available in a particular device. All Input Capture channels are functionally identical. In this section, an 'x' in the pin name or register name denotes the specific Input Capture channel.

The Input Capture module has multiple Operating modes, which are selected via the ICxCON register. The Operating modes include:

- Capture timer value on every falling edge of input applied at the ICx pin
- Capture timer value on every rising edge of input applied at the ICx pin
- Capture timer value on every fourth rising edge of input applied at the ICx pin
- Capture timer value on every 16th rising edge of input applied at the ICx pin
- Capture timer value on every rising and every falling edge of input applied at the ICx pin

The Input Capture module has a four-level FIFO buffer. The number of capture events required to generate a CPU interrupt can be selected by the user.

**Figure 13-1: Input Capture Block Diagram**




**Note:** An 'x' in a signal, register or bit name denotes the number of the capture channel.

### 13.2 Input Capture Registers

Each capture channel available on the dsPIC30F devices has the following registers, where 'x' denotes the number of the capture channel:

- ICxCON: Input Capture Control Register
- ICxBUF: Input Capture Buffer Register

**Register 13-1: ICxCON: Input Capture x Control Register**

| **Upper Byte:** | | | | | | | |
|---|---|---|---|---|---|---|---|
| U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | ICSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| **Lower Byte:** | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/W-0 | R/W-0 | R/W-0 | R-0, HC | R-0, HC | R/W-0 | R/W-0 | R/W-0 |
| ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | |
| bit 7 | | | | | | | bit 0 |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Module Stop in Idle Control bit
1 = Input capture module will halt in CPU Idle mode
0 = Input capture module will continue to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **ICTMR:** Input Capture Timer Select bits
1 = TMR2 contents are captured on capture event
0 = TMR3 contents are captured on capture event

**Note:** Timer selections may vary. Refer to the device data sheet for details.

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag (Read Only) bit
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Empty Status (Read Only) bit
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
111 = Input Capture functions as interrupt pin only, when device is in Sleep or Idle mode
(Rising edge detect only, all other control bits are not applicable.)
110 = Unused (module disabled)
101 = Capture mode, every 16th rising edge
100 = Capture mode, every 4th rising edge
011 = Capture mode, every rising edge
010 = Capture mode, every falling edge
001 = Capture mode, every edge (rising and falling)
(ICI<1:0> does not control interrupt generation for this mode.)
000 = Input capture module turned off

| Legend: | | | |
|---|---|---|---|
| HC = Cleared in Hardware | HS = Set in Hardware | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

### 13.3 Timer Selection

Each dsPIC30F device may have one or more input capture channels. Each channel can select between one of two 16-bit timers for the time base. Refer to the device data sheet for the specific timers that can be selected.

Selection of the timer resource is accomplished through the ICTMR control bit (ICxCON<7>). The timers can be setup using the internal clock source (FOSC/4), or using a synchronized external clock source applied at the TxCK pin.

### 13.4 Input Capture Event Modes

The input capture module captures the 16-bit value of the selected time base register when an event occurs at the ICx pin. The events that can be captured are listed below in three categories:

1. Simple Capture Event modes
   - Capture timer value on every falling edge of input at ICx pin
   - Capture timer value on every rising edge of input at ICx pin
2. Capture timer value on every edge (rising and falling)
3. Prescaler Capture Event modes
   - Capture timer value on every 4th rising edge of input at ICx pin
   - Capture timer value on every 16th rising edge of input at ICx pin

These Input Capture modes are configured by setting the appropriate Input Capture mode bits, ICM<2:0> (ICxCON<2:0>).

#### 13.4.1 Simple Capture Events

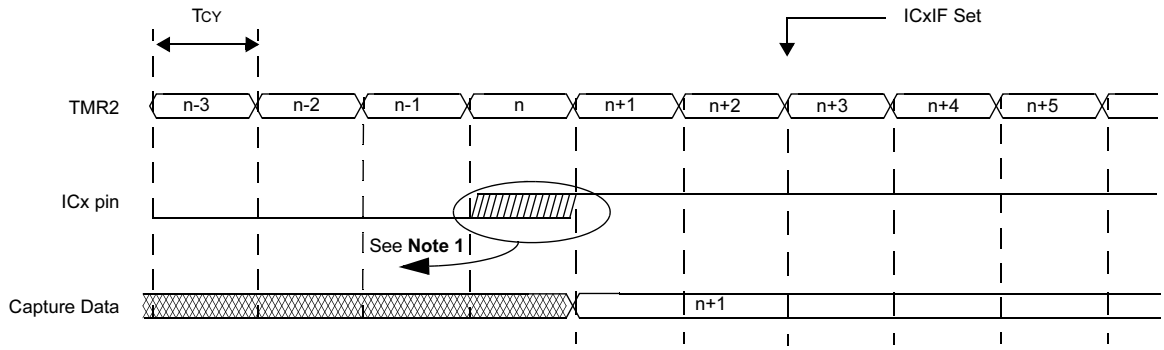
The capture module can capture a timer count value (TMR2 or TMR3) based on the selected edge (rising or falling defined by mode) of the input applied to the ICx pin. These modes are specified by setting the ICM<2:0> (ICxCON<2:0>) bits to '010' or '011', respectively. In these modes, the prescaler counter is not used. See Figure 13-3 and Figure 13-2 for simplified timing diagrams of a simple capture event.

The input capture logic detects and synchronizes the rising or falling edge of the capture pin signal on the internal phase clocks. If the rising/falling edge has occurred, the capture module logic will write the current time base value to the capture buffer and signal the interrupt generation logic. When the number of elapsed capture events matches the number specified by the ICI<1:0> control bits, the respective capture channel interrupt status flag, ICxIF, is asserted 2 instruction cycles after the capture buffer write event.

If the capture time base increments every instruction cycle, the captured count value will be the value that was present 1 or 2 instruction cycles past the time of the event on the ICx pin. This time delay is a function of the actual ICx edge event related to the instruction cycle clock and delay associated with the input capture logic. If the input clock to the capture time base is prescaled, then the delay in the captured value can be eliminated. See Figure 13-3 and Figure 13-2 for details.

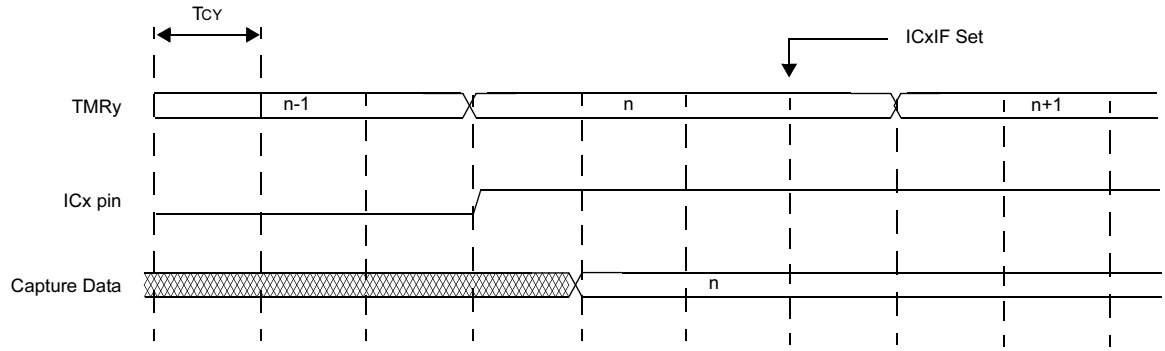
The input capture pin has minimum high time and low time specifications. Refer to the "Electrical Specifications" section of the device data sheet for further details.

**Figure 13-2: Simple Capture Event Timing Diagram, Time Base Prescaler = 1:1**




**Note 1:** A capture signal edge that occurs in this region will result in a capture buffer entry value of 1 or 2 timer counts from the capture signal edge.

**Figure 13-3: Simple Capture Event Timing Diagram, Time Base Prescaler = 1:4**



### 13.4.2 Prescaler Capture Events

The capture module has two Prescaled Capture modes. The Prescale modes are selected by setting the ICM<2:0> (ICxCON<2:0>) bits to '100' or '101', respectively. In these modes, the capture module counts four or sixteen rising edge pin events before a capture event occurs.

The capture prescaler counter is incremented on every valid rising edge applied to the capture pin. The rising edge applied to the pin effectively serves as a clock to a counter. When the prescaler counter equals four or sixteen counts (depending on the mode selected), the counter will output a "valid" capture event signal, which is then synchronized to the instruction cycle clock. This synchronized capture event signal will trigger a capture buffer write event and signal the interrupt generation logic. The respective capture channel interrupt status flag, ICxIF, is asserted 2 instruction cycles after the capture buffer write event.

If the capture time base increments every instruction cycle, the captured count value will be the value that was present 1 or 2 instruction cycles past the time of the synchronized capture event.

The input capture pin has minimum high time and low time specifications. Refer to the "Electrical Specifications" section of the device data sheet for further details.

Switching from one prescale setting to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 13-1 shows the recommended method for switching between capture prescale settings.

The prescaler counter is cleared when:

- The capture channel is turned off (i.e., ICM<2:0> = '000').
- Any device Reset.

The prescaler counter is not cleared when:

- The user switches from one active Capture mode to another.

**Example 13-1: Prescaled Capture Code Example**

```
;   The following code example will set the Input Capture 1 module
;   for interrupts on every second capture event, capture on every
;   fourth rising edge and select Timer 2 as the time-base. This
;   code example clears ICxCON to avoid unexpected interrupts.

    BSET    IPC0,   #IC1IP0     ; Setup Input Capture 1 interrupt for
    BCLR    IPC0,   #IC1IP1     ; desired priority level
    BCLR    IPC0,   #IC1IP2     ; (this example assigns level 1 priority)
    BCLR    IFS0,   #IC1IF      ; Clear the IC1 interrupt status flag
    BSET    IEC0,   #IC1IE      ; Enable IC1 interrupts

    CLR     IC1CON              ; Turn off Input Capture 1 Module.
    MOV     #0x00A2, w0         ; Load the working register with the new
    MOV     w0, IC1CON          ; prescaler mode and write to IC1CON

    MOV     #IC1BUF, w0         ; Create capture data fetch pointer
    MOV     #TEMP_BUFF, w1      ; Create data storage pointer
                                ; Assumes TEMP_BUFF is already defined

;   The following code shows how to read the capture buffer when
;   an interrupt is generated. W0 contains the capture buffer address.

;   Example code for Input Capture 1 ISR:

__IC1Interrupt:
    BCLR    IFS0,   #IC1IF      ; Reset respective interrupt flag
    MOV     [w0++], [w1++]      ; Read and save off first capture entry
    MOV     [w0],   [w1]        ; Read and save off second capture entry
                                ; Remaining user code here
    RETFIE                      ; Return from ISR
```

**Note:** It is recommended that the user turn off the capture module (i.e., clear ICM<2:0> (ICxCON<2:0>)) before switching to a new mode. If the user switches to a new Capture mode, the prescaler counter is not cleared. Therefore, it is possible that the first capture event and its associated interrupt is generated due to a non-zero prescaler counter (at the time of switching modes).

### 13.4.3 Edge Detection Mode

The capture module can capture a time base count value on every rising and falling edge of the input signal applied to the ICx pin. The Edge Detection mode is selected by setting the ICM<2:0> (ICxCON<2:0>) bits to '001'. In this mode, the capture prescaler counter is not used. See Figure 13-4 for a simplified timing diagram.

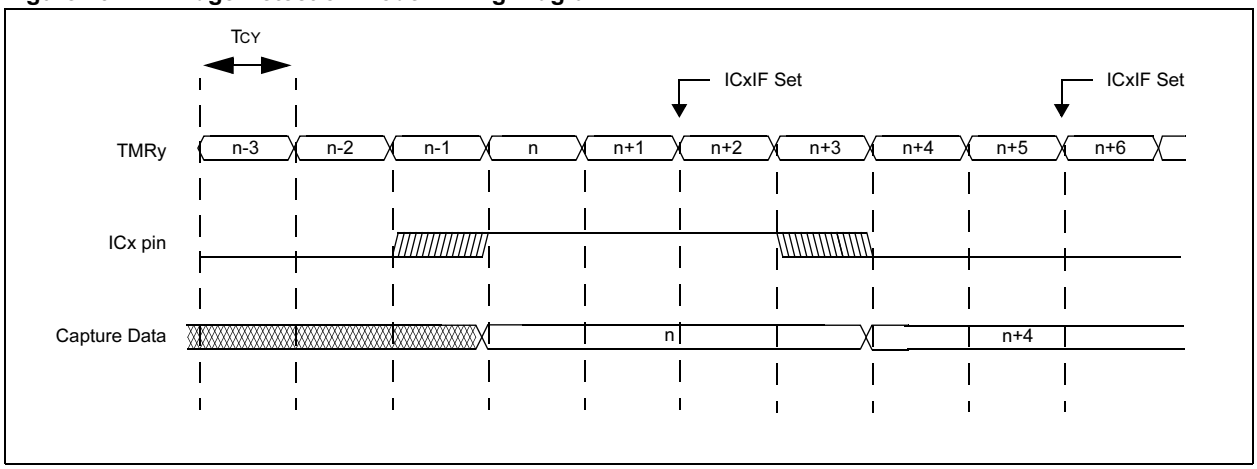
When the input capture module is configured for Edge Detection mode, the module will:

- Set the input capture interrupt flag (ICxIF) on every edge, rising and falling.
- The Interrupt-on-Capture mode bits, ICI<1:0> (ICxCON<6:5>), are not used in this mode. Every capture event will generate an interrupt.
- No capture overflow, ICOV (ICxCON<4>), bit is generated.

As with the simple Capture Event mode, the input capture logic detects and synchronizes the rising and falling edge of the capture pin signal on the internal phase clocks. If the rising or falling edge has occurred, the capture module logic will write the current timer count to the capture buffer and signal the interrupt generation logic. The respective capture channel interrupt status flag, ICxIF, is asserted 2 instruction cycles after the capture buffer write event.

The captured timer count value will be 1 or 2 TCY (instruction cycles) past the time of the occurrence of the edge at the ICx pin (see Figure 13-4).

**Figure 13-4: Edge Detection Mode Timing Diagram**




## 13.5 Capture Buffer Operation

Each capture channel has an associated four-deep FIFO buffer. The ICxBUF register is the buffer register visible to the user, as it is memory mapped.

When the input capture module is reset, ICM<2:0> = 000 (ICxCON<2:0>), the input capture logic will:

- Clear the overflow condition flag (i.e., clear ICxOV (ICxCON<4>) to '0').
- Reset the capture buffer to the empty state (i.e., clears ICBNE (ICxCON<3>) to '0').

Reading the FIFO buffer under the following conditions will lead to indeterminate results:

- In the event the input capture module is first disabled and at some later time re-enabled.
- In the event a FIFO read is performed when the buffer is empty.
- After a device Reset.

There are two status flags which provide status on the FIFO buffer:

- ICBNE (ICxCON<3>): Input Capture Buffer Not Empty
- ICOV (ICxCON<4>): Input Capture Overflow

### 13.5.1 Input Capture Buffer Not Empty (ICBNE)

The ICBNE read only Status bit (ICxCON<3>) will be set on the first input capture event and remain set until all capture events have been read from the capture buffer. For example, if three capture events have occurred, then three reads of the capture buffer are required before the ICBNE (ICxCON<3>) flag will be cleared. If four capture events, then four reads are required to clear the ICBNE (ICxCON<3>) flag. Each read of the capture buffer will allow the remaining word(s) to move to the next available top location. Since the ICBNE reflects the capture buffer state, the ICBNE Status bit will be cleared in the event of any device Reset.

### 13.5.2 Input Capture Overflow (ICOV)

The ICOV read only Status bit (ICxCON<4>) will be set when the capture buffer overflows. In the event that buffer is full with four capture events and a fifth capture event occurs prior to a read of the buffer, an overrun condition will occur, the ICOV (ICxCON<4>) bit will be set to a logic '1' and the respective capture event interrupt will not be generated. In addition, the fifth capture event is not recorded and all subsequent capture events will not alter the current buffer contents.

To clear the overrun condition, the capture buffer must be read four times. Upon the fourth read, the ICOV (ICxCON<4>) status flag will be cleared and the capture channel will resume normal operation.

Clearing of the overflow condition can be accomplished in the following ways:

- Set ICM<2:0> (ICxCON<2:0>) = 000
- Read capture buffer until ICBNE (ICxCON<3>) = 0
- Any device Reset

#### 13.5.2.1 ICOV and Interrupt Only Mode

The input capture module can also be configured to function as an external interrupt pin. For this mode, the ICI<1:0> (ICxCON<6:5>) bits must be set to '00'. Interrupts will be generated independently of buffer reads.

## 13.6 Input Capture Interrupts

The input capture module has the ability to generate an interrupt based upon a selected number of capture events. A capture event is defined as a write of a time base value into the capture buffer. This setting is configured by the control bits ICI<1:0> (ICxCON<6:5>).

Except for the case when ICI<1:0> = '00', no interrupts will be generated until a buffer overflow condition is removed (see **Section 13.5.2 "Input Capture Overflow (ICOV)"**). When the capture buffer has been emptied, either by a Reset condition or a read operation, the interrupt count is reset. This allows for the resynchronization of the interrupt count to the FIFO entry status.

### 13.6.1 Interrupt Control Bits

Each input capture channel has interrupt flag Status bits (ICxIF), interrupt enable bits (ICxIE) and interrupt priority control bits (ICxIP<2:0>). Refer to **Section 6. "Reset Interrupts"** for further information on peripheral interrupts.

## 13.7 UART Autobaud Support

The input capture module can be used by the UART module when the UART is configured for the Autobaud mode of operation, ABAUD = 1 (UxMODE<5>). When the ABAUD control bit is set, the UART RX pin will be internally connected to the assigned input capture module input. The I/O pin associated with the capture module will be disconnected. The baud rate can be determined by measuring the width of the Start bit when a NULL character is received. Note that the capture module must be configured for the Edge Detection mode (capture on every rising and falling edge) to take advantage of the autobaud feature. The input capture module assignment for each UART will depend on the dsPIC30F device variant that is selected. Refer to the device data sheet for further details on the autobaud support.

## 13.8 Input Capture Operation in Power Saving States

### 13.8.1 Input Capture Operation in Sleep Mode

When the device enters Sleep mode, the system clock is disabled. In Sleep mode, the input capture module can only function as an external interrupt source. This mode is enabled by setting control bits ICM<2:0> = '111'. In this mode, a rising edge on the capture pin will generate device wake-up from Sleep condition. If the respective module interrupt bit is enabled and the module priority is of the required priority, an interrupt will be generated.

In the event the capture module has been configured for a mode other than ICM<2:0> = '111' and the dsPIC30F does enter the Sleep mode, no external pin stimulus, rising or falling, will generate a wake-up condition from Sleep.

### 13.8.2 Input Capture Operation in Idle Mode

When the device enters Idle mode, the system clock sources remain functional and the CPU stops executing code. The ICSIDL bit (ICxCON<13>) selects if the module will stop in Idle mode, or continue to operate in Idle mode.

If ICSIDL = 0 (ICxCON<13>), the module will continue operation in Idle mode. Full functionality of the input capture module is provided for, including the 4:1 and 16:1 capture prescale settings, defined by control bits ICM<2:0> (ICxCON<2:0>). These modes require that the selected timer is enabled during Idle mode as well.

If the Input Capture mode is configured for ICM<2:0> = '111', the input capture pin will serve only as an external interrupt pin. In this mode, a rising edge on the capture pin will generate device wake-up from Idle mode. A capture time base does not have to be enabled. If the respective module interrupt enable bit is set and the user assigned priority is greater than the current CPU priority level, an interrupt will be generated.

If ICSIDL = 1 (ICxCON<13>), the module will stop in Idle mode. The module will perform the same functions when stopped in Idle mode as for Sleep mode (see **Section 13.8.1 "Input Capture Operation in Sleep Mode"**).

### 13.8.3 Device Wake-up on Sleep/Idle

An input capture event can generate a device wake-up or interrupt, if enabled, if the device is in Idle or Sleep mode.

Independent of the timer being enabled, the input capture module will wake-up from Sleep or Idle mode when a capture event occurs, if the following are true:

- Input Capture mode bits, ICM<2:0> = '111' (ICxCON<2:0>) and
- The interrupt enable bit (ICxIE) is asserted.

This same wake-up feature will interrupt the CPU if:

- The respective interrupt is enabled (ICxIE = 1) and is of the required priority.

This wake-up feature is quite useful for adding extra external pin interrupts. The following conditions are true when the input capture module is used in this mode:

- The capture prescaler counter is not utilized while in this mode.
- The ICI<1:0>(ICxCON<6:5>) bits are not applicable.

## 13.9 I/O Pin Control

When the capture module is enabled, the user must ensure the I/O pin direction is configured for an input by setting the associated TRIS bit. The pin direction is not set when the capture module is enabled. Furthermore, all other peripherals multiplexed with the input pin must be disabled.

## 13.10 Special Function Registers Associated with the Input Capture Module

**Table 13-1: Example Memory Map for Input Capture Modules**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0084 | CNIF | MI2CIF | SI2CIF | NVMIF | ADIF | U1TXIF | U1RXIF | SPI1IF | T3IF | T2IF | OC2IF | IC2IF | T1IF | OC1IF | IC1IF | INT0F | 0000 0000 0000 0000 |
| IFS1 | 0086 | IC6IF | IC5IF | IC4IF | IC3IF | C1IF | SPI2IF | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | IC8IF | IC7IF | INT1IF | 0000 0000 0000 0000 |
| IEC0 | 008C | CNIE | MI2CIE | SI2CIE | IR12 | ADIE | U1TXIE | U1RXIE | SPI1IE | T3IE | T2IE | OC2IE | IC2IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 0000 0000 0000 |
| IEC1 | 008E | IC6IE | EI30 | IC4IE | IC3IE | C1IE | SPI2IE | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | IC8IE | IC7IE | INT1IE | 0000 0000 0000 0000 |
| IPC0 | 0094 | — | T1IP<2:0> | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | | 0100 0100 0100 0100 |
| IPC1 | 0096 | — | T31P<2:0> | | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | | 0100 0100 0100 0100 |
| IPC4 | 009C | — | OC3IP<2:0> | | — | IC8IP<2:0> | | | — | IC7IP<2:0> | | | — | INT1IP<2:0> | | | | 0100 0100 0100 0100 |
| IPC7 | 00A2 | — | IC6IP<2:0> | | — | IC5IP<2:0> | | | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | | 0100 0100 0100 0100 |
| IC1BUF | 0140 | Input 1 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC1CON | 0142 | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC2BUF | 0144 | Input 2 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC2CON | 0146 | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC3BUF | 0148 | Input 3 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC3CON | 014A | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC4BUF | 014C | Input 4 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC4CON | 014E | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC5BUF | 0150 | Input 5 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC5CON | 0152 | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC6BUF | 0154 | Input 6 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC6CON | 0156 | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC7BUF | 0158 | Input 7 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC7CON | 015A | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |
| IC8BUF | 015C | Input 8 Capture Register | | | | | | | | | | | | | | | | uuuu uuuu uuuu uuuu |
| IC8CON | 015E | — | — | ICSIDL | — | — | — | — | — | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 0000 0000 0000 |

Legend: u = uninitialized

**Note:** Refer to the device data sheet for specific memory map details.

## 13.11 Design Tips

**Question 1:** ***Can the Input Capture module be used to wake the device from Sleep mode?***

**Answer:** Yes. When the Input Capture module is configured to ICM<2:0> = '111' and the respective channel interrupt enable bit is asserted, ICxIE = 1, a rising edge on the capture pin will wake-up the device from Sleep (see **Section 13.8 "Input Capture Operation in Power Saving States"**).

## 13.12 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Input Capture module are:

| Title | Application Note # |
|---|---|
| Using the CCP Module(s) | AN594 |
| Implementing Ultrasonic Ranging | AN597 |

**Note:** Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F Family of devices.

## 13.13 Revision History

### Revision A

This is the initial released revision of this document.

### Revision B

There were no technical content or editorial revisions to this section of the manual, however, this section was updated to reflect Revision B throughout the manual.

### Revision C

There were no technical content revisions to this section of the manual, however, this section was updated to reflect Revision C throughout the manual.