Section 9. Low Voltage Detect (LVD)

HIGHLIGHTS

This section of the manual contains the following topics:

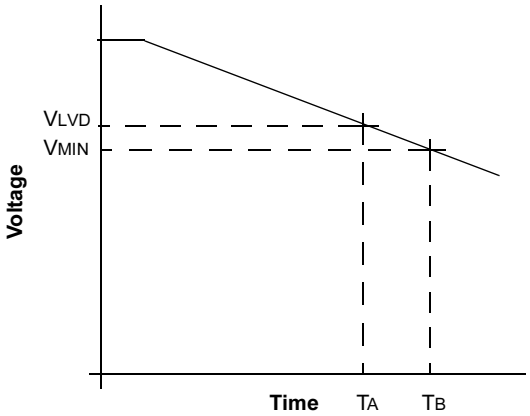
9.1 Introduction

The LVD module is applicable to battery operated applications. As the battery drains its energy, the battery voltage slowly drops. The battery source impedance also increases as it loses energy. The LVD module is used to detect when the battery voltage (and therefore, the V_{DD} of the device) drops below a threshold, which is considered near the end of battery life for the application. This allows the application to gracefully shutdown its operation.

The LVD module uses an internal reference voltage for comparison. The threshold voltage, V_{LVD}, is programmable during run-time.

Figure 9-1 shows a possible application battery voltage curve. Over time, the device voltage decreases. When the device voltage equals voltage V_{LVD}, the LVD logic generates an interrupt. This occurs at time T_A. The application software then has until the device voltage is no longer in valid operating range to shutdown the system. Voltage point V_B is the minimum valid operating voltage specification. This gives a time T_B. The total time for shutdown is $T_B - T_A$.

Figure 9-1: Typical Low Voltage Detect Application

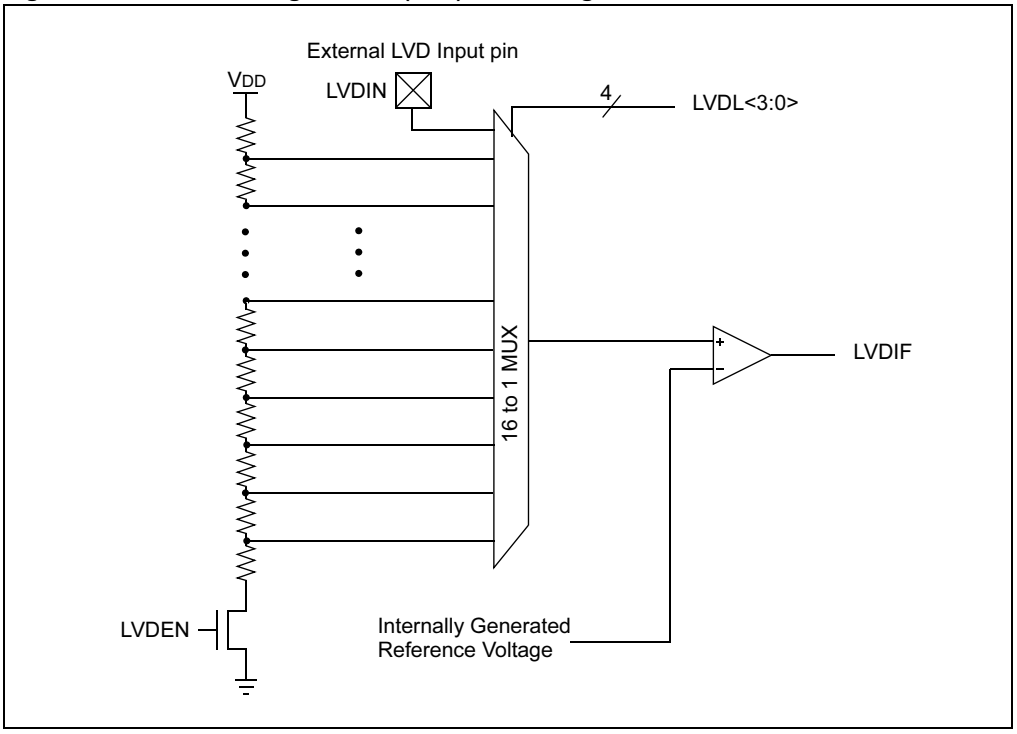


Legend:
V_{LVD} = LVD trip point
V_{MIN} = Minimum valid device operating voltage

Figure 9-2 shows the block diagram for the LVD module. A comparator uses an internally generated reference voltage as the set point. When the selected tap output of the device voltage is lower than the reference voltage, the LVDIF bit (IFS2<10>) is set.

Each node in the resistor divider represents a “trip point” voltage. This voltage is software programmable to any one of 16 values.

Figure 9-2: Low Voltage Detect (LVD) Block Diagram



9.1.1 LVD Control Bits

The LVD module control bits are located in the RCON register.

The LVDEN bit (RCON<12>) enables the Low Voltage Detect module. The LVD module is enabled when LVDEN = 1. If power consumption is important, the LVDEN bit can be cleared for maximum power savings.

9.1.1.1 LVD Trip Point Selection

The LVDL<3:0> bits (RCON<11:8>) will choose the LVD trip point. There are 15 trip point options that may be selected from the internal voltage divider connected to VDD. If none of the trip point options are suitable for the application, there is one option that allows the LVD sample voltage to be applied externally on the LVDIN pin. (Refer to the specific device data sheet for the pin location.) The nominal trip point voltage for the external LVD input is 1.24 volts. The LVD external input option requires that the user select values for an external voltage divider circuit that will generate a LVD interrupt at the desired VDD.

9.1.2 Internal Voltage Reference

The LVD uses an internal bandgap voltage reference circuit that requires a nominal amount of time to stabilize. Refer to the “Electrical Specifications” in the specific device data sheet for details. The BGST status bit (RCON<13>) indicates when the bandgap voltage reference has stabilized. The user should poll the BGST status bit in software after the LVD module is enabled. At the end of the stabilization time, the LVDIF bit (IFS2<10>) should be cleared. Refer to the LVD module setup procedure in **Section 9.2 “LVD Operation”**.

The bandgap voltage reference circuit can also be used by other peripherals on the device so it may already be active (and stabilized) prior to enabling the LVD module.

Register 9-1: RCON: Reset Control Register

Upper Byte:							
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
TRAPR	IOPUWR	**BGST**	**LVDEN**	**LVDL<3:0>**			
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

bit 13 **BGST:** Bandgap Stable bit
1 = The bandgap has stabilized
0 = Bandgap is not stable and LVD interrupts should be disabled

bit 12 **LVDEN:** Low Voltage Detect Power Enable bit
1 = Enables LVD, powers up LVD circuit
0 = Disables LVD, powers down LVD circuit

bit 11-8 **LVDL<3:0>:** Low Voltage Detection Limit bits
1111 = Input to LVD is the LVDIN pin (1.24V threshold, nominal)
1110 = 4.6V
1101 = 4.3V
1100 = 4.1V
1011 = 3.9V
1010 = 3.7V
1001 = 3.6V
1000 = 3.4V
0111 = 3.1V
0110 = 2.9V
0101 = 2.8V (default value at Reset)
0100 = 2.6V
0011 = 2.5V
0010 = 2.3V
0001 = 2.1V
0000 = 1.9V

Note: The voltage threshold values shown here are provided for design guidance only. Refer to the "Electrical Specifications" in the device data sheet for further details.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Note: See **Section 8. "Reset"** for a description of other bits in the RCON register.

9.2 LVD Operation

The LVD module adds robustness to the application because the device can monitor the state of the device voltage. When the device voltage enters a voltage window near the lower limit of the valid operating voltage range, the device can save values to ensure a “clean” shutdown.

Note:	The system design should ensure that the application software is given adequate time to save values before the device exits the valid operating range, or is forced into a Brown-out Reset.

Depending on the power source for the device, the supply voltage may decrease relatively slowly. This means that the LVD module does not need to be constantly operating. To decrease the current requirements, the LVD circuitry only needs to be enabled for short periods where the voltage is checked. After doing the check, the LVD module may be disabled.

9.2.1 LVD Initialization Steps

The following steps are required to setup the LVD module:

1. If the external LVD input pin is used (LVDIN), ensure that all other peripherals multiplexed on the pin are disabled and the pin is configured as an input by setting the appropriate bit in the TRISx registers.
2. Write the desired value to the LVDL control bits (RCON<11:8>), which selects the desired LVD threshold voltage.
3. Ensure that LVD interrupts are disabled by clearing the LVDIE bit (IEC2<10>).
4. Enable the LVD module by setting the LVDEN bit (RCON<12>).
5. Wait for the internal voltage reference to become stable by polling the BGST status bit (RCON<13>), if required (see **Section 9.1.2 “Internal Voltage Reference”**).
6. Ensure that the LVDIF bit (IFS2<10>) is cleared before interrupts are enabled. If LVDIF is set, the device VDD may be below the chosen LVD threshold voltage.
7. Set LVD interrupts to the desired CPU priority level by writing the LVDIP<2:0> control bits (IPC10<10:8>).
8. Enable LVD interrupts by setting the LVDIE control bit.

Once the VDD has fallen below the programmed LVD threshold, the LVDIF bit will remain set. When the LVD module has interrupted the CPU, one of two actions may be taken in the ISR:

1. Clear the LVDIE control bit to disable further LVD module interrupts and take the appropriate shutdown procedures.

or

2. Decrease the LVD voltage threshold using the LVDL control bits and clear the LDVIF status bit. This technique can be used to track a gradually decreasing battery voltage.

9.2.2 Current Consumption for LVD Operation

The LVD circuit relies on an internal voltage reference circuit that is shared with other peripheral devices, such as the Brown-out Reset (BOR) module. The internal voltage reference will be active whenever one of its associated peripherals is enabled. For this reason, the user may not observe the expected change in current consumption when the LVD module is disabled.

9.2.3 Operation in Sleep and Idle Mode

When enabled, the LVD circuitry continues to operate during Sleep or Idle modes. If the device voltage crosses the trip point, the LVDIF bit will be set.

The criteria for exiting from Sleep or Idle modes are as follows:

- If the LVDIE bit (IEC2<10>) is set, the device will wake from Sleep or Idle mode.
- If the assigned priority for the LVD interrupt is *less than or equal to* the current CPU priority, the device will wake-up and continue code execution from the instruction following the `PWRSAV` instruction that initiated the Sleep or Idle mode.
- If the assigned priority level for the LVD interrupt is *greater* than the current CPU priority, the device will wake-up and the CPU exception process will begin. Code execution will continue from the first instruction of the LVD ISR.

9.3 Design Tips

Question 1: ***The LVD circuitry seems to be generating random interrupts?***

Answer: Ensure that the internal voltage reference is stable before enabling the LVD interrupt. This is done by polling the BGST status bit (RCON<13>) after the LVD module is enabled. After this time delay, the LVDIF bit should be cleared and then, the LVDIE bit may be set.

Question 2: ***How can I reduce the current consumption of the module?***

Answer: Low Voltage Detect is used to monitor the device voltage. The power source is normally a battery that ramps down slowly. This means that the LVD circuity can be disabled for most of the time, and only enabled occasionally to do the device voltage check.

Question 3: ***Should I enable the BOR circuit for a battery powered application?***

Answer: The BOR circuit is intended to protect the device from improper operation due to power supply fluctuations caused by the AC line voltage. The BOR is typically not required for battery applications and can be disabled for lower current consumption.

9.4 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Low Voltage Detect module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F Family of devices.

9.5 Revision History

Revision A

This is the initial released revision of this document.

Revision B

There were no technical content or editorial revisions to this section of the manual, however, this section was updated to reflect Revision B throughout the manual.

Revision C

There were no technical content revisions to this section of the manual, however, this section was updated to reflect Revision C throughout the manual.