# Section 8. Reset

## HIGHLIGHTS

This section of the manual contains the following topics:

## 8.1 Introduction

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- EXTR: Pin Reset (MCLR)
- SWR: RESET Instruction
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- TRAPR: Trap Conflict Reset
- IOPR: Illegal Opcode Reset
- UWR: Uninitialized W Register Reset

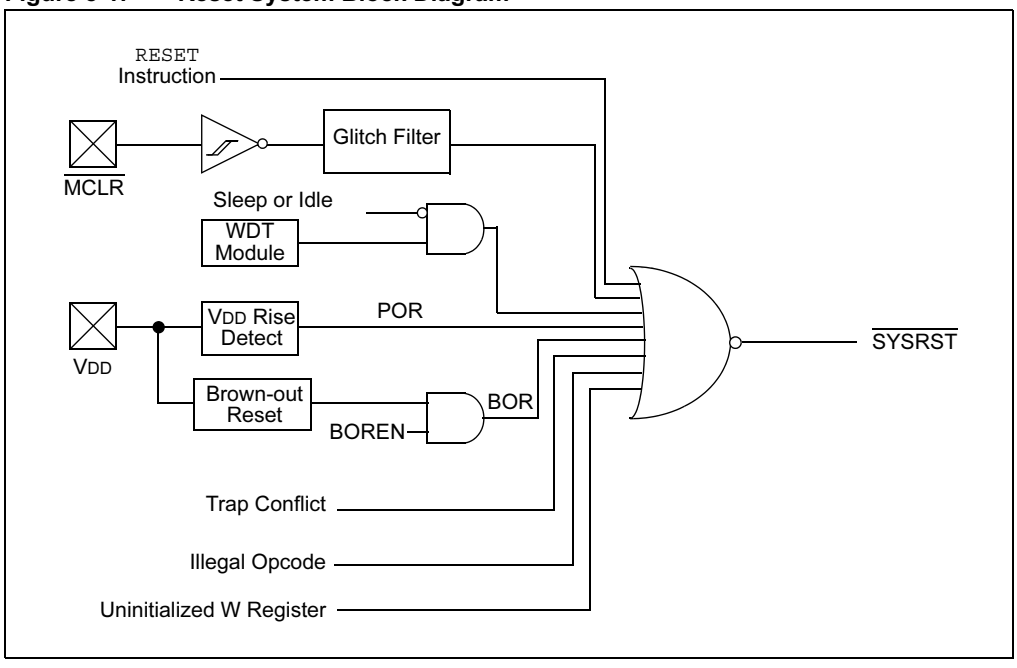
A simplified block diagram of the Reset module is shown in Figure 8-1. Any active source of Reset will make the SYSRST signal active. Many registers associated with the CPU and peripherals are forced to a known "Reset state". Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

| **Note:** | Refer to the specific peripheral or CPU section of this manual for register Reset states. |
|---|---|

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 8-1). A POR will clear all bits except for the POR and BOR bits (RCON<2:1>), which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Low Voltage Detect module, Watchdog Timer, and device power saving states. The function of these bits is discussed in other sections of this manual.

**Figure 8-1: Reset System Block Diagram**



**Register 8-1: RCON: Reset Control Register**

| Upper Byte: | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-1 |
| TRAPR | IOPUWR | BGST | LVDEN | LVDL<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| Lower Byte: | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
| EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal Address mode, or uninitialized W register used as an address pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13 **BGST:** Bandgap Stable bit
1 = The bandgap has stabilized
0 = Bandgap is not stable and LVD interrupts should be disabled

bit 12 **LVDEN:** Low Voltage Detect Power Enable bit
1 = Enables LVD, powers up LVD circuit
0 = Disables LVD, powers down LVD circuit

bit 11-8 **LVDL<3:0>:** Low Voltage Detection Limit bits
Refer to **Section 9. "Low Voltage Detect (LVD)"** for further details.

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit
1 = WDT is turned on
0 = WDT is turned off

**Note:** If FWDTEN fuse bit is '1' (unprogrammed), the WDT is ALWAYS ENABLED, regardless of the SWDTEN bit setting.

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

**Register 8-1: RCON: Reset Control Register (Continued)**

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred. Note that BOR is also set after Power-on Reset.
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-up Reset has occurred
0 = A Power-up Reset has not occurred

| **Note:** | All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset. |
|---|---|

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

## 8.2 Clock Source Selection at Reset

If clock switching is enabled, the system clock source at device Reset is chosen as shown in Table 8-1. If clock switching is disabled, the system clock source is always selected according to the oscillator configuration fuses. Refer to **Section 7. "Oscillator"** for further details.

**Table 8-1: Oscillator Selection vs. Type of Reset (Clock Switching Enabled)**

| Reset Type | Clock Source Selected Based On |
|---|---|
| POR | Oscillator Configuration Fuses |
| BOR | Oscillator Configuration Fuses |
| EXTR | COSC Control bits (OSCCON<13:12>) |
| WDTR | COSC Control bits (OSCCON<13:12>) |
| SWR | COSC Control bits (OSCCON<13:12>) |

## 8.3 POR: Power-on Reset

There are two threshold voltages associated with a Power-on Reset (POR). The first voltage is the device threshold voltage, VPOR. The device threshold voltage is the voltage at which the device logic circuits become operable. The second voltage associated with a POR event is the POR circuit threshold voltage which is nominally 1.85V.

A power-on event will generate an internal Power-on Reset pulse when a VDD rise is detected. The Reset pulse will be generated at VPOR. The device supply voltage characteristics must meet specified starting voltage and rise rate requirements to generate the POR pulse. In particular, VDD must fall below VPOR before a new POR is initiated. For more information on the VPOR and the VDD rise rate specifications, please refer to the "Electrical Specifications" section of the device data sheet.

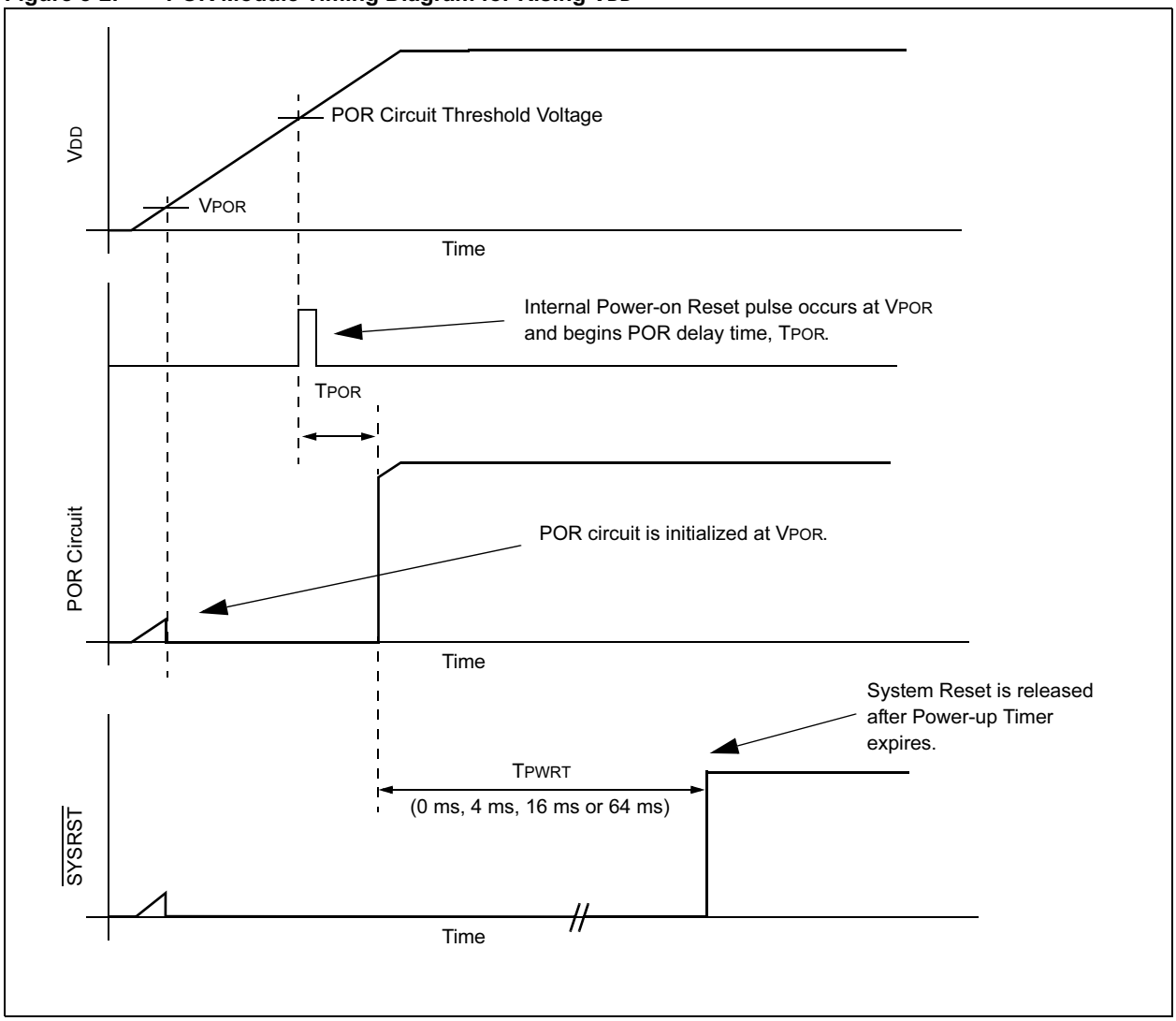
The POR pulse will reset a POR timer and place the device in the Reset state. The POR also selects the device clock source identified by the oscillator configuration bits.

After the Power-on Reset pulse is generated, the POR circuit inserts a small delay, TPOR, which is nominally 10 μs and ensures that internal device bias circuits are stable. Furthermore, a user selected Power-up Time-out (TPWRT) may be applied. The TPWRT parameter is based on device configuration bits and can be 0 ms (no delay), 4 ms, 16 ms or 64 ms. The total delay time at device power-up is TPOR + TPWRT. When these delays have expired, $\overline{\text{SYSRST}}$ will be released on the next leading edge of the instruction cycle clock, and the PC will jump to the Reset vector.

The timing for the $\overline{\text{SYSRST}}$ signal is shown in Figure 8-2. A Power-on Reset is initialized when VDD falls below a threshold voltage, VT. The POR delay time is inserted when VDD crosses the POR circuit threshold voltage. Finally, the PWRT delay time, TPWRT, is inserted before $\overline{\text{SYSRST}}$ is released.

The power-on event will set the POR and BOR status bits (RCON<1:0>).

**Figure 8-2: POR Module Timing Diagram for Rising VDD**




| | |
|---|---|
| **Note:** | When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges, otherwise the device will not function correctly. The user must ensure that the delay between the time power is first applied and the time $\overline{\text{SYSRST}}$ becomes inactive is long enough to get all operating parameters within specification. |

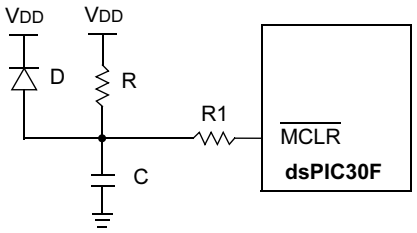
### 8.3.1 Using the POR Circuit

To take advantage of the POR circuit, just tie the MCLR pin directly to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise time for VDD is required. Refer to the "Electrical Specifications" section in the specific device data sheet for further details.

Depending on the application, a resistor may be required between the MCLR pin and VDD. This resistor can be used to decouple the MCLR pin from a noisy power supply rail. The resistor will also be necessary if the device programming voltage, VPP, needs to be placed on the MCLR pin while the device is installed in the application circuit. VPP is 13 volts for most devices.

Figure 8-3 shows a possible POR circuit for a slow power supply ramp up. The external Power-on Reset circuit is only required if the device would exit Reset before the device VDD is in the valid operating range. The diode, D, helps discharge the capacitor quickly when VDD powers down.

**Figure 8-3: External Power-on Reset Circuit (For Slow VDD Rise Time)**




**Note 1:** The value of R should be low enough so that the voltage drop across it does not violate the VIH specification of the MCLR pin.

**2:** R1 will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

### 8.3.2 Power-up Timer (PWRT)

The PWRT provides an optional time delay (TPWRT) before SYSRST is released at a device POR or BOR (Brown-out Reset). The PWRT time delay is provided in addition to the POR delay time (TPOR). The PWRT time delay may be 0 ms, 4 ms, 16 ms or 64 ms nominal (see Figure 8-2).

The PWRT delay time is selected using the FPWRT<1:0> configuration fuses in the FBORPOR Device Configuration register. Refer to **Section 24. "Device Configuration"** for further details.

## 8.4 External Reset (EXTR)

Whenever the MCLR pin is driven low, the device will asynchronously assert SYSRST, provided the input pulse on MCLR is longer than a certain minimum width. (Refer to the "Electrical Specifications" in the specific device data sheet for further details.) When the MCLR pin is released, SYSRST will be released on the next instruction clock cycle, and the Reset vector fetch will commence. The processor will maintain the existing clock source that was in use before the EXTR occurred. The EXTR status bit (RCON<7>) will be set to indicate the MCLR Reset.

## 8.5 Software `RESET` Instruction (SWR)

Whenever the `RESET` instruction is executed, the device will assert SYSRST, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the `RESET` instruction will remain. SYSRST will be released at the next instruction cycle, and the Reset vector fetch will commence.

## 8.6 Watchdog Time-out Reset (WDTR)

Whenever a Watchdog time-out occurs, the device will asynchronously assert SYSRST. The clock source will remain unchanged. Note that a WDT time-out during Sleep or Idle mode will wake-up the processor, but NOT reset the processor. For more information, refer to **Section 10. "Watchdog Timer and Power Saving Modes"**.

## 8.7 Brown-out Reset (BOR)

The BOR (Brown-out Reset) module is based on an internal voltage reference circuit. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (i.e., missing waveform portions of the AC cycles due to bad power transmission lines), or voltage sags due to excessive current draw when a large load is energized.

The BOR module allows selection of one of the following voltage trip points:

- $V_{BOR}$ = 2.0V
- $V_{BOR}$ = 2.7V
- $V_{BOR}$ = 4.2V
- $V_{BOR}$ = 4.5V

| **Note:** | The BOR voltage trip points indicated here are nominal values provided for design guidance only. Refer to the “Electrical Specifications” in the specific device data sheet for BOR voltage limit specifications. |
|---|---|

On a BOR, the device will select the system clock source based on the device configuration bit values (FPR<3:0>, FOS<1:0>). The PWRT time-out ($T_{PWRT}$), if enabled, will be applied before $\overline{SYSRST}$ is released.

If a crystal oscillator source is selected, the Brown-out Reset will invoke the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If a system clock source is derived from the PLL, then the clock will be held until the LOCK bit (OSCCON<5>) is set.

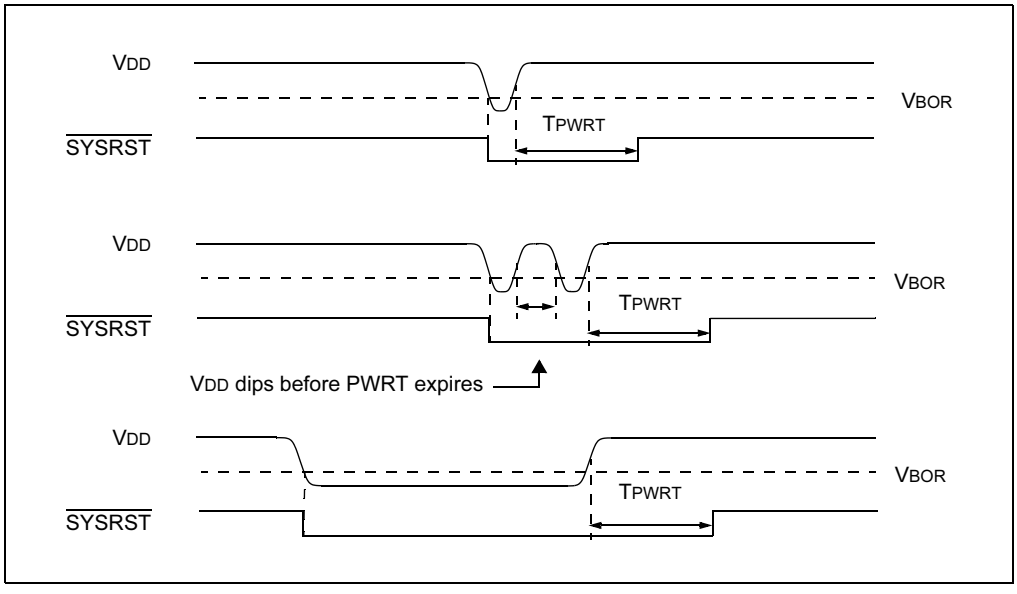
The BOR status bit (RCON<1>) will be set to indicate that a BOR has occurred.

The BOR circuit, if enabled, will continue to operate while in Sleep or Idle modes and will reset the device should $V_{DD}$ fall below the BOR threshold voltage.

Refer to the “Electrical Specifications” section of the appropriate device data sheet for the BOR electrical specifications.

Typical brown-out scenarios are shown in Figure 8-4. As shown, a PWRT delay (if enabled) will be initiated each time $V_{DD}$ rises above the $V_{BOR}$ trip point.

**Figure 8-4: Brown-out Situations**



### 8.7.1 BOR Configuration

The BOR module is enabled/disabled and configured via device configuration fuses.

The BOR module is enabled by default and may be disabled (to reduce power consumption) by programming the BOREN device configuration fuse to a '0' (FBORPOR<7>). The BOREN configuration fuse is located in the FBORPOR Device Configuration register. The BOR voltage trip point ($V_{BOR}$) is selected using the BORV<1:0> configuration fuses (FBOR<5:4>). Refer to **Section 24. "Device Configuration"** for further details.

### 8.7.2 Current Consumption for BOR Operation

The BOR circuit relies on an internal voltage reference circuit that is shared with other peripheral devices, such as the Low Voltage Detect module. The internal voltage reference will be active whenever one of its associated peripherals is enabled. For this reason, the user may not observe the expected change in current consumption when the BOR is disabled.

### 8.7.3 Illegal Opcode Reset

A device Reset will be generated if the device attempts to execute an illegal opcode value that was fetched from program memory. The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with `0x3F`, which is an illegal opcode value.

If a device Reset occurs as a result of an illegal opcode value, the IOPUWR status bit (RCON<14>) will be set.

### 8.7.4 Uninitialized W Register Reset

The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to. An attempt to use an uninitialized register as an address pointer will reset the device. Furthermore, the IOPUWR status bit (RCON<14>) will be set.

### 8.7.5 Trap Conflict Reset

A device Reset will occur whenever multiple hard trap sources become pending at the same time. The TRAPR status bit (RCON<15>) will be set. Refer to **Section 6. "Reset Interrupts"** for more information on Trap Conflict Resets.

### 8.8 Using the RCON Status Bits

The user can read the RCON register after any device Reset to determine the cause of the Reset.

| **Note:** | The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful. |
|---|---|

Table 8-2 provides a summary of the Reset flag bit operation.

**Table 8-2: Reset Flag Bit Operation**

| Flag Bit | Set by: | Cleared by: |
|---|---|---|
| **TRAPR** (RCON<15>) | Trap conflict event | POR |
| **IOPWR** (RCON<14>) | Illegal opcode or uninitialized W register access | POR |
| **EXTR** (RCON<7>) | $\overline{\text{MCLR}}$ Reset | POR |
| **SWR** (RCON<6>) | `RESET` instruction | POR |
| **WDTO** (RCON<4>) | WDT time-out | `PWRSAV` instruction, POR |
| **SLEEP** (RCON<3>) | `PWRSAV #SLEEP` instruction | POR |
| **IDLE** (RCON<2>) | `PWRSAV #IDLE` instruction | POR |
| **BOR** (RCON<1>) | POR, BOR | |
| **POR** (RCON<0>) | POR | |

**Note:** All RESET flag bits may be set or cleared by the user software.

## 8.9 Device Reset Times

The Reset times for various types of device Reset are summarized in Table 8-3. Note that the system Reset signal, SYSRST, is released after the POR delay time and PWRT delay times expire.

The time that the device actually begins to execute code will also depend on the system oscillator delays, which include the Oscillator Start-up Timer (OST) and the PLL lock time. The OST and PLL lock times occur in parallel with the applicable SYSRST delay times.

The FSCM delay determines the time at which the FSCM begins to monitor the system clock source after the SYSRST signal is released.

**Table 8-3: Reset Delay Times for Various Device Resets**

| Reset Type | Clock Source | $\overline{\text{SYSRST}}$ Delay | System Clock Delay | FSCM Delay | Notes |
|---|---|---|---|---|---|
| POR | EC, EXTRC, FRC, LPRC | TPOR + TPWRT | — | — | **1, 2** |
| | EC + PLL | TPOR + TPWRT | TLOCK | TFSCM | **1, 2, 4, 5** |
| | XT, HS, XTL, LP | TPOR + TPWRT | TOST | TFSCM | **1, 2, 3, 5** |
| | XT + PLL | TPOR + TPWRT | TOST + TLOCK | TFSCM | **1, 2, 3, 4, 5** |
| BOR | EC, EXTRC, FRC, LPRC | TPWRT | — | — | **2** |
| | EC + PLL | TPWRT | TLOCK | TFSCM | **1, 2, 4, 5** |
| | XT, HS, XTL, LP | TPWRT | TOST | TFSCM | **1, 2, 3, 5** |
| | XT + PLL | TPWRT | TOST + TLOCK | TFSCM | **1, 2, 3, 4, 5** |
| $\overline{\text{MCLR}}$ | Any Clock | — | — | — | |
| WDT | Any Clock | — | — | — | |
| Software | Any clock | — | — | — | |
| Illegal Opcode | Any Clock | — | — | — | |
| Uninitialized W | Any Clock | — | — | — | |
| Trap Conflict | Any Clock | — | — | — | |

**Note 1:** TPOR = Power-on Reset delay (10 μs nominal).

**2:** TPWRT = Additional "power-up" delay as determined by the FPWRT<1:0> configuration bits. This delay is 0 ms, 4 ms, 16 ms or 64 ms nominal.

**3:** TOST = Oscillator Start-up Timer. A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.

**4:** TLOCK = PLL lock time (20 μs nominal).

**5:** TFSCM = Fail-Safe Clock Monitor delay (100 μs nominal).

### 8.9.1 POR and Long Oscillator Start-up Times

The oscillator start-up circuitry and its associated delay timers is not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The oscillator start-up timer has NOT expired (if a crystal oscillator is used).
- The PLL has not achieved a LOCK (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

### 8.9.2 Fail-Safe Clock Monitor (FSCM) and Device Resets

If the FSCM is enabled, it will begin to monitor the system clock source when $\overline{\text{SYSRST}}$ is released. If a valid clock source is not available at this time, the device will automatically switch to the FRC oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine.

#### 8.9.2.1 FSCM Delay for Crystal and PLL Clock Sources

When the system clock source is provided by a crystal oscillator and/or the PLL, a small delay, $T_{FSCM}$, will automatically be inserted after the POR and PWRT delay times. The FSCM will not begin to monitor the system clock source until this delay expires. The FSCM delay time is nominally 100 μs and provides additional time for the oscillator and/or PLL to stabilize. In most cases, the FSCM delay will prevent an oscillator failure trap at a device Reset when the PWRT is disabled.

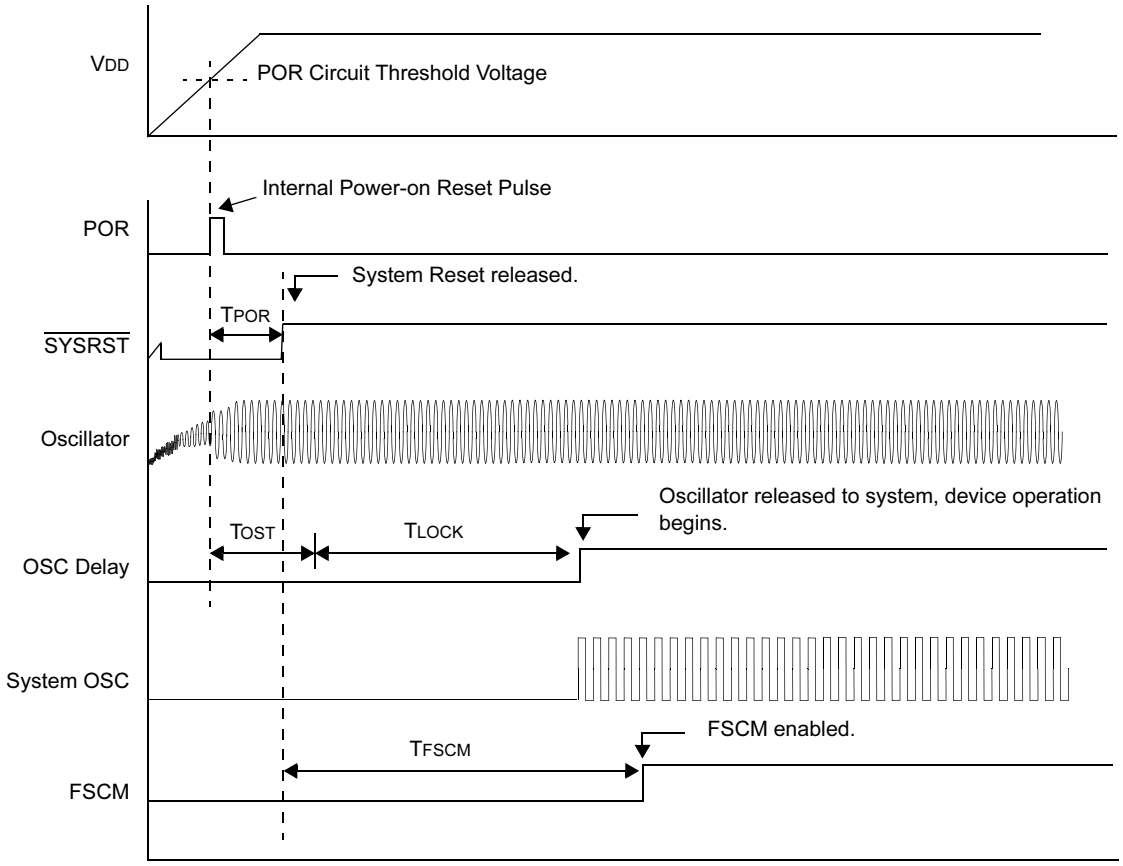
### 8.10 Device Start-up Time Lines

Figure 8-5 through Figure 8-8 show graphical time lines of the delays associated with device Reset for several operating scenarios.

Figure 8-5 shows the delay time line when a crystal oscillator and PLL are used as the system clock and the PWRT is disabled. The internal Power-on Reset pulse occurs at the VPOR threshold. A small POR delay occurs after the internal Reset pulse. (The POR delay is always inserted before device operation begins.)

The FSCM, if enabled, begins to monitor the system clock for activity when the FSCM delay expires. Figure 8-5 shows that the oscillator and PLL delays expire before the Fail-Safe Clock Monitor (FSCM) is enabled. However, it is possible that these delays may not expire until after FSCM is enabled. In this case, the FSCM would detect a clock failure and a clock failure trap will be generated. If the FSCM delay does not provide adequate time for the oscillator and PLL to stabilize, the PWRT could be enabled to allow more delay time before device operation begins and the FSCM starts to monitor the system clock.

**Figure 8-5: Device Reset Delay, Crystal + PLL Clock Source, PWRT Disabled**




**Note 1:** Delay times shown are not drawn to scale.

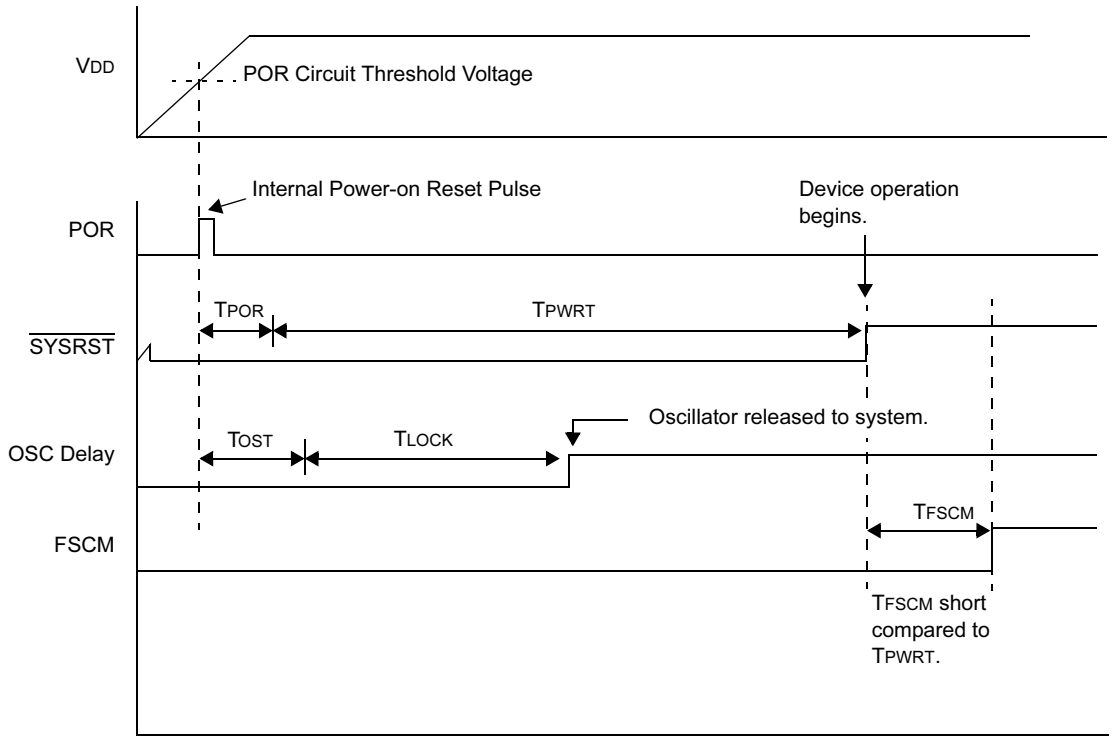
**2:** FSCM, if enabled, monitors system clock at expiration of TPOR + TFSCM.

**3:** TLOCK not inserted when PLL is disabled.

The Reset time line shown in Figure 8-6 is similar to that shown in Figure 8-5, except that the PWRT has been enabled to increase the amount of delay time before SYSRST is released.

The FSCM, if enabled, will begin to monitor the system clock after TFSCM expires. Note that the additional PWRT delay time added to TFSCM provides ample time for the system clock source to stabilize in most cases.

**Figure 8-6: Device Reset Delay, Crystal + PLL Clock Source, PWRT Enabled**



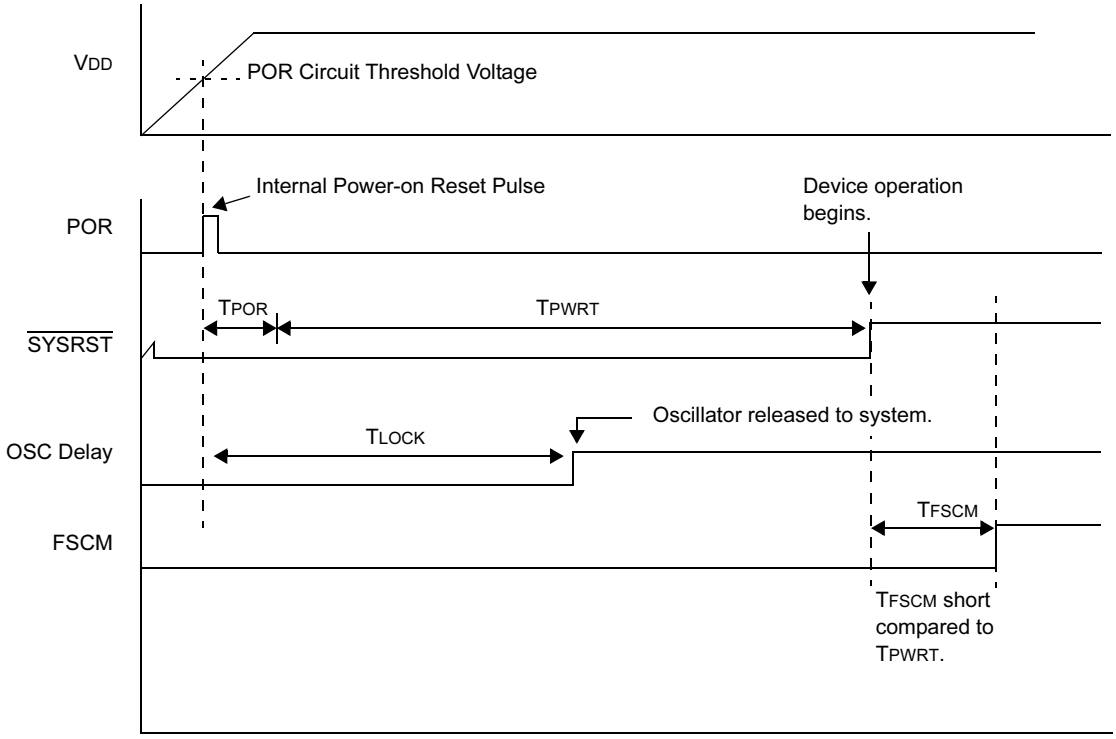

**Note 1:** Delay times shown are not drawn to scale.

**2:** FSCM, if enabled, monitors system clock at expiration of TPOR + TPWRT + TFSCM.

**3:** TLOCK not inserted when PLL is is disabled.

The Reset time line in Figure 8-7 shows an example when an EC + PLL clock source is used as the system clock and the PWRT is enabled. This example is similar to the one shown in Figure 8-6, except that the oscillator start-up timer delay, TOST, does not occur.

**Figure 8-7: Device Reset Delay, EC + PLL Clock, PWRT Enabled**



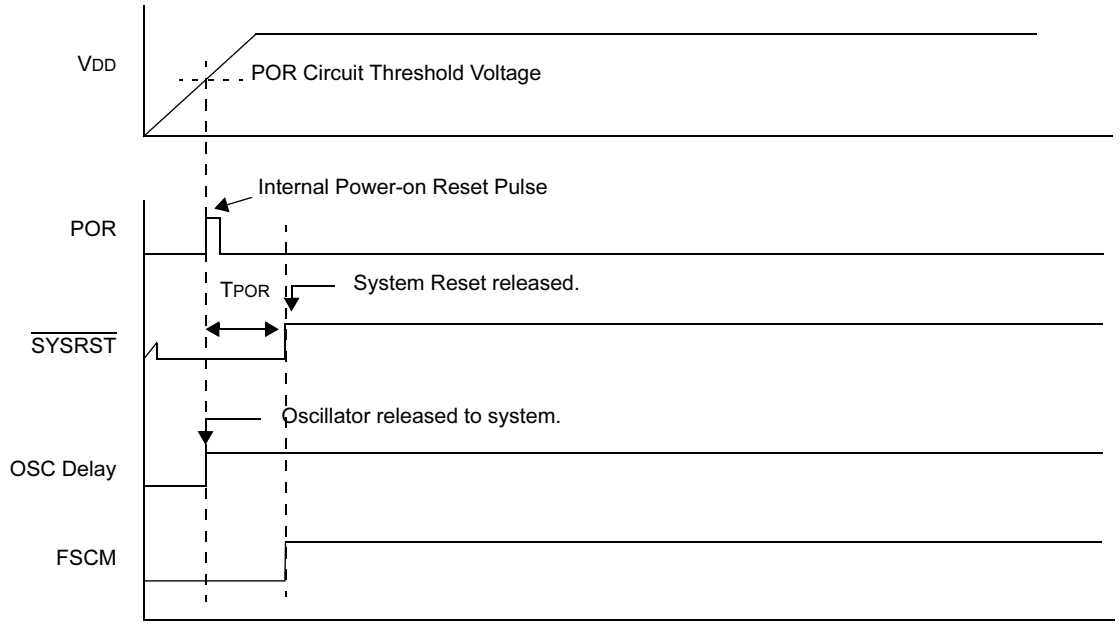

**Note 1:** Delay times shown are not drawn to scale.

**2:** FSCM, if enabled, monitors system clock at expiration of TPOR + TPWRT + TFSCM.

**3:** TLOCK not inserted when PLL is is disabled.

The Reset time line shown in Figure 8-8 shows an example where an EC without PLL, or RC system clock source is selected and the PWRT is disabled. Note that this configuration provides minimal Reset delays. The POR delay is the only delay time that occurs before device operation begins. No FSCM delay will occur if the FSCM is enabled, because the system clock source is not derived from a crystal oscillator or the PLL.

**Figure 8-8: Device Reset Delay, EC or RC Clock, PWRT Disabled**




**Note 1:** Delay times shown are not drawn to scale.

**2:** If enabled, FSCM will begin to monitor system clock at expiration of TPOR.

## 8.11 Special Function Register Reset States

Most of the special function registers (SFRs) associated with the dsPIC30F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in each section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of two registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the oscillator configuration bits in the FOSC Device Configuration register (see Table 8-1).

## 8.12 Design Tips

**Question 1:** ***How do I use the RCON register?***

**Answer:** The initialization code after a Reset should examine RCON and confirm the source of the Reset. In certain applications, this information can be used to take appropriate action to correct the problem that caused the Reset to occur. All Reset status bits in the RCON register should be cleared after reading them to ensure the RCON value will provide meaningful results after the next device Reset.

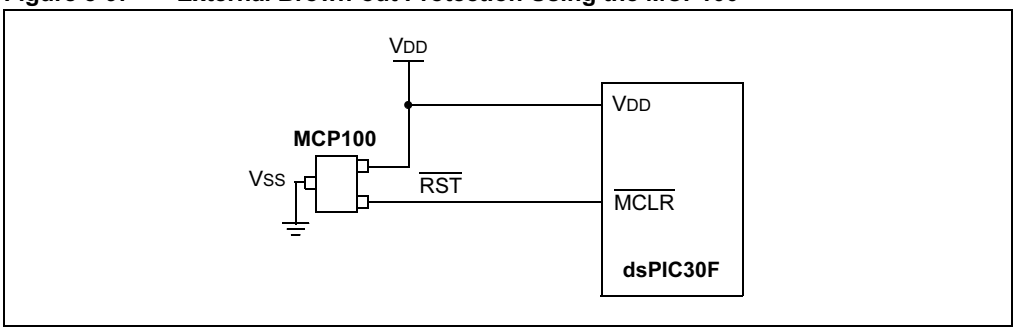
**Question 2:** ***How should I use BOR in a battery operated application?***

**Answer:** The BOR feature is not designed to operate as a low battery detect, and should be disabled in battery operated systems (to save current). The Low Voltage Detect peripheral can be used to detect when the battery has reached its end of life voltage.

**Question 3:** ***The BOR module does not have the programmable trip points that my application needs. How can I work around this?***

**Answer:** There are some applications where the device's programmable BOR trip point levels may still not be at the desired level for the application. Figure 8-9 shows a possible circuit for external brown-out protection, using the MCP100 system supervisor.

**Figure 8-9: External Brown-out Protection Using the MCP100**




**Question 4:** ***I initialized a W register with a 16-bit address, but the device appears to reset when I attempt to use the register as an address.***

**Answer:** Because all data addresses are 16 bit values, the uninitialized W register logic only recognizes that a register has been initialized correctly if it was subjected to a word load. Two byte moves to a W register, even if successive, will not work, resulting in a device Reset if the W register is used as an address pointer in an operation.

## 8.13 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Reset module are:

| Title | Application Note # |
|---|---|
| Power-up Trouble Shooting | AN607 |
| Power-up Considerations | AN522 |

**Note:** Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F Family of devices.

## 8.14 Revision History

### Revision A

This is the initial released revision of this document.

### Revision B

There were no technical content or editorial revisions to this section of the manual, however, this section was updated to reflect Revision B throughout the manual.

### Revision C

There were no technical content revisions to this section of the manual, however, this section was updated to reflect Revision C throughout the manual.

**NOTES:**