Section 7. Oscillator

HIGHLIGHTS

This section of the manual contains the following topics:

7.1 Introduction

This section describes the operation of the oscillator system for dsPIC30F devices in the General Purpose, Sensor and Motor Control families. The oscillator system has the following modules and features:

- Various external and internal oscillator options as clock sources
- An on-chip PLL to boost internal operating frequency
- Clock switching between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- Device clocking controlled by Special Function Registers as well as nonvolatile Configuration bits

A simplified diagram of the oscillator system is shown in Figure 7-1.

7.1.1 Oscillator System Features Summary

dsPIC30F devices in the General Purpose, Sensor and Motor Control families feature one of three versions of the oscillator system – VERSION 1, VERSION 2 and VERSION 3. The features of the three versions of the oscillator system are summarized in Table 7-1.

Note: Refer to the device data sheet to determine the version of the oscillator system featured on the dsPIC30F device you are using.

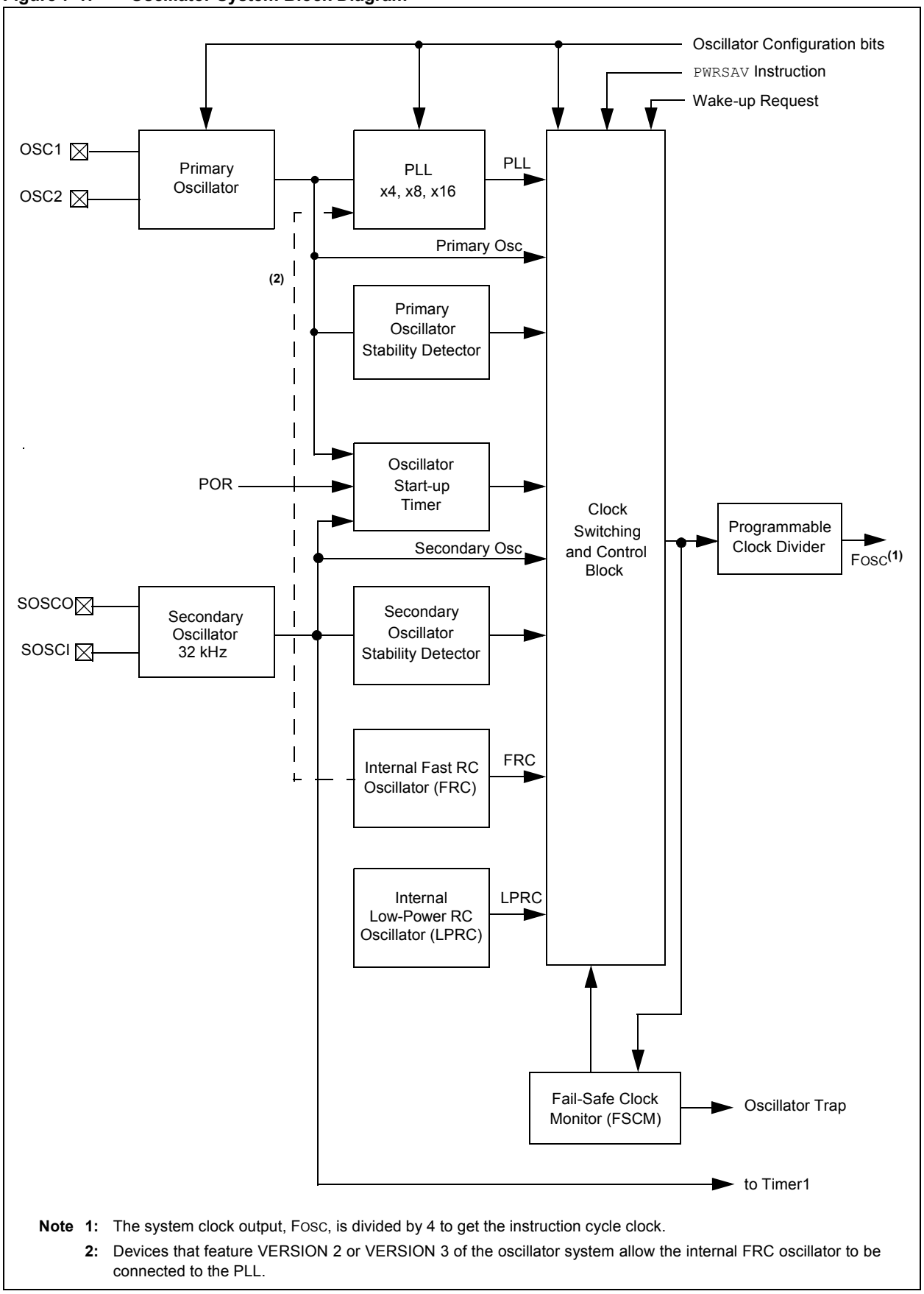
Table 7-1: Device-Specific Oscillator System Feature Summary

Oscillator System	dsPIC30F Device	Feature Summary
VERSION 1	30F6010, 30F6011, 30F6012, 30F6013, 30F6014	**Oscillator Sources:** • Primary Oscillator with Multiple Clock modes – XT, EC, HS • Secondary Oscillator (Low-Power 32 kHz Crystal Oscillator) • FRC Oscillator: Fast Internal RC (7.37 MHz) • LPRC Oscillator: Low-Power Internal RC (512 kHz) **PLL Clock Multiplier:** • 4 MHz-10 MHz Input Frequency Range • 4x Multiplier mode (FOUT = 16 MHz-40 MHz) • 8x Multiplier mode (FOUT = 32 MHz-80 MHz) • 16x Multiplier mode (FOUT = 64 MHz-120 MHz) • PLL VCO Lock Indication plus ‘out of lock’ Trap Option • PLL Input Provided by the Following Sources: - XT or EC Primary Oscillator **Clock Scaling Options:** Generic postscaler for device clock (divide by 4, 16, 64) **Fail-Safe Clock Monitor (FSCM):** Detects clock failure and switches over to internal FRC oscillator
VERSION 2	30F2010, 30F4011, 30F4012, 30F5011, 30F5013	Oscillator System VERSION 2 adds the following capabilities to VERSION 1: • Internal FRC oscillator may also be provided as an input to the PLL to allow fast execution while eliminating the need for an external clock source (this feature is applicable to all devices other than the 30F2010) • User tuning capability added for the Internal FRC oscillator

Table 7-1: Device-Specific Oscillator System Feature Summary (Continued)

Oscillator System	dsPIC30F Device	Feature Summary
VERSION 3	30F2011, 30F2012, 30F3010, 30F3011, 30F3012, 30F3013, 30F3014, 30F4013, 30F5015, 30F5016, 30F6010A, 30F6011A, 30F6012A, 30F6013A, 30F6014A, 30F6015	Oscillator System VERSION 3 adds the following capabilities to VERSION 2: • HS oscillator may also be provided as an input to the PLL to allow greater choices of crystal frequency

Figure 7-1: Oscillator System Block Diagram



Note 1: The system clock output, FOSC, is divided by 4 to get the instruction cycle clock.

2: Devices that feature VERSION 2 or VERSION 3 of the oscillator system allow the internal FRC oscillator to be connected to the PLL.

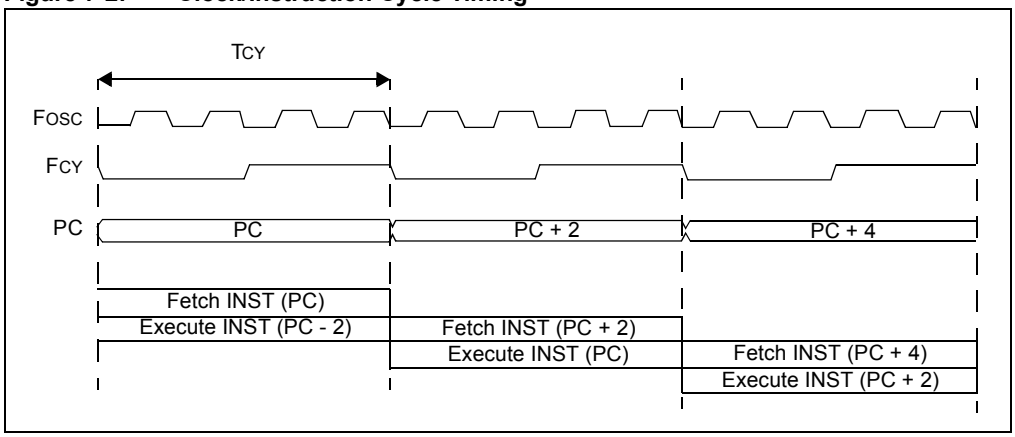
7.2 Device Clocking and MIPS

Referring to Figure 7-1, the system clock source can be provided by one of four sources. These sources are the Primary oscillator, Secondary oscillator, Internal Fast RC (FRC) oscillator or the Low-Power RC (LPRC) oscillator. The primary oscillator source has the option of using the internal PLL. The frequency of the selected clock source can optionally be reduced by the programmable postscaler (clock divider). The output from the programmable postscaler becomes the system clock source, FOSC.

The system clock source is divided by four to produce the internal instruction cycle clock, FCY. In this document, the instruction cycle clock is also denoted by FOSC/4. The timing diagram in Figure 7-2 shows the relationship between the system clock source and instruction execution.

The internal instruction cycle clock, FCY, can be provided on the OSC2 I/O pin for some operating modes of the primary oscillator (see **Section 7.3 "Oscillator Configuration"**).

Figure 7-2: Clock/Instruction Cycle Timing



Equation 7-1: MIPS and Source Oscillator Frequency Relationship

$$FCY = \frac{FOSC}{4} = \left(\frac{\text{SOURCE OSCILLATOR FREQUENCY} * \text{PLL MULTIPLIER}}{\text{PROGRAMMABLE POSTSCALER} * 4} \right)$$

7.3 Oscillator Configuration

The oscillator source (and operating mode) that is used at a device Power-on Reset event is selected using nonvolatile Configuration bits. The oscillator Configuration bits are located in the FOSC Configuration register.

The FOS bits in the FOSC nonvolatile Configuration register select the oscillator source that is used at a Power-on Reset. The primary oscillator is the default (unprogrammed) selection. The secondary oscillator, or one of the internal oscillators, may be chosen by programming these bit locations.

The FPR bits in the FOSC nonvolatile Configuration register select the operating mode of the primary oscillator.

dsPIC30F devices in the General Purpose, Sensor and Motor Control families may feature one of three versions of the oscillator system. The definition of the FOSC nonvolatile Configuration register varies between these versions, as described in the sub-sections below.

7.3.1 Oscillator System VERSION 1 Configuration

For devices that feature the oscillator system VERSION 1, the FOSC nonvolatile Configuration register is shown in Register 7-1. The operating modes for the FPR bits may be selected as shown in Table 7-2.

7.3.2 Oscillator System VERSION 2 Configuration

For devices that feature the oscillator system VERSION 2, the FOSC nonvolatile Configuration register is shown in Register 7-2. The operating modes for the FPR bits may be selected as shown in Table 7-3.

7.3.3 Oscillator System VERSION 3 Configuration

For devices that feature the oscillator system VERSION 3, the FOSC nonvolatile Configuration register is shown in Register 7-3. The operating modes for the FPR bits may be selected as shown in Table 7-4.

7.3.4 Clock Switching Mode Configuration Bits

The FCKSM<1:0> Configuration bits (FOSC<15:14>) are used to enable/disable device clock switching and the Fail-Safe Clock Monitor (FSCM). When these bits are unprogrammed (default), clock switching and the FSCM are disabled. These bits carry the same definition and functionality across all versions of the oscillator system.

Register 7-1: FOSC: Oscillator Configuration Register for Oscillator System VERSION 1

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
R/P	R/P	U	U	U	U	R/P	R/P
FCKSM<1:0>		—	—	—	—	FOS<1:0>	
bit 15							bit 8

Lower Byte:							
U	U	U	U	R/P	R/P	R/P	R/P
—	—	—	—	FPR<3:0>			
bit 7							bit 0

bit 23-16 **Unimplemented:** Read as '0'

bit 15-14 **FCKSM<1:0>:** Clock Switching Mode Selection Fuses bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-10 **Unimplemented:** Read as '0'

bit 9-8 **FOS<1:0>:** Oscillator Source Selection on POR bits
11 = Primary oscillator (Primary Oscillator mode selected by FPR<3:0>)
10 = Internal low-power RC oscillator
01 = Internal fast RC oscillator
00 = Low-power 32 kHz oscillator (Timer1 oscillator)

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **FPR<3:0>:** Oscillator Selection within Primary Group bits (see Table 7-2)

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Table 7-2: Oscillator System VERSION 1: Configuration Bit Values for Clock Selection

Oscillator Mode	Oscillator Source	FOS<1:0>		FPR<3:0>				OSC2 Pin Function
EC w/PLL 16x	Primary	1	1	1	1	1	1	I/O **(Note 4)**
EC w/PLL 8x	Primary	1	1	1	1	1	0	I/O
EC w/PLL 4x	Primary	1	1	1	1	0	1	I/O
ECIO	Primary	1	1	1	1	0	0	I/O
EC	Primary	1	1	1	0	1	1	FOSC/4
Reserved	Primary	1	1	1	0	1	0	n/a
ERC	Primary	1	1	1	0	0	1	FOSC/4
ERCIO	Primary	1	1	1	0	0	0	I/O
XT w/PLL 16x	Primary	1	1	0	1	1	1	**(Note 3)**
XT w/PLL 8x	Primary	1	1	0	1	1	0	**(Note 3)**
XT w/PLL 4x	Primary	1	1	0	1	0	1	**(Note 3)**
XT	Primary	1	1	0	1	0	0	**(Note 3)**
HS	Primary	1	1	0	0	1	x	**(Note 3)**
XTL	Primary	1	1	0	0	0	x	**(Note 3)**
LP	Secondary	0	0	—	—	—	—	**(Notes 1, 2)**
FRC	Internal	0	1	—	—	—	—	**(Notes 1, 2)**
LPRC	Internal	1	0	—	—	—	—	**(Notes 1, 2)**

Note 1: OSC2 pin function is determined by the Primary Oscillator mode selection (FPR<3:0> Configuration bits).

2: Note that OSC1 pin cannot be used as an I/O pin, even if the Secondary oscillator or an internal clock source is selected at all times.

3: In these Oscillator modes, a crystal is connected between the OSC1 and OSC2 pins.

4: This is the default Oscillator mode for an unprogrammed (erased) device. An unprogrammed Configuration bit has a value of '1'.

5: XTL – XTL Crystal Oscillator mode (200 kHz-4 MHz crystal).

6: XT – XT Crystal Oscillator mode (4 MHz-10 MHz crystal).

7: HS – HS Crystal Oscillator mode (10 MHz-25 MHz crystal).

Register 7-2: FOSC: Oscillator Configuration Register for Oscillator System VERSION 2

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
R/P	R/P	U	U	U	U	R/P	R/P
FCKSM<1:0>		—	—	—	—	FOS<1:0>	
bit 15							bit 8

Lower Byte:							
U	U	U	U	R/P	R/P	R/P	R/P
—	—	—	—	FPR<3:0>			
bit 7							bit 0

bit 23-16 **Unimplemented:** Read as '0'

bit 15-14 **FCKSM<1:0>:** Clock Switching Mode Selection Fuses bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-10 **Unimplemented:** Read as '0'

bit 9-8 **FOS<1:0>:** Oscillator Source Selection on POR bits
11 = Primary oscillator (Primary Oscillator mode selected by FPR<3:0>)
10 = Internal low-power rc oscillator
01 = Internal fast RC oscillator
00 = Low-power 32 khz oscillator (Timer1 oscillator)

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **FPR<3:0>:** Oscillator Mode Selection within Primary Group bits (see Table 7-3)

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Table 7-3: Oscillator System VERSION 2: Configuration Bit Values for Clock Selection:

Oscillator Mode	Oscillator Source	FOS<1:0>		FPR<3:0>				OSC2 Pin Function
EC	Primary	1	1	1	0	1	1	CLKO
ECIO	Primary	1	1	1	1	0	0	I/O
EC w/PLL 4x	Primary	1	1	1	1	0	1	I/O
EC w/PLL 8x	Primary	1	1	1	1	1	0	I/O
EC w/PLL 16x	Primary	1	1	1	1	1	1	I/O **(Note 4)**
ERC	Primary	1	1	1	0	0	1	CLKO
ERCIO	Primary	1	1	1	0	0	0	I/O
XT	Primary	1	1	0	1	0	0	**(Note 3)**
XT w/PLL 4x	Primary	1	1	0	1	0	1	**(Note 3)**
XT w/PLL 8x	Primary	1	1	0	1	1	0	**(Note 3)**
XT w/PLL 16x	Primary	1	1	0	1	1	1	**(Note 3)**
XTL	Primary	1	1	0	0	0	0	**(Note 3)**
HS	Primary	1	1	0	0	1	0	**(Note 3)**
FRC w/PLL 4x	Primary	1	1	0	0	0	1	I/O
FRC w/PLL 8x	Primary	1	1	1	0	1	0	I/O
FRC w/PLL 16x	Primary	1	1	0	0	1	1	I/O
LP	Secondary	0	0	—	—	—	—	**(Notes 1, 2)**
FRC	Internal FRC	0	1	—	—	—	—	**(Notes 1, 2)**
LPRC	Internal LPRC	1	0	—	—	—	—	**(Notes 1, 2)**

Note 1: OSC2 pin function is determined by the Primary Oscillator mode selection (FPR<3:0>).

2: Note that OSC1 pin cannot be used as an I/O pin, even if the secondary oscillator or an internal clock source is selected at all times.

3: In these Oscillator modes, a crystal is connected between the OSC1 and OSC2 pins.

4: This is the default Oscillator mode for an unprogrammed (erased) device. An unprogrammed Configuration bit has a value of '1'.

5: XTL – XTL Crystal Oscillator mode (200 kHz-4 MHz crystal).

6: XT – XT Crystal Oscillator mode (4 MHz-10 MHz crystal).

7: HS – HS Crystal Oscillator mode (10 MHz-25 MHz crystal).

Register 7-3: FOSC: Oscillator Configuration Register for Oscillator System VERSION 3

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
R/P	R/P	U	U	U	R/P	R/P	R/P
FCKSM<1:0>		—	—	—	FOS<2:0>		
bit 15							bit 8

Lower Byte:							
U	U	U	R/P	R/P	R/P	R/P	R/P
—	—	—	FPR<4:0>				
bit 7							bit 0

bit 23-16 **Unimplemented:** Read as '0'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **FOS<2:0>:** Oscillator Group Selection on POR bit
111 = PLL Oscillator; PLL source selected by FPR<4:0> bits
011 = EXT: External Oscillator; OSC1/OSC2 pins; external oscillator configuration selected by FPR<4:0> bits
010 = LPRC: Internal Low-Power RC
001 = FRC: Internal Fast RC
000 = LPOSC: Low-Power Crystal Oscillator; SOSCI/SOSCO pins

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **FPR<4:0>:** Oscillator Selection within Primary Group bits (see Table 7-4)

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'

Table 7-4: Oscillator System VERSION 3: Configuration Bit Values for Clock Selection

Oscillator Mode	Oscillator Source	FOS<2:0>			FPR<4:0>					OSC2 Pin Function
ECIO w/PLL 4x	PLL	1	1	1	0	1	1	0	1	I/O
ECIO w/PLL 8x	PLL	1	1	1	0	1	1	1	0	I/O
ECIO w/PLL 16x	PLL	1	1	1	0	1	1	1	1	I/O
FRC w/PLL 4x	PLL	1	1	1	0	0	0	0	1	I/O
FRC w/PLL 8x	PLL	1	1	1	0	1	0	1	0	I/O
FRC w/PLL 16x	PLL	1	1	1	0	0	0	1	1	I/O
XT w/PLL 4x	PLL	1	1	1	0	0	1	0	1	**(Note 3)**
XT w/PLL 8x	PLL	1	1	1	0	0	1	1	0	**(Note 3)**
XT w/PLL 16x	PLL	1	1	1	0	0	1	1	1	**(Note 3)**
HS2 w/PLL 4x	PLL	1	1	1	1	0	0	0	1	**(Note 3)**
HS2 w/PLL 8x	PLL	1	1	1	1	0	0	1	0	**(Note 3)**
HS2 w/PLL 16x	PLL	1	1	1	1	0	0	1	1	**(Note 3)**
HS3 w/PLL 4x	PLL	1	1	1	1	0	1	0	1	**(Note 3)**
HS3 w/PLL 8x	PLL	1	1	1	1	0	1	1	0	**(Note 3)**
HS3 w/PLL 16x	PLL	1	1	1	1	0	1	1	1	**(Note 3)**
ECIO	External	0	1	1	0	1	1	0	0	I/O
XT	External	0	1	1	0	0	1	0	0	**(Note 3)**
HS	External	0	1	1	0	0	0	1	0	**(Note 3)**
EC	External	0	1	1	0	1	0	1	1	CLKOUT
ERC	External	0	1	1	0	1	0	0	1	CLKOUT
ERCIO	External	0	1	1	0	1	0	0	0	I/O
XTL	External	0	1	1	0	0	0	0	0	**(Note 3)**
LP	Secondary	0	0	0	x	x	x	x	x	**(Note 1, 2)**
FRC	Internal FRC	0	0	1	x	x	x	x	x	**(Note 1, 2)**
LPRC	Internal LPRC	0	1	0	x	x	x	x	x	**(Note 1, 2)**

Note 1: OSC2 pin function is determined by (FPR<4:0>).

2: OSC1 pin cannot be used as an I/O pin even if the secondary oscillator or an internal clock source is selected at all times.

3: In these Oscillator modes, a crystal is connected between the OSC1 and OSC2 pins.

4: XTL – XTL Crystal Oscillator mode (200 kHz-4 MHz crystal).

5: XT – XT Crystal Oscillator mode (4 MHz-10 MHz crystal).

6: HS – HS Crystal Oscillator mode (10 MHz-25 MHz crystal).

7.4 Oscillator Control Registers – OSCCON and OSCTUN

Run-time control and status of the oscillator system is provided to the user via Special Function Registers. Table 7-5 summarizes the run-time control features provided in VERSION 1, VERSION 2 and VERSION 3 of the oscillator system. Refer to the device data sheet to determine the version of the oscillator system featured on the dsPIC30F device you are using.

Table 7-5: Oscillator Control SFRs

Oscillator System	Oscillator Control SFRs Feature Summary
VERSION 1	Control via OSCCON SFR. Refer to Register 7-4.
VERSION 2	Control via OSCCON SFR. User may tune the FRC oscillator via TUN<3:0> bits in OSCCON. Refer to Register 7-5.
VERSION 3	Control via OSCCON and OSCTUN SFRs. User may tune the FRC oscillator via TUN<3:0> bits in OSCTUN. Refer to Register 7-6 and Register 7-7.

The OSCCON Control register provides control of clock switching and clock source status information.

The COSC status bits in OSCCON are read-only bits that indicate the oscillator source that the device is operating from. The COSC bits are set to the FOS Configuration bit values at a Power-on Reset and will change to indicate the new oscillator source at the end of a clock switch operation.

The NOSC status bits in OSCCON are control bits that select the new clock source for a clock switch operation. The NOSC bits are set to the FOS Configuration bit values at a Power-on Reset or Brown-out Reset and are modified by the user software during a clock switch operation.

The POST<1:0> control bits (OSCCON<8:7>) control the system clock divide ratio.

The LOCK status bit (OSCCON<5>) is read-only and indicates the status of the PLL circuit.

The CF status bit (OSCCON<3>) is a readable/writable status bit that indicates a clock failure.

The LPOSCEN control bit (OSCCON<1>) is used to enable or disable the 32 kHz low-power crystal oscillator.

The OSWEN control bit (OSCCON<0>) is used to initiate a clock switch operation. The OSWEN bit is cleared automatically after a successful clock switch.

The TUN<3:0> bits allow the user to tune the internal FRC oscillator to frequencies higher and lower than the nominal value of 7.37 MHz.

Note: The OSCCON register is write-protected because it controls the device clock switching mechanism. See **Section 7.4.1 "Protection Against Accidental Writes to OSCCON"** for instructions on writing to OSCCON.

7.4.1 Protection Against Accidental Writes to OSCCON

A write to the OSCCON register is intentionally made difficult, because it controls clock switching and clock scaling.

To write to the OSCCON low byte, the following code sequence must be executed without any other instructions in between:

```
Byte Write 0x46 to OSCCONL
Byte Write 0x57 to OSCCONL
```

After this sequence, a byte write to OSCCONL is allowed for one instruction cycle. Write the desired value or use a bit manipulation instruction.

To write to the OSCCON high byte, the following instructions must be executed without any other instructions in between:

```
Byte Write 0x78 to OSCCONH
Byte Write 0x9A to OSCCONH
```

After this sequence, a byte write is allowed to OSCCONH for one instruction cycle. Write the desired value or use a bit manipulation instruction.

Register 7-4: OSCCON: Oscillator Control Register – Oscillator System VERSION 1

Upper Byte:							
U-0	U-0	R-y	R-y	U-0	U-0	R/W-y	R/W-y
—	—	COSC<1:0>		—	—	NOSC<1:0>	
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	R/W-0	R/W-0
POST<1:0>		LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **COSC<1:0>:** Current Oscillator Source Status bits
11 = Primary oscillator
10 = Internal LPRC oscillator
01 = Internal FRC oscillator
00 = Low-power 32 kHz crystal oscillator (Timer1)

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **NOSC<1:0>:** New Oscillator Group Selection bits
11 = Primary oscillator
10 = Internal LPRC oscillator
01 = Internal FRC oscillator
00 = Low-power 32 kHz crystal oscillator (Timer1)

bit 7-6 **POST<1:0>:** Oscillator Postscaler Selection bits
11 = Oscillator postscaler divides clock by 64
10 = Oscillator postscaler divides clock by 16
01 = Oscillator postscaler divides clock by 4
00 = Oscillator postscaler does not alter clock

bit 5 **LOCK:** PLL Lock Status bit
1 = Indicates that PLL is in lock
0 = Indicates that PLL is out of lock (or disabled)
Reset on POR or BOR. Reset when a valid clock switching sequence is initiated. Set when PLL lock is achieved after a PLL start. Reset when lock is lost. Read zero when PLL is not selected as a system clock.

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Status bit
1 = FSCM has detected a clock failure
0 = FSCM has not detected a clock failure
Reset on POR or BOR. Reset when a valid clock switching sequence is initiated. Set when clock fail detected.

bit 2 **Unimplemented:** Read as '0'

bit 1 **LPOSCEN:** 32 kHz LP Oscillator Enable bit
1 = LP oscillator is enabled
0 = LP oscillator is disabled
Reset on POR or BOR

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Request oscillator switch to selection specified by NOSC<1:0> bits
0 = Oscillator switch is complete

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
y = Value set from Configuration bits on POR or BOR			

Register 7-5: OSCCON: Oscillator Control Register – Oscillator System VERSION 2

Upper Byte:							
R/W-0	R/W-0	R-y	R-y	R/W-0	R/W-0	R/W-y	R/W-y
TUN3	TUN2	COSC<1:0>		TUN1	TUN0	NOSC<1:0>	
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	R/W-0	R/W-0
POST<1:0>		LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

bit 15-14 **TUN<3:2>:** Upper 2 bits of the TUN bit field
Refer to the description of TUN<1:0> (OSCCON<11:10>) bits for details.

bit 13-12 **COSC<1:0>:** Current Oscillator Source Status bits
11 = Primary oscillator
10 = Internal LPRC oscillator
01 = Internal FRC oscillator
00 = Low-power 32 kHz crystal oscillator (Timer1)

bit 11-10 **TUN<1:0>:** Lower 2 bits of the TUN bit field
The four-bit field specified by TUN<3:0> allows the user to tune the internal fast RC oscillator which has a nominal frequency of 7.37 MHz. For example, the user may be able to tune the frequency of the FRC oscillator within a range of +/-12% (or 960 kHz) in steps of 1.5% around the factory calibrated frequency setting, as follows:
TUN<3:0> = 0111 provides the highest frequency
•
•
•
TUN<3:0> = 0000 provides the factory calibrated frequency
•
•
•
TUN<3:0> = 1000 provides the lowest frequency

Note: Refer to the device-specific data sheet for the exact tuning range and tuning step size for the FRC oscillator on your device.

bit 9-8 **NOSC<1:0>:** New Oscillator Group Selection bits
11 = Primary oscillator
10 = Internal LPRC oscillator
01 = Internal FRC oscillator
00 = Low-power 32 kHz crystal oscillator (Timer1)

bit 7-6 **POST<1:0>:** Oscillator Postscaler Selection bits
11 = Oscillator postscaler divides clock by 64
10 = Oscillator postscaler divides clock by 16
01 = Oscillator postscaler divides clock by 4
00 = Oscillator postscaler does not alter clock

bit 5 **LOCK:** PLL Lock Status bit
1 = Indicates that PLL is in lock
0 = Indicates that PLL is out of lock (or disabled)
Reset on POR or BOR. Reset when a valid clock switching sequence is initiated. Set when PLL lock is achieved after a PLL start. Reset when lock is lost. Read zero when PLL is not selected as a system clock.

bit 4 **Unimplemented:** Read as '0'

Register 7-5: OSCCON: Oscillator Control Register – Oscillator System VERSION 2 (Continued)

bit 3 **CF:** Clock Fail Status bit
1 = FSCM has detected a clock failure
0 = FSCM has not detected a clock failure
Reset on POR or BOR. Reset when a valid clock switching sequence is initiated. Set when clock fail detected.

bit 2 **Unimplemented:** Read as '0'

bit 1 **LPOSCEN:** 32 kHz LP Oscillator Enable bit
1 = LP oscillator is enabled
0 = LP oscillator is disabled
Reset on POR or BOR.

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Request oscillator switch to selection specified by NOSC<1:0> bits
0 = Oscillator switch is complete

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
y = Value set from Configuration bits on POR or BOR			

Register 7-6: OSCCON: Oscillator Control Register – Oscillator System VERSION 3

Upper Byte:							
U-0	R-y	R-y	R-y	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0>		
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	R/W-0	R/W-0
POST<1:0>		LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Group Selection bits (read-only)
111 = PLL oscillator; PLL source selected by FPR<4:0> bits
011 = External oscillator; OSC1/OSC2 pins; external oscillator configuration selected by FPR<4:0> bits
010 = LPRC internal low-power RC
001 = FRC internal fast RC
000 = LP crystal oscillator; SOSCI/SOSCO pins
Set to FOS<2:0> values on POR or BOR. Loaded with NOSC<2:0> at the completion of a successful clock switch. Set to FRC value when FSCM detects a failure and switches clock to FRC.

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Group Selection bits
111 = PLL oscillator; PLL source selected by FPR<4:0> bits
011 = External oscillator; OSC1/OSC2 pins; external oscillator configuration selected by FPR<4:0> bits
010 = LPRC internal low-power RC
001 = FRC internal fast RC
000 = LP crystal oscillator; SOSCI/SOSCO pins
Set to FOS<2:0> values on POR or BOR.

bit 7-6 **POST<1:0>:** Oscillator Postscaler Selection bits
11 = Oscillator postscaler divides clock by 64
10 = Oscillator postscaler divides clock by 16
01 = Oscillator postscaler divides clock by 4
00 = Oscillator postscaler does not alter clock

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock
0 = Indicates that PLL is out of lock (or disabled)
Reset on POR or BOR. Reset when a valid clock switching sequence is initiated. Set when PLL lock is achieved after a PLL start. Reset when lock is lost. Read zero when PLL is not selected as a system clock.

bit 4 **Unimplemented:** Read as '0'

OSCCON: Oscillator Control Register – Oscillator System VERSION 3 (Continued)

bit 3 **CF:** Clock Fail Detect bit (read/clearable by application)
1 = FSCM has detected clock failure
0 = FSCM has NOT detected clock failure
Reset on POR or BOR. Reset when a valid clock switching sequence is initiated. Set when clock fail detected.

bit 2 **Unimplemented:** Read as '0'

bit 1 **LPOSCEN:** 32 kHz Secondary (LP) Oscillator Enable bit
1 = Secondary oscillator is enabled
0 = Secondary oscillator is disabled
Reset on POR or BOR.

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Request oscillator switch to selection specified by NOSC<2:0> bits
0 = Oscillator switch is complete
Reset on POR or BOR. Reset after a successful clock switch. Reset after a redundant clock switch (i.e., a clock switch operation is requested to the current oscillator). Reset after FSCM switches the oscillator to (Group 1) FRC.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
y = Value set from Configuration bits on POR			

Register 7-7: OSCTUN: FRC Oscillator Tuning Register – Oscillator System VERSION 3 Only

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	TUN<3:0>(1,2)			
bit 7							bit 0

bit 15-4 **Unimplemented:** Read as '0'

bit 3-0 **TUN<3:0>:** The four-bit field specified by TUN<3:0> allows the user to tune the internal fast RC oscillator which has a nominal frequency of 7.37 MHz(1,2).

TUN<3:0> = 0111 provides the highest frequency

•
•
•

TUN<3:0> = 0000 provides the factory calibrated frequency

•
•
•

TUN<3:0> = 1000 provides the lowest frequency

Note 1: Refer to the device-specific data sheet for the exact tuning range and tuning step size for the FRC oscillator on your device.

2: Certain devices may have more than four TUN bits. Refer to the device-specific data sheet to identify the number of TUN bits available to the user for tuning the FRC oscillator.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
y = Value set from Configuration bits on POR			

7.5 Primary Oscillator

The primary oscillator is available on the OSC1 and OSC2 pins of the dsPIC30F device family. The primary oscillator has a wide variety of operation modes summarized in Table 7-6. In general, the primary oscillator can be configured for an external clock input, external RC network or an external crystal. Further details of the Primary Oscillator Operating modes are described in subsequent sections.

The FPR bits in the FOSC nonvolatile Configuration register select the operating mode of the primary oscillator.

Table 7-6:Primary Oscillator Operating Modes

Oscillator Mode(4)	Description
XTL	200 kHz-4 MHz crystal on OSC1:OSC2.
XT	4 MHz-10 MHz crystal on OSC1:OSC2.
XT w/PLL 4x	4 MHz-10 MHz crystal on OSC1:OSC2, 4x PLL enabled.
XT w/PLL 8x	4 MHz-10 MHz crystal on OSC1:OSC2, 8x PLL enabled.
XT w/PLL 16x	4 MHz-10 MHz crystal on OSC1:OSC2, 16x PLL enabled(1).
LP	32 kHz crystal on SOSCO:SOSCI(2).
HS	10 MHz-25 MHz crystal.
HS/2 w/PLL 4x	10 MHz -25 MHz crystal, divide by 2, 4x PLL enabled.
HS/2 w/PLL 8x	10 MHz-25MHz crystal, divide by 2, 8x PLL enabled.
HS/2 w/PLL 16x	10 MHz-25MHz crystal, divide by 2, 16x PLL enabled(1).
HS/3 w/PLL 4x	10 MHz-25 MHz crystal, divide by 3, 4x PLL enabled.
HS/3 w/PLL 8x	10 MHz-25MHz crystal, divide by 3, 8x PLL enabled.
HS/3 w/PLL 16x	10 MHz-25MHz crystal, divide by 3, 16x PLL enabled(1).
EC	External clock input (0-40 MHz).
ECIO	External clock input (0-40 MHz), OSC2 pin is I/O.
EC w/PLL 4x	External clock input (4-10 MHz), OSC2 pin is I/O, 4x PLL enabled(1).
EC w/PLL 8x	External clock input (4-10 MHz), OSC2 pin is I/O, 8x PLL enabled(1).
EC w/PLL 16x	External clock input (4-10 MHz), OSC2 pin is I/O, 16x PLL enabled(1).
ERC	External RC oscillator, OSC2 pin is FOSC/4 output(3).
ERCIO	External RC oscillator, OSC2 pin is I/O(3).
FRC	7.37 MHz internal fast RC oscillator.
FRC w/PLL 4x	7.37 MHz internal fast RC oscillator, 4x PLL enabled.
FRC w/PLL 8x	7.37 MHz internal fast RC oscillator, 8x PLL enabled.
FRC w/PLL 16x	7.37 MHz internal fast RC oscillator, 16x PLL enabled.
LPRC	512 kHz internal low-power RC oscillator.

Note 1: dsPIC30F maximum operating frequency of 120 MHz must be met.
2: LP oscillator can be conveniently shared as system clock, as well as real-time clock for Timer1.
3: Requires external R and C. Frequency operation up to 4 MHz.
4: This table lists a cumulative set of operating modes featured in oscillator system VERSION 1, VERSION 2 and VERSION 3.

7.5.1 Oscillator Mode Selection Guidelines

The main difference between the XT, XTL and HS modes is the gain of the internal inverter of the oscillator circuit, which allows the different frequency ranges. In general, use the oscillator option with the lowest possible gain that still meets specifications. This will result in lower dynamic currents (IDD). The frequency range of each Oscillator mode is the recommended frequency cutoff, but the selection of a different Gain mode is acceptable as long as a thorough validation is performed (voltage, temperature and component variations, such as resistor, capacitor and internal oscillator circuitry).

The oscillator feedback circuit is disabled in all EC and ECIO modes. The OSC1 pin is a high-impedance input and can be driven by a CMOS driver.

The ERC and ERCIO modes provide the least expensive solution for device oscillation (only an external resistor and capacitor is required). These modes also provide the most variation in the oscillation frequency.

If the primary oscillator is configured for an external clock input or an external RC network, the OSC2 pin is not required to support the oscillator function. For these modes, the OSC2 pin can be used as an additional device I/O pin or a clock output pin. When the OSC2 pin is used as a clock output pin, the output frequency is FOSC/4.

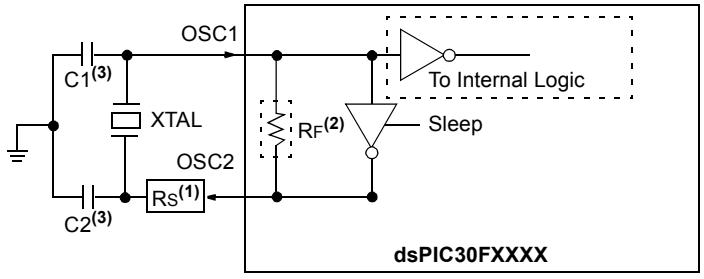
The XTL mode is a Low-Power/Low-Frequency mode. This mode of the oscillator consumes the least amount of power of the three Crystal modes. The XT mode is a Medium Power/Medium Frequency mode and HS mode provides the highest oscillator frequencies with a crystal.

The EC and XT modes that use the PLL circuit provide the highest device operating frequencies. The oscillator circuit will consume the most current in these modes because the PLL is enabled to multiply the frequency of the oscillator.

7.6 Crystal Oscillators/Ceramic Resonators

In XT, XTL and HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 7-3). The dsPIC30F oscillator design requires the use of a parallel cut crystal. Using a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

Figure 7-3: Crystal or Ceramic Resonator Operation (XT, XTL or HS Oscillator Mode)



Note 1: A series resistor, Rs, may be required for AT strip cut crystals.
2: The internal feedback resistor, RF, is typically in the range of 2 to 10 MΩ.
3: See **Section 7.7 "Determining Best Values for Crystals, Clock Mode, C1, C2 and Rs"**.

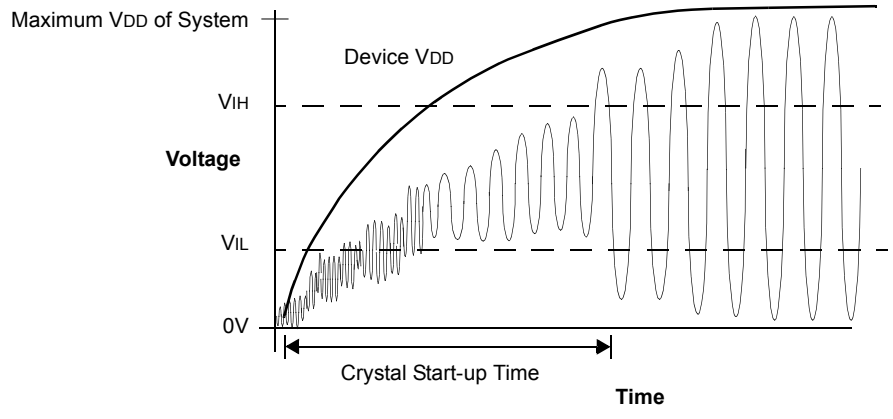
7.6.1 Oscillator/Resonator Start-up

As the device voltage increases from VSS, the oscillator will start its oscillations.The time required for the oscillator to start oscillating depends on many factors. These include:

- Crystal/resonator frequency
- Capacitor values used (C1 and C2 in Figure 7-3)
- Device VDD rise time
- System temperature
- Series resistor value and type if used (Rs in Figure 7-3)
- Oscillator mode selection of device (selects the gain of the internal oscillator inverter)
- Crystal quality
- Oscillator circuit layout
- System noise

Figure 7-4 shows a plot of a typical oscillator/resonator start-up.

Figure 7-4: Example Oscillator/Resonator Start-up Characteristics



7.6.2 Tuning the Oscillator Circuit

Since Microchip devices have wide operating ranges (frequency, voltage and temperature; depending on the part and version ordered) and external components (crystals, capacitors,...) of varying quality and manufacture, validation of operation needs to be performed to ensure that the component selection will comply with the requirements of the application.

There are many factors that go into the selection and arrangement of these external components. These factors include:

- Amplifier gain
- Desired frequency
- Resonant frequency(s) of the crystal
- Temperature of operation
- Supply voltage range
- Start-up time
- Stability
- Crystal life
- Power consumption
- Simplification of the circuit
- Use of standard components
- Component count

7.6.3 Oscillator Start-up from Sleep Mode

The most difficult time for the oscillator to start-up is when waking up from Sleep mode. This is because the load capacitors have both partially charged to some quiescent value, and phase differential at wake-up is minimal. Thus, more time is required to achieve stable oscillation. Remember also that low voltage, high temperatures and the Lower Frequency Clock modes also impose limitations on loop gain, which in turn affects start-up. Each of the following factors increases the start-up time:

- Low-frequency design (with a Low Gain Clock mode)
- Quiet environment (such as a battery operated device)
- Operating in a shielded box (away from the noisy RF area)
- Low voltage
- High temperature
- Wake-up from Sleep mode

Noise actually helps lower the oscillator start-up time since it provides a “kick start” to the oscillator.

Prior to entering Sleep mode, the application may switch to the Internal FRC(+PLL) oscillator in order to reduce the time taken by the device to wake-up from Sleep.

7.7 Determining Best Values for Crystals, Clock Mode, C1, C2 and Rs

The best method for selecting components is to apply a little knowledge and a lot of trial, measurement and testing.

Crystals are usually selected by their parallel resonant frequency only, however, other parameters may be important to your design, such as temperature or frequency tolerance. Application note *AN588* "*PICmicro® Microcontroller Oscillator Design Guide*", is an excellent reference to learn more about crystal operation and their ordering information.

The dsPIC30F internal oscillator circuit is a parallel oscillator circuit, which requires that a parallel resonant crystal be selected. The load capacitance is usually specified in the 22 pF to 33 pF range. The crystal will oscillate closest to the desired frequency with a load capacitance in this range. It may be necessary to alter these values, as described later, in order to achieve other benefits.

The Clock mode is primarily chosen based on the desired frequency of the crystal oscillator. The main difference between the XT, XTL and HS Oscillator modes is the gain of the internal inverter of the oscillator circuit, which allows the different frequency ranges. In general, use the oscillator option with the lowest possible gain that still meets specifications. This will result in lower dynamic currents (I_{DD}). The frequency range of each Oscillator mode is the recommended frequency cutoff, but the selection of a different Gain mode is acceptable, as long as a thorough validation is performed (voltage, temperature and component variations, such as resistor, capacitor and internal oscillator circuitry).

C1 and C2 (see Figure 7-3) should also be initially selected based on the load capacitance as suggested by the crystal manufacturer and the tables supplied in the device data sheet. The values given in the device data sheet can only be used as a starting point since the crystal manufacturer, supply voltage, and other factors already mentioned may cause your circuit to differ from the one used in the factory characterization process.

Ideally, the capacitance is chosen so that it will oscillate at the highest temperature and the lowest V_{DD} that the circuit will be expected to perform under. High temperature and low V_{DD} both have a limiting effect on the loop gain, such that if the circuit functions at these extremes, the designer can be more assured of proper operation at other temperatures and supply voltage combinations. The output sine wave should not be clipped in the highest gain environment (highest V_{DD} and lowest temperature) and the sine output amplitude should be large enough in the lowest gain environment (lowest V_{DD} and highest temperature) to cover the logic input requirements of the clock as listed in the device data sheet.

A method for improving start-up is to use a value of C2 greater than C1. This causes a greater phase shift across the crystal at power-up, which speeds oscillator start-up.

Besides loading the crystal for proper frequency response, these capacitors can have the effect of lowering loop gain if their value is increased. C2 can be selected to affect the overall gain of the circuit. A higher C2 can lower the gain if the crystal is being over driven (also, see discussion on Rs). Capacitance values that are too high can store and dump too much current through the crystal, so C1 and C2 should not become excessively large. Unfortunately, measuring the wattage through a crystal is difficult, but if you do not stray too far from the suggested values, you should not have to be concerned with this.

A series resistor, Rs, is added to the circuit if, after all other external components are selected to satisfaction, the crystal is still being overdriven. This can be determined by looking at the OSC2 pin, which is the driven pin, with an oscilloscope. Connecting the probe to the OSC1 pin will load the pin too much and negatively affect performance. Remember that a scope probe adds its own capacitance to the circuit, so this may have to be accounted for in your design (i.e., if the circuit worked best with a C2 of 22 pF and the scope probe was 10 pF, a 33 pF capacitor may actually be called for). The output signal should not be clipping or flattened. Overdriving the crystal can also lead to the circuit jumping to a higher harmonic level or even crystal damage.

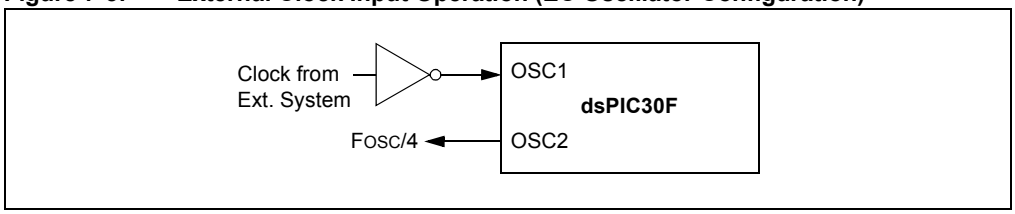
The OSC2 signal should be a clean sine wave that easily spans the input minimum and maximum of the clock input pin (4V to 5V peak-to-peak for a 5V VDD is usually good). An easy way to set this is to again test the circuit at the minimum temperature and maximum VDD that the design will be expected to perform in, then look at the output. This should be the maximum amplitude of the clock output. If there is clipping or the sine wave is distorted near VDD and VSS, increasing load capacitors may cause too much current to flow through the crystal or push the value too far from the manufacturer's load specification. To adjust the crystal current, add a trimmer potentiometer between the crystal inverter output pin and C2 and adjust it until the sine wave is clean. The crystal will experience the highest drive currents at the low temperature and high VDD extremes. The trimmer potentiometer should be adjusted at these limits to prevent overdriving. A series resistor, Rs, of the closest standard value can now be inserted in place of the trimpot. If Rs is too high, perhaps more than 20 kOhms, the input will be too isolated from the output, making the clock more susceptible to noise. If you find a value this high is needed to prevent overdriving the crystal, try increasing C2 to compensate or changing the Oscillator Operating mode. Try to get a combination where Rs is around 10k or less and load capacitance is not too far from the manufacturer specification.

7.8 External Clock Input

Two of the Primary Oscillator modes use an external clock. These modes are EC and ECIO.

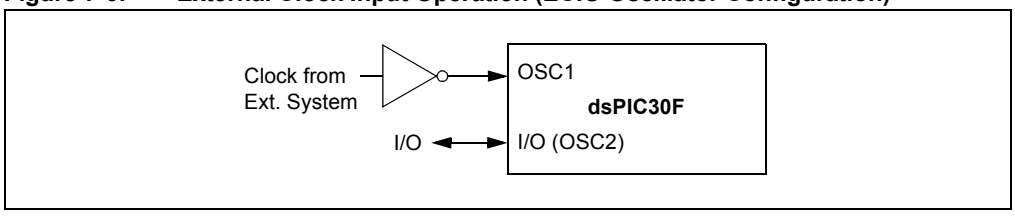
In the EC mode (Figure 7-5), the OSC1 pin can be driven by CMOS drivers. In this mode, the OSC1 pin is high-impedance and the OSC2 pin is the clock output (FOSC/4). This output clock is useful for testing or synchronization purposes.

Figure 7-5: External Clock Input Operation (EC Oscillator Configuration)



In the ECIO mode (Figure 7-6), the OSC1 pin can be driven by CMOS drivers. In this mode, the OSC1 pin is high-impedance and the OSC2 pin becomes a general purpose I/O pin. The feedback device between OSC1 and OSC2 is turned off to save current.

Figure 7-6: External Clock Input Operation (ECIO Oscillator Configuration)



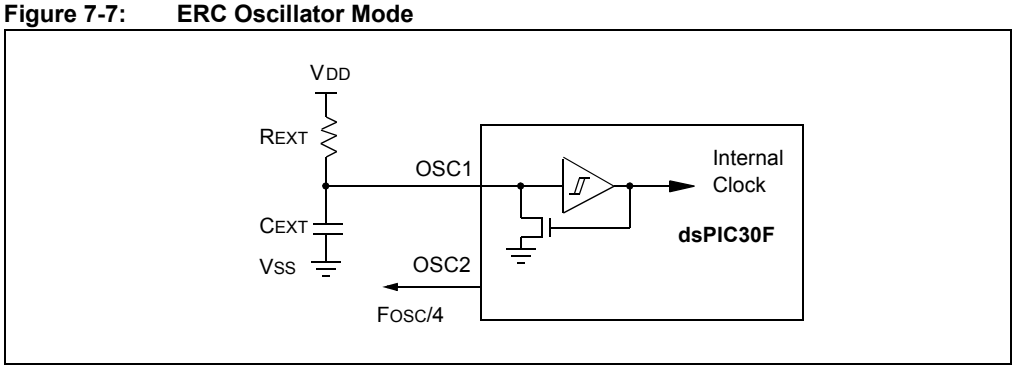
7.9 External RC Oscillator

For timing insensitive applications, the ERC and ERCIO modes of the primary oscillator offer additional cost savings. The RC oscillator frequency is a function of the:

- Supply voltage
- External resistor (REXT) values
- External capacitor (CEXT) values
- Operating temperature

In addition to this, the oscillator frequency will vary from unit-to-unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external REXT and CEXT components used. Figure 7-7 shows how the RC combination is connected. For REXT values below 2.2 kΩ, oscillator operation may become unstable or stop completely. For very high REXT values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, it is recommended that a REXT value between 3 kΩ and 100 kΩ is used.

Figure 7-7: ERC Oscillator Mode



Although the oscillator will operate with no external capacitor (CEXT = 0 pF), a value above 20 pF should be used for noise and stability reasons. With no or a small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance and package lead frame capacitance.

The oscillator frequency, divided by 4, is available on the OSC2/CLKO pin, and can be used for test purposes or to synchronize other logic.

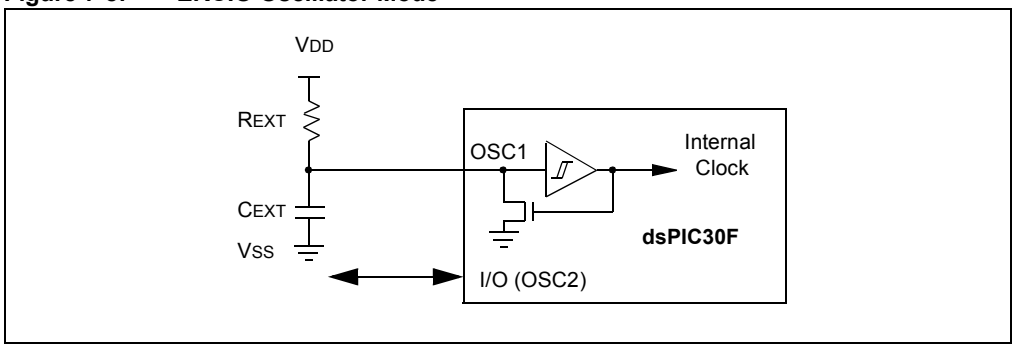
Note:	An external clock source should not be connected to the OSC1 pin when the oscillator is configured for ERC or ERCIO modes.

7.9.1 External RC Oscillator with I/O Enabled

The ERCIO Oscillator mode functions in the exact same manner as the ERC Oscillator mode. The only difference is that the OSC2 pin is configured as an I/O pin.

As in the RC mode, the user needs to take into account any variation of the clock frequency due to tolerance of external REXT and CEXT components used, process variation, voltage and temperature. Figure 7-8 shows how the RC with the I/O pin combination is connected.

Figure 7-8: ERCIO Oscillator Mode



7.9.2 External RC Start-up

There is no start-up delay associated with the RC oscillator. Oscillation will begin when VDD is applied.

Note:	The user should verify that VDD is within specifications before the device begins to execute code.

7.9.3 RC Operating Frequency

The following graphs show the external RC oscillator frequency as a function of device voltage for a selection of RC component values.

Note:	The following graphs should be used only as approximate guidelines for RC component selection. The actual frequency will vary based on the system temperature and device. Please refer to the specific device data sheet for further RC oscillator characteristic data.

Figure 7-9: Typical External RC Oscillator Frequency vs. VDD, CEXT = 20 pF

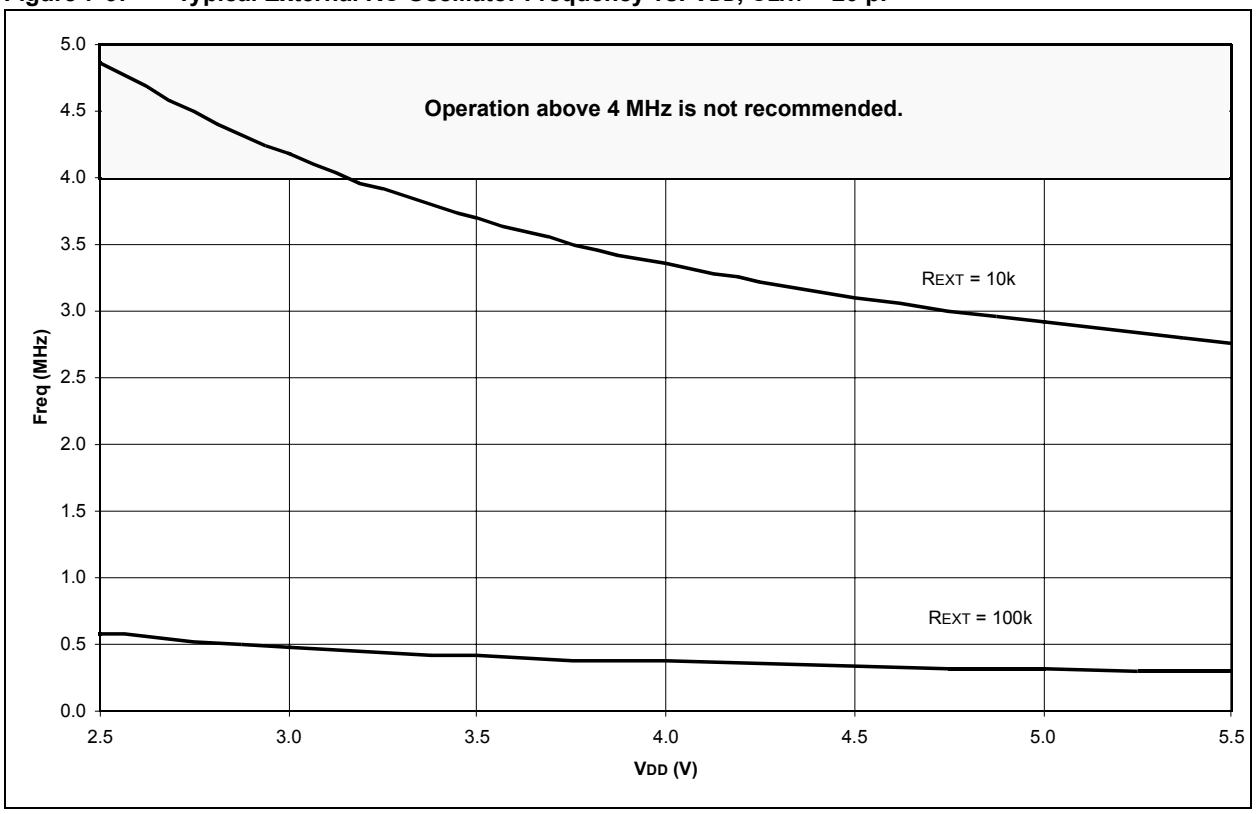


Figure 7-10: Typical External RC Oscillator Frequency vs. VDD, CEXT = 100 pF

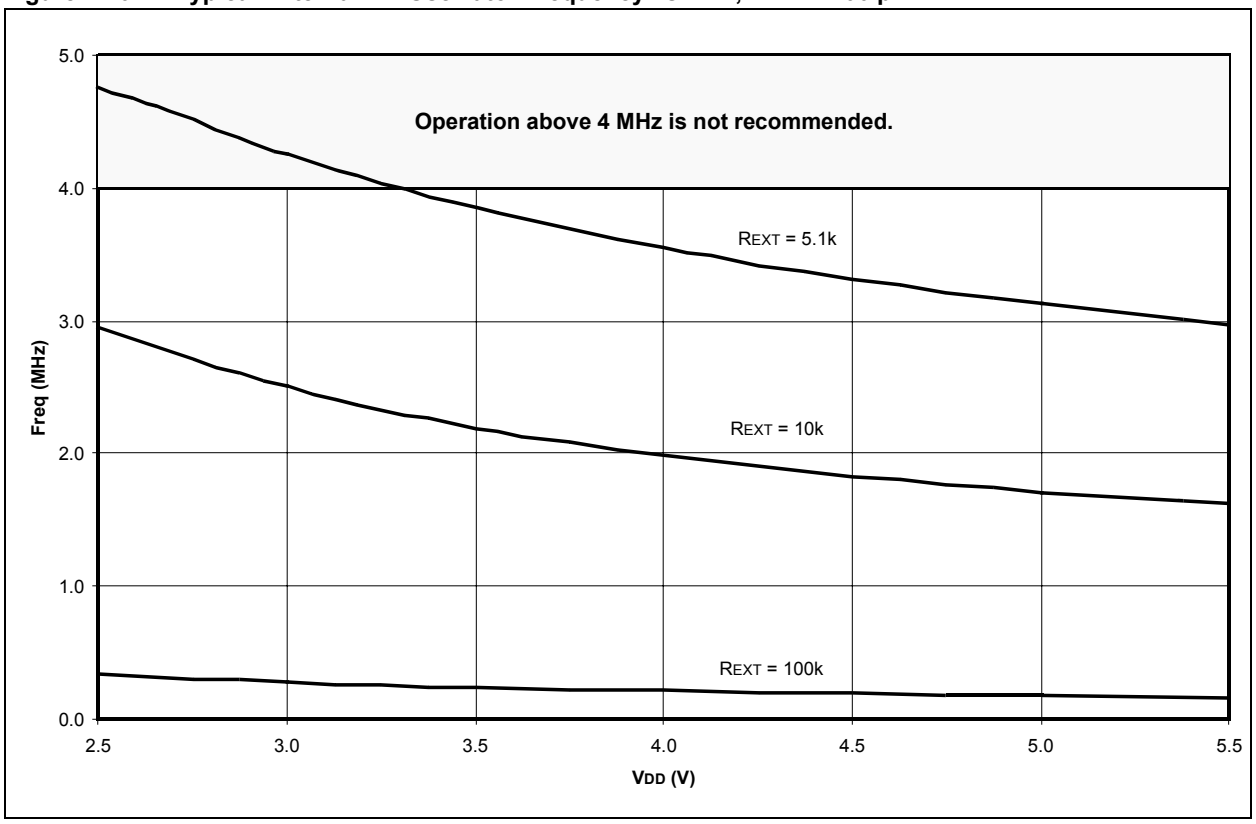
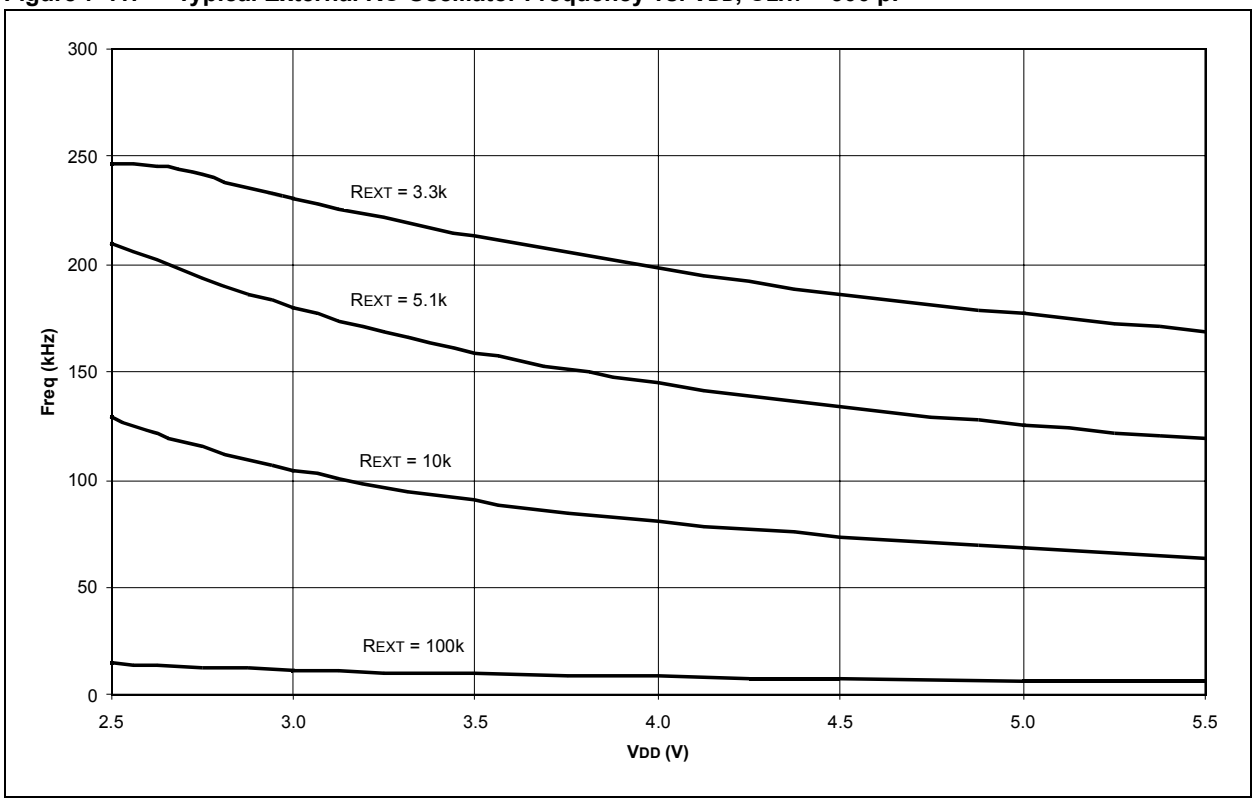


Figure 7-11: Typical External RC Oscillator Frequency vs. VDD, CEXT = 300 pF



7.10 Phase Locked Loop (PLL)

The PLL can be enabled for x4, x8 or x16 Operation modes using the FPR<3:0> oscillator Configuration bits. The input and output frequency ranges for each Operating mode are summarized in Table 7-7.

Note:	Some PLL output frequency ranges can be achieved that exceed the maximum operating frequency of the dsPIC30F device. Refer to the "Electrical Specifications" in the specific device data sheet for further details.

Table 7-7: PLL Frequency Range

FIN	PLL Multiplier	FOUT
4 MHz-10 MHz	x4	16 MHz-40 MHz
4 MHz-10 MHz	x8	32 MHz-80 MHz
4 MHz-7.5 MHz	x16	64 MHz-120 MHz

7.10.1 PLL Lock Status

The PLL circuit is able to detect when the PLL enters a phase locked state. It can also detect when the PLL loses lock. The time delay for the PLL to achieve lock is designated as TLOCK. The TLOCK value is nominally 20 μs. Refer to the "Electrical Specifications" in the specific device data sheet for further information.

The LOCK bit is a read-only Status bit (OSCCON<5>) that reflects the LOCK status of the PLL. The LOCK bit is cleared at a Power-on Reset.

7.10.1.1 Loss of PLL Lock During Clock Switching

When the PLL is selected as a destination clock source in a clock switch operation (including a Power-on Reset), the LOCK bit is cleared. The LOCK bit is set after phase lock has been achieved. If the PLL fails to achieve lock, then the clock switching circuit will NOT switch to the PLL output for system clock; instead, it will continue to run with the old clock source.

7.10.1.2 Loss of PLL Lock During a Power-on Reset

If the PLL fails to achieve lock at a Power-on Reset (POR) and the Fail-Safe Clock Monitor (FSCM) is enabled, the FRC oscillator will become the device clock source and a clock failure trap will occur.

7.10.1.3 Loss of PLL Lock During Normal Device Operation

If the PLL loses lock during normal operation for at least 4 input clock cycles, then the LOCK bit is cleared, indicating a loss of PLL lock. Furthermore, a clock failure trap will be generated. *In this situation, the processor continues to run using the PLL clock source.* The user can switch to another clock source in the Trap Service Routine, if desired.

Note:	Refer to **Section 6. "Reset Interrupts"** for further details about oscillator failure traps. A loss of PLL lock during normal device operation will generate a clock failure trap, but the system clock source will not be changed. The FSCM does not need to be enabled to detect the loss of lock.

7.11 Low-Power 32 kHz Crystal Oscillator

The LP or secondary oscillator is designed specifically for low-power operation with a 32 kHz crystal. The LP oscillator is located on the SOSCO and SOSCI device pins and serves as a secondary crystal clock source for low-power operation. The LP oscillator can also drive Timer1 for a real-time clock application.

7.11.1 LP Oscillator Enable

The following control bits affect the operation of the LP oscillator:

1. The COSC<1:0> bits in the OSCCON register (OSCCON<13:12>).
2. The LPOSCEN bit in the OSCCON register (OSCCON<1>).

When the LP oscillator is enabled, the SOSCO and SOSCI I/O pins are controlled by the oscillator and cannot be used for other I/O functions.

7.11.1.1 LP Oscillator Continuous Operation

The LP oscillator will always be enabled if the LPOSCEN control bit (OSCCON<1>) is set. There are two reasons to leave the LP oscillator running. First, keeping the LP oscillator ON at all times allows a fast switch to the 32 kHz system clock for lower power operation. Returning to the faster main oscillator will still require an oscillator start-up time if it is a crystal type source (see **Section 7.12 "Oscillator Start-up Timer (OST)"**). Second, the oscillator should remain ON at all times when using Timer1 as a Real-Time Clock (RTC).

7.11.1.2 LP Oscillator Intermittent Operation

When the LPOSCEN control bit (OSCCON<1>) is cleared, the LP oscillator will only operate when it is selected as the current device clock source (COSC<1:0> = 00). The LP oscillator will be disabled if it is the current device clock source and the device enters Sleep mode.

7.11.2 LP Oscillator Operation with Timer1

The LP oscillator can be used as a clock source for Timer1 in a Real-Time Clock application. Refer to **Section 12. "Timers"** for further details.

7.12 Oscillator Start-up Timer (OST)

In order to ensure that a crystal oscillator (or ceramic resonator) has started and stabilized, an Oscillator Start-up Timer (OST) is provided. It is a simple 10-bit counter that counts 1024 TOSC cycles before releasing the oscillator clock to the rest of the system. The time-out period is designated as TOST. The amplitude of the oscillator signal must reach the VIL and VIH thresholds for the oscillator pins before the OST can begin to count cycles (see Figure 7-4).

The TOST time is involved every time the oscillator has to restart (i.e., on POR, BOR and wake-up from Sleep mode). The Oscillator Start-up Timer is applied to the LP oscillator and the XT, XTL and HS modes for the primary oscillator.

7.13 Internal Fast RC Oscillator (FRC)

The FRC oscillator is a fast (7.37 MHz nominal) internal RC oscillator. This oscillator is intended to provide a range of device operating speeds without the use of an external crystal, ceramic resonator or RC network. Devices featuring the oscillator system VERSIONs 2 or 3 may optionally provide the FRC oscillator as an input frequency to the PLL.

7.14 Internal Low-Power RC (LPRC) Oscillator

The LPRC oscillator is a component of the Watchdog Timer (WDT) and oscillates at a nominal frequency of 512 kHz. The LPRC oscillator is the clock source for the Power-up Timer (PWRT) circuit, WDT and clock monitor circuits. It may also be used to provide a low-frequency clock source option for applications where power consumption is critical, and timing accuracy is not required.

Note:	The oscillation frequency of the LPRC oscillator will vary depending on the device voltage and operating temperature. Refer to the “Electrical Specifications” in the specific device data sheet for further details.

7.14.1 Enabling the LPRC Oscillator

The LPRC oscillator is always enabled at a Power-on Reset because it is the clock source for the PWRT. After the PWRT expires, the LPRC oscillator will remain ON if one of the following is TRUE:

- The Fail-Safe Clock Monitor is enabled.
- The WDT is enabled.
- The LPRC oscillator is selected as the system clock (COSC<1:0> = 10).

If none of the above conditions is true, the LPRC will shut-off after the PWRT expires.

7.15 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming the FCKSM bits (Clock Switch and Monitor bits) in the FOSC device Configuration register. Refer to **Section 7.3 “Oscillator Configuration”** for further details. If the FSCM function is enabled, the LPRC internal oscillator will run at all times (except during Sleep mode).

In the event of an oscillator failure, the FSCM will generate a clock failure trap and will switch the system clock to the FRC oscillator. The user will then have the option to either attempt to restart the oscillator or execute a controlled shutdown.

The FSCM module will take the following actions when switching to the FRC oscillator:

1. The COSC<1:0> bits are loaded with ‘01’.
2. The CF bit is set to indicate the clock failure.
3. The OSWEN control bit is cleared to cancel any pending clock switches.

Note:	For more information about the oscillator failure trap, please refer to **Section 6. “Reset Interrupts”**.

7.15.1 FSCM Delay

On a POR, BOR or wake-up event from Sleep mode, a nominal 100 μs delay (TFSCM) may be inserted before the FSCM begins to monitor the system clock source. The purpose of the FSCM delay is to provide time for the oscillator and/or PLL to stabilize when the Power-up Timer (PWRT) is not utilized. The FSCM delay will be generated after the internal System Reset signal, SYSRST, has been released. Refer to **Section 8. “Reset”** for FSCM delay timing information.

The FSCM delay, TFSCM, is applied when the FSCM is enabled and any of the following device clock sources is selected as the system clock:

- EC+PLL
- XT+PLL
- XT
- HS
- HS/2 or HS/3 + PLL
- XTL
- LP

Note:	Please refer to the “Electrical Specifications” section of the device data sheet for TFSCM specification values.

7.15.2 FSCM and Slow Oscillator Start-up

If the chosen device oscillator has a slow start-up time coming out of POR, BOR or Sleep mode, it is possible that the FSCM delay will expire before the oscillator has started. In this case, the FSCM will initiate a clock failure trap. As this happens, the COSC<1:0> bits (OSCCON<13:12>) are loaded with the FRC oscillator selection. This will effectively shut-off the original oscillator that was trying to start. The user can detect this situation and initiate a clock switch back to the desired oscillator in the Trap Service Routine.

7.15.3 FSCM and WDT

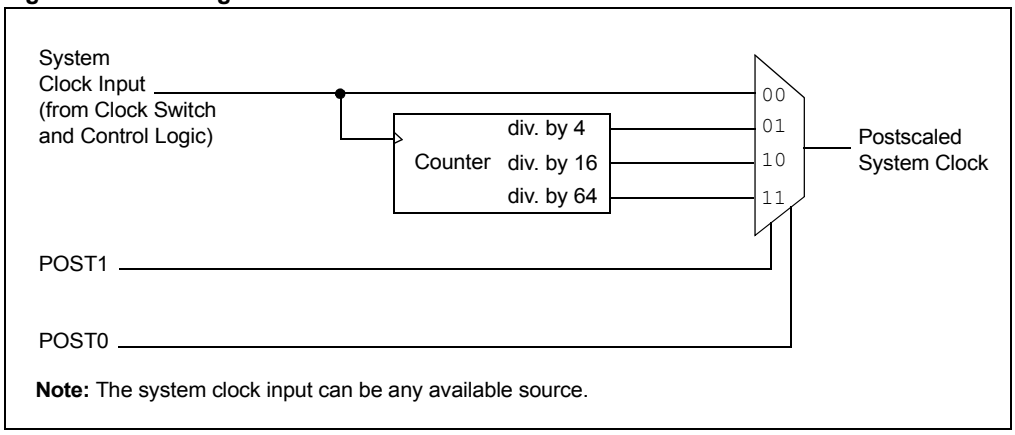
In the event of a clock failure, the WDT is unaffected and continues to run on the LPRC clock.

7.16 Programmable Oscillator Postscaler

The postscaler allows the user to save power by lowering the frequency of the clock which feeds the CPU and the peripherals. Postscale values can be changed at any time via the POST<1:0> control bits (OSCCON<7:6>).

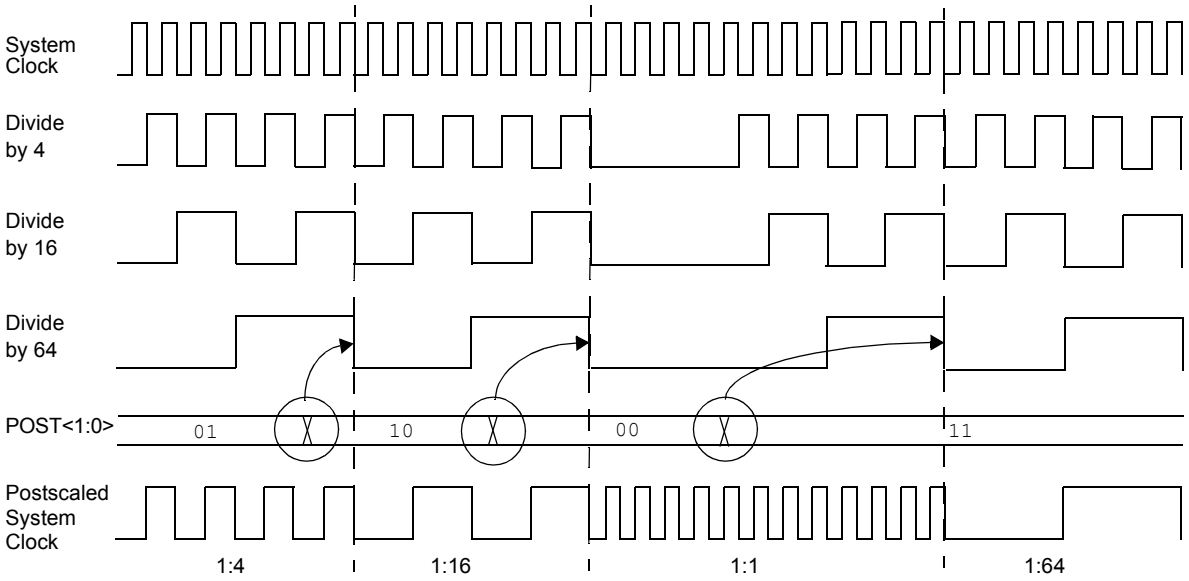
To ensure a clean clock transition, there is some delay before a clock change occurs. The clock postscaler does not change the clock selection multiplexer until a falling edge on the divide-by-64 output occurs. In effect, the switching delay could be up to 64 system clock cycles depending on when the POST<1:0> control bits are written. Figure 7-13 shows the postscaler operation for three different postscaler changes.

Figure 7-12: Programmable Oscillator Postscaler



Note: The system clock input can be any available source.

Figure 7-13: Postscaler Update Timing



Note: This diagram demonstrates the clock postscaler function only. The divide ratios shown in the timing diagram are not correct.

7.17 Clock Switching Operation

The selection of clock sources available for clock switching during device operation are as follows:

- Primary oscillator on OSC1/OSC2 pins
- Low-Power 32 kHz Crystal (Secondary) oscillator on SOSCO/SOSCI pins
- Internal Fast RC (FRC) oscillator
- Internal Low-Power RC (LPRC) oscillator

Note:	The primary oscillator has multiple operating modes (EC, RC, XT, FRC etc.). The operating mode of the primary oscillator is determined by the FPR Configuration bits in the FOSC device Configuration register. (Refer to **7.3 "Oscillator Configuration"** for further details.)

7.17.1 Clock Switching Enable

To enable clock switching, the FCKSM1 Configuration bit in the FOSC Configuration register must be programmed to a '0'. (Refer to **7.3 "Oscillator Configuration"** for further details.)

If the FCKSM1 Configuration bit is a '1' (unprogrammed), then the clock switching function is disabled. The Fail-Safe Clock Monitor function is also disabled. This is the default setting. The NOSC control bits in OSCCON do not control the clock selection when clock switching is disabled. However, the COSC bits in OSCCON will reflect the clock source selected by the FPR and FOS Configuration bits in the FOSC Configuration register. The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled. It is held at '0' at all times.

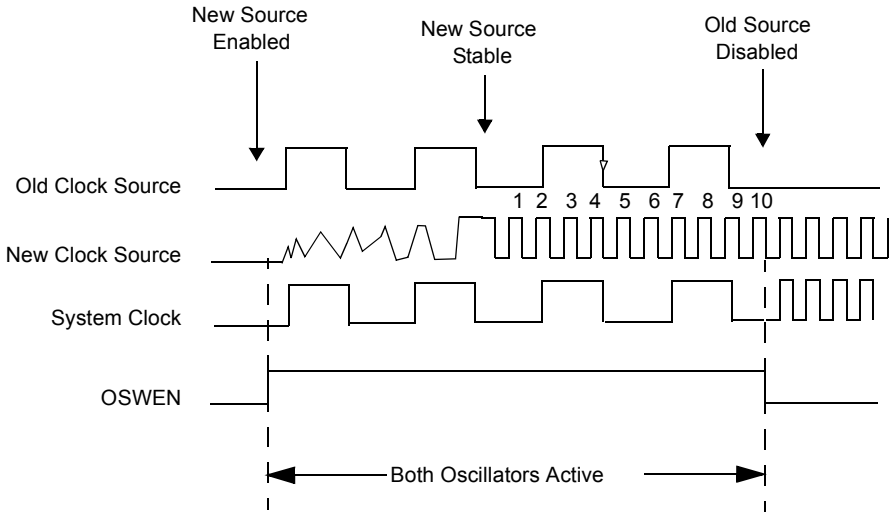
7.17.2 Oscillator Switching Sequence

The following steps are taken by the hardware and software to change the device clock source. (The steps shown below use the OSCCON register definition for the oscillator system VERSION 1. For a description of the OSCCON register for the oscillator system VERSION 2 and VERSION 3, refer to **Section 7.4 "Oscillator Control Registers – OSCCON and OSCTUN"**):

1. Read the COSC<1:0> status bits (OSCCON<13:12>), if desired, to determine current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSC<1:0> control bits (OSCCON<9:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit (OSCCON<0>). This will INITIATE the oscillator switch.
6. The clock switching hardware compares the COSC<1:0> status bits with the new value of the NOSC<1:0> control bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
7. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and the CF (OSCCON<3>) status bits are cleared.
8. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
9. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
10. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC<1:0> bit values are transferred to the COSC<1:0> status bits.
11. The clock switch is completed. The old clock source will be turned off at this time, with the following exceptions:
    - The LPRC oscillator will stay on if the WDT or FSCM is enabled.
    - The LP oscillator will stay on if LPOSCEN = 1 (OSCCON<1>).

Note:	The processor will continue to execute code throughout the clock switching sequence. Timing sensitive code should not be executed during this time.

Figure 7-14: Clock Transition Timing Diagram



Note: The system clock can be any selected source – Primary, Secondary, FRC or LPRC.

7.17.3 Clock Switching Tips

- If the destination clock source is a crystal oscillator, the clock switch time will be dominated by the oscillator start-up time.
- If the new clock source does not start, or is not present, then the clock switching hardware will simply wait for the 10 synchronization cycles to occur. The user can detect this situation because the OSWEN bit (OSCCON<0>) remains set indefinitely.
- If the new clock source uses the PLL, a clock switch will not occur until lock has been achieved. The user can detect a loss of PLL lock because the LOCK bit will be cleared and the OSWEN bit is set.
- The user may wish to consider the settings of the POST<1:0> control bits (OSCCON<7:6>) when executing a clock switch. Switching to a low-frequency clock source, such as the LP oscillator with a postscaler ratio greater than 1:1, will result in very slow device operation.

Note: The application should not attempt to switch to a clock of frequency lower than 100 kHz when the Fail-Safe Clock Monitor is enabled. If such clock switching is performed, the device may generate an oscillator fail trap and switch to the fast RC oscillator.

7.17.4 Aborting a Clock Switch

In the event the clock switch did not complete, the clock switch logic can be reset by clearing the OSWEN bit. Clearing the OSWEN bit (OSCCON<0>) will:

1. Abandon the clock switch
2. Stop and reset the OST, if applicable
3. Stop the PLL, if applicable

A clock switch procedure can be aborted at any time.

7.17.5 Entering Sleep Mode During a Clock Switch

If the device enters Sleep mode during a clock switch operation, the clock switch operation is aborted. The processor keeps the old clock selection and the OSWEN bit is cleared. The `PWRSAV` instruction is then executed normally.

7.17.6 Recommended Code Sequence for Clock Switching

The following steps should be taken to change the oscillator source:

- Disable interrupts during the OSCCON register unlock and write sequence.
- Execute unlock sequence for OSCCON high byte.
- Write new oscillator source to NOSC control bits.
- Execute unlock sequence for OSCCON low byte.
- Set OSWEN bit.
- Continue to execute code that is not clock sensitive (optional).
- Invoke an appropriate amount of software delay (cycle counting) to allow for oscillator and/or PLL start-up.
- Check to see if OSWEN is '0'. If it is, we are DONE SUCCESSFULLY.
- If OSWEN is still set, then check LOCK bit to determine cause of failure.

7.17.7 Clock Switch Code Examples

7.17.7.1 Starting a Clock Switch

The following code sequence shows how to unlock the OSCCON register and begin a clock switch operation:

Example 7-1:

```
;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
    MOV     #OSCCONH, w1
    MOV     #0x78, w2
    MOV     #0x9A, w3
    MOV.B   w2, [w1]
    MOV.B   w3, [w1]

;Set new oscillator selection
    MOV.B   WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
    MOV     #OSCCONL, w1
    MOV.B   #0x01, w0
    MOV     #0x46, w2
    MOV     #0x57, w3
    MOV.B   w2, [w1]
    MOV.B   w3, [w1]

;Start oscillator switch operation
    MOV.b   w0, [w1]
```

7.17.7.2 Aborting a Clock Switch

The following code sequence would be used to ABORT an unsuccessful clock switch:

Example 7-2:

```
MOV         OSCCON,W0           ; Read OSCCON into W0
BCLR        W0, #OSWEN          ; Clear bit 0 in W0
MOV         #OSCCON,W1          ; pointer to OSCCON
MOV.B       #0x46,W2            ; first unlock code
MOV.B       #0x57,W3            ; second unlock code
MOV.B       W2, [W1]            ; write first unlock code
MOV.B       W3, [W1]            ; write second unlock code
MOV.B       W0, [W1]            ; ABORT the switch
```

7.18 Design Tips

Question 1: ***When looking at the OSC2 pin after power-up with an oscilloscope, there is no clock. What can cause this?***

Answer:

1. Entering Sleep mode with no source for wake-up (such as, WDT, $\overline{\text{MCLR}}$, or an interrupt). Verify that the code does not put the device to Sleep without providing for wake-up. If it is possible, try waking it up with a low pulse on $\overline{\text{MCLR}}$. Powering up with $\overline{\text{MCLR}}$ held low will also give the crystal oscillator more time to start-up, but the Program Counter will not advance until the $\overline{\text{MCLR}}$ pin is high.
2. The wrong Clock mode is selected for the desired frequency. For a blank device, the default oscillator is EC + 16x PLL. Most parts come with the clock selected in the Default mode, which will not start oscillation with a crystal or resonator. Verify that the Clock mode has been programmed correctly.
3. The proper power-up sequence has not been followed. If a CMOS part is powered through an I/O pin prior to power-up, bad things can happen (latch-up, improper start-up, etc.). It is also possible for brown-out conditions, noisy power lines at start-up, and slow V_{DD} rise times to cause problems. Try powering up the device with nothing connected to the I/O, and power-up with a known, good, fast rise, power supply. Refer to the power-up information in the device data sheet for considerations on brown-out and power-up sequences.
4. The C1 and C2 capacitors attached to the crystal have not been connected properly or are not the correct values. Make sure all connections are correct. The device data sheet values for these components will usually get the oscillator running; however, they just might not be the optimal values for your design.

Question 2: ***The device starts, but runs at a frequency much higher than the resonant frequency of the crystal.***

Answer: The gain is too high for this oscillator circuit. Refer to **Section 7.6 "Crystal Oscillators/Ceramic Resonators"** to aid in the selection of C2 (may need to be higher), Rs (may be needed) and Clock mode (wrong mode may be selected). This is especially possible for low-frequency crystals, like the common 32.768 kHz.

Question 3: ***The design runs fine, but the frequency is slightly off. What can be done to adjust this?***

Answer: Changing the value of C1 has some effect on the oscillator frequency. If a SERIES resonant crystal is used, it will resonate at a different frequency than a PARALLEL resonant crystal of the same frequency call-out. Ensure that you are using a PARALLEL resonant crystal.

Question 4: ***The board works fine, then suddenly quits or loses time.***

Answer: Other than the obvious software checks that should be done to investigate losing time, it is possible that the amplitude of the oscillator output is not high enough to reliably trigger the oscillator input. Look at the C1 and C2 values and ensure that the device Configuration bits are correct for the desired Oscillator mode.

Question 5: ***If I put an oscilloscope probe on an oscillator pin, I don't see what I expect. Why?***

Answer: Remember that an oscilloscope probe has capacitance. Connecting the probe to the oscillator circuitry will modify the oscillator characteristics. Consider using a low-capacitance (active) probe.

7.19 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Oscillator module are:

Title	Application Note #
PICmicro® Microcontroller Oscillator Design Guide	AN588
Low Power Design using PICmicro® Microcontrollers	AN606
Crystal Oscillator Basics and Crystal Selection for rfPIC® and PICmicro® Devices	AN826

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F Family of devices.

7.20 Revision History

Revision A

This is the initial released revision of this document.

Revision B

This revision incorporates technical content changes for the dsPIC30F Oscillator module.

Revision C

This revision incorporates all known errata at the time of this document update.

Revision D

This revision incorporates details on the three versions (VERSION 1, VERSION 2 and VERSION 3) of the Oscillator system implemented in dsPIC30F devices in the General Purpose, Sensor and Motor Control families.

Revision E

This revision incorporates a correction to **Register 7-3: "FOSC: Oscillator Configuration Register for Oscillator System VERSION 3"**.