**HIGHLIGHTS**

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</table>
62.1 INTRODUCTION

This Digital-to-Analog Converter (DAC) module has 10-bit resolution. Data input is in the form of a 10-bit digital value and it supports left and right-justified input data. Data output is an analog voltage, which is proportional to the digital input value. The module can generate output voltages between AVSS and the configured positive DAC reference.

When the DAC module is disabled, it consumes minimum current and its associated output pin can be used as an I/O. The module takes warm-up time (TON) to stabilize after it is enabled. A simplified block diagram of DAC module is shown in Figure 62-1.

Note: For more information on Power-Down current (IPD) and TON specifications, refer to the specific device data sheet.

---

Figure 62-1: DAC Module Block Diagram

Note 1: The INTREF is an internal reference voltage. The INTREF source can vary with the device. For more information refer to the specific device data sheet.

2: The supported trigger inputs vary with the device. For more information on supported trigger inputs, refer to the specific device data sheet.
Section 62. 10-bit Digital-to-Analog Converter (DAC)

62.2 KEY FEATURES

The DAC has the following key features:
- High-Precision 10-bit DAC Core
- High-Data-Throughput/Fast Settling Time
- Supports Internal and External Reference Options
- Supports both Left and Right-Justified Input Data Options
- Integration with other Peripherals
- Selectable Trigger Options
- Input Data can be supplied by DMA
- Operates in Idle and Sleep Mode

62.3 DAC REGISTERS

The DAC module is controlled by two DAC registers.
- DACxCON: DAC Control Register
  This register configures the corresponding DAC module by:
  - Enabling/Disabling the DAC Module
  - Specifying Input Data Format (Right-justified or Left-justified)
  - Enabling DAC Trigger Input
  - Selecting DAC Trigger Source
  - Enabling DAC Output
  - Operations in Idle/Sleep Mode
  - Selecting Reference Source
- DACxDAT: DAC Data Register
  This register specifies both right and left-justified data and also holds the digital data which needs to be converted into analog voltage.
Register 62-1: DACxCON: DAC CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DACEN</td>
<td>—</td>
<td>D ACSIDL</td>
<td>DACSLP</td>
<td>DACFM</td>
<td>—</td>
<td>—</td>
<td>D ACTRIG</td>
</tr>
</tbody>
</table>

bit 15
DACEN: DAC Module Enable bit
1 = Module is enabled
0 = Module is disabled (power consumption is minimal)

bit 14
DACSIDL: DAC Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = DAC continues to operate and outputs the last set value

bit 13
DACSLP: DAC Enable During Sleep Mode
1 = DAC continues to operate and outputs the last set value
0 = Discontinue module operation in Sleep mode

bit 12
DACFM: DAC Data Format Select bit
1 = Data is left-justified
0 = Data is right-justified

bit 11-9
Unimplemented: Read as '0'

bit 8
DACTRIG: Trigger Input Enable bit
1 = The DAC output changes on low-to-high transition of the selected trigger source
0 = The DAC analog output value updates when the DACxDAT is written

bit 7
DACOE: DAC Output Buffer Enable(1)
1 = Output is enabled; DAC voltage is driven to pin (when DACEN = 1)
0 = Output is disabled and the pin can be used as an I/O

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown

**Note 1:** The DACOE bit is not implemented in all devices. For more information on DACOE bit, refer to the specific device data sheet. When implemented, it is recommended to set DACOE bit before enabling DACEN bit.

**Note 2:** For more information on supported trigger inputs, refer to the specific device data sheet.

**Note 3:** If 2 * INTREF is selected as a reference source, ensure that the INTREF voltage is not exceeding AVDD/2.
Section 62. 10-bit Digital-to-Analog Converter (DAC)

Register 62-1: DACxCON: DAC CONTROL REGISTER (Continued)

bit 6-2: DACTSEL<4:0>: DAC Trigger Source Select bits\(^{(2)}\)

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11111</td>
<td>Reserved</td>
</tr>
<tr>
<td>00110</td>
<td>DAC Trigger 6</td>
</tr>
<tr>
<td>00100</td>
<td>DAC Trigger 5</td>
</tr>
<tr>
<td>00011</td>
<td>DAC Trigger 4</td>
</tr>
<tr>
<td>00010</td>
<td>DAC Trigger 3</td>
</tr>
<tr>
<td>00001</td>
<td>DAC Trigger 2</td>
</tr>
<tr>
<td>00000</td>
<td>DAC Trigger 1</td>
</tr>
</tbody>
</table>

bit 1-0: DACREF<1:0>: Reference Source Select bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Reference connected to 2 * INTREF internal reference output(^{(3)})</td>
</tr>
<tr>
<td>10</td>
<td>AVDD</td>
</tr>
<tr>
<td>01</td>
<td>DVREF+ Pin</td>
</tr>
<tr>
<td>00</td>
<td>Reference not connected; analog portion of DAC consumes minimal reference current</td>
</tr>
</tbody>
</table>

Note 1: The DACOE bit is not implemented in all devices. For more information on DACOE bit, refer to the specific device data sheet. When implemented, it is recommended to set DACOE bit before enabling DACEN bit.

2: For more information on supported trigger inputs, refer to the specific device data sheet.

3: If 2 * INTREF is selected as a reference source, ensure that the INTREF voltage is not exceeding AVDD/2.
Register 62-2: **DACxDAT: DAC Data Register (DACFM = 0) – Data Right-Justified**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DACDAT&lt;9:8&gt;</td>
<td></td>
</tr>
</tbody>
</table>

bit 15

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DACDAT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

bit 15-10: **Unimplemented**: Read as '0'

bit 9-0: **DACDAT<9:0>: DAC Data bits**
Data input register for DAC (right-justified)

Register 62-3: **DACxDAT: DAC Data Register (DACFM = 1) – Data Left-Justified**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DACDAT&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 15

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DACDAT&lt;7:6&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

bit 15-6: **DACDAT<15:6>: DAC Data bits**
Data input register for DAC (left-justified)

bit 5-0: **Unimplemented**: Read as '0'
62.4 DAC CONFIGURATION

62.4.1 DAC Input Data Format Selection

The 10-bit input data to DAC can either be left-justified or right-justified. This can be selected using the DACFM (DACxCON<11>) bit.

62.4.2 DAC Reference Source Selection

There are three reference sources available for the DAC module. They are AVDD, DVREF+ pin and 2 * INTREF is selected as a reference source, ensure that the INTREF voltage is not exceeding AVDD/2. One of these can be selected using the DACREF<1:0> (DACxCON<1:0>) bits. These reference sources are only the upper reference and the lower reference is always fixed at AVSS.

62.4.3 DAC Trigger and Trigger Source Selection

The DAC input data is provided in two ways. When the DACTRIG (DACxCON<8>) bit is ‘0’, the input data is provided as soon as DACxDAT register is updated. When the DACTRIG bit is ‘1’, the last DACxDAT value is provided to DAC module when the selected trigger source triggers. The trigger source can be selected using the DACTSEL<4:0> (DACxCON<6:2>) bits.

When the Trigger mode is selected, the data shadow register is automatically enabled. This shadow register provides the data available in DACxDAT register to the DAC module, only on the occurrence of the selected trigger event. This triggering is synchronised with the system clock.

Figure 62-2 and Figure 62-3 illustrate the timing diagram for DAC input when the trigger is enabled or disabled.
62.4.4 Enabling the DAC Module

The DAC module is enabled using the DACEN (DACxCON<15>) bit. When DACEN bit is ‘1’, the DAC module is enabled and the module takes TON time to get warmed up. When DACEN bit is ‘0’, the DAC module is disabled. When the DAC module is disabled the Reference Voltage Source is disconnected from the converter to optimize the power consumption.

62.4.5 Enabling DAC Output

The output of the DAC module can be enabled by using the DACOE (DACxCON<7>) bit. On enabling the output, an analog voltage corresponding to digital input data will be available on the pin as shown in Equation 62-1.

Equation 62-1: DAC OUTPUT VOLTAGE

\[ V_{DAC} = \frac{(V_{DACREF}) \cdot (DACxDAT)}{1024} \]

Where,

- \( V_{DAC} \) is the analog output voltage provided to the DACx pin.
- \( V_{DACREF} \) is the reference voltage applied on \( DV_{REF} \) pin, \( AV_{DD} \) or 2 * INTREF, as per the selection.
Section 62. 10-bit Digital-to-Analog Converter (DAC)

62.5 DAC INTERRUPT GENERATION

DAC module generates interrupt only when the DAC Trigger mode is enabled (DACTRIG = 1). The interrupt is generated when the selected trigger source triggers the DAC conversion. Upon DAC interrupt generation DACxIF bit becomes ‘1’.

62.6 DAC CONFIGURATION EXAMPLE

The following steps should be followed to configure DAC module:
1. Select the DAC Reference Voltage (DACxCON<1:0>).
2. Select the Input Data Format (DACxCON<11>).
3. Select the Input Data Feed mode (DACxCON<8>).
4. Select Trigger Source, if Trigger mode is enabled (DACxCON<6:2>).
5. Configure the DAC interrupt (if required):
   a) Clear the DACxIF bit
   b) Select interrupt priority bit (DACxIP<2:0>)
   c) Set the DACxE bit
   d) Enable DAC Output (DACxCON<7>)
6. If the DMA is used to provide input data to DAC then refer to the “DMA” section in the specific device data sheet for how to configure the DMA.
7. Turn-on DAC module (DACxCON<15>).

62.7 OPERATION IN POWER-SAVING MODES

62.7.1 DAC Operation during CPU Idle Mode

When the CPU enters Idle mode, the module behaves in one of two ways depending on the state of the DACSIDL (DACxCON<13>) bit.

- When DACSIDL = 0, the module operates without any change and the last output voltage remains on the pin.
- When DACSIDL = 1, the module shuts down, when device enters Idle mode tri-stating the DACO pin.

62.7.2 DAC Operation during CPU Doze Mode

When the CPU enters Doze mode, the DAC module is not affected and operates normally.

62.7.3 DAC Operation during CPU Sleep Mode

When the CPU enters Sleep mode, the module behaves in one of two ways depending on the state of the DACSLP ((DACxCON<12>) bit.

- When DACSLP = 1, the module operates without any change and the last output voltage remains on the pin.
- When DACSLP = 0, the module shuts down, when device enters Sleep mode tri-stating the DACO pin.
### 62.8 REGISTER MAP

**TABLE 62-2: DACx REGISTER MAP**

<table>
<thead>
<tr>
<th>File Name</th>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 11</th>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>All Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>DACxCON</td>
<td>Dacen</td>
<td>—</td>
<td>Dacsidl</td>
<td>Dacslp</td>
<td>Dacfm</td>
<td>—</td>
<td>—</td>
<td>Dacrig</td>
<td>Dacoe</td>
<td>Dactsel4</td>
<td>Dactsel3</td>
<td>Dactsel2</td>
<td>Dactsel1</td>
<td>Dactsel0</td>
<td>Dacref1</td>
<td>Dacref0</td>
<td>DACxCON</td>
</tr>
<tr>
<td>DACxDAT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10-bit DACx Digital Input Value Register (right or left-justified)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:  
— = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.
## Section 62. 10-bit Digital-to-Analog Converter (DAC)

### 62.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Digital-to-Analog Converter (DAC) are:

<table>
<thead>
<tr>
<th>Title</th>
<th>Application Note #</th>
</tr>
</thead>
<tbody>
<tr>
<td>No related application notes are available at this time.</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Please visit the Microchip web site ([www.microchip.com](http://www.microchip.com)) for additional application notes and code examples for the PIC24F family of devices.
62.10  REVISION HISTORY

Revision A (August 2012)
This is the initial released version of the document.
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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Fax: 86-571-2819-3189

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Fax: 86-532-8502-7205

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Fax: 86-21-5407-5066

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Fax: 86-27-5980-5118

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Fax: 86-29-8833-7256

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Fax: 86-592-2388130

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Fax: 81-66-152-9310

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Fax: 82-53-744-4302

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82-2-558-5934

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