Section 62. 10-bit Digital-to-Analog Converter (DAC)

HIGHLIGHTS

This section of the manual contains the following major topics:

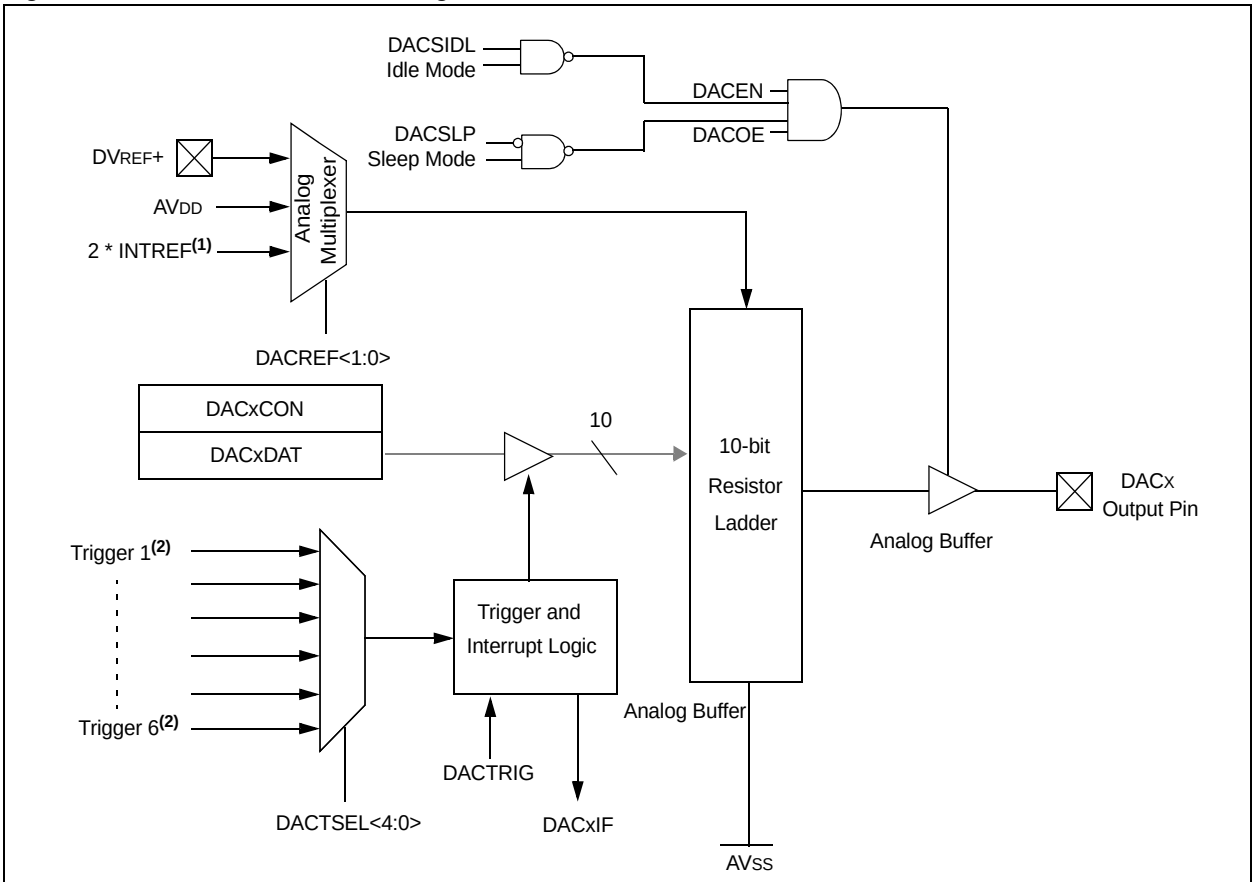
62.1 INTRODUCTION

This Digital-to-Analog Converter (DAC) module has 10-bit resolution. Data input is in the form of a 10-bit digital value and it supports left and right-justified input data. Data output is an analog voltage, which is proportional to the digital input value. The module can generate output voltages between AVSS and the configured positive DAC reference.

When the DAC module is disabled, it consumes minimum current and its associated output pin can be used as an I/O. The module takes warm-up time (TON) to stabilize after it is enabled. A simplified block diagram of DAC module is shown in Figure 62-1.

Note:	For more information on Power-Down current (IPD) and TON specifications, refer to the specific device data sheet.

Figure 62-1: DAC Module Block Diagram



Note 1: The INTREF is a internal reference voltage. The INTREF source can be vary with the device. For more information refer to the specific device data sheet.

2: The supported trigger inputs vary with the device. For more information on supported trigger inputs, refer to the specific device data sheet.

62.2 KEY FEATURES

The DAC has the following key features:

- High-Precision 10-bit DAC Core
- High-Data-Throughput/Fast Settling Time
- Supports Internal and External Reference Options
- Supports both Left and Right-Justified Input Data Options
- Integration with other Peripherals
- Selectable Trigger Options
- Input Data can be supplied by DMA
- Operates in Idle and Sleep Mode

62.3 DAC REGISTERS

The DAC module is controlled by two DAC registers.

- DACxCON: DAC Control Register

This register configures the corresponding DAC module by:

  - Enabling/Disabling the DAC Module
  - Specifying Input Data Format (Right-justified or Left-justified)
  - Enabling DAC Trigger Input
  - Selecting DAC Trigger Source
  - Enabling DAC Output
  - Operations in Idle/Sleep Mode
  - Selecting Reference Source

- DACxDAT: DAC Data Register

This register specifies both right and left-justified data and also holds the digital data which needs to be converted into analog voltage.

Register 62-1: DACxCON: DAC CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
DACEN	—	DACSIDL	DACSLP	DACFM	—	—	DACTRIG
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACOE	DACTSEL<4:0>					DACREF<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DACEN:** DAC Module Enable bit
1 = Module is enabled
0 = Module is disabled (power consumption is minimal)

bit 14 **Unimplemented:** Read as '0'

bit 13 **DACSIDL:** DAC Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = DAC continues to operate and outputs the last set value

bit 12 **DACSLP:** DAC Enable During Sleep Mode
1 = DAC continues to operate and outputs the last set value
0 = Discontinue module operation in Sleep mode

bit 11 **DACFM:** DAC Data Format Select bit
1 = Data is left-justified
0 = Data is right-justified

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **DACTRIG:** Trigger Input Enable bit
1 = The DAC output changes on low-to-high transition of the selected trigger source
0 = The DAC analog output value updates when the DACxDAT is written

bit 7 **DACOE:** DAC Output Buffer Enable(1)
1 = Output is enabled; DAC voltage is driven to pin (when DACEN = 1)
0 = Output is disabled and the pin can be used as an I/O

Note 1: The DACOE bit is not implemented in all devices. For more information on DACOE bit, refer to the specific device data sheet. When implemented, it is recommended to set DACOE bit before enabling DACEN bit.
2: For more information on supported trigger inputs, refer to the specific device data sheet.
3: If 2 * INTREF is selected as a reference source, ensure that the INTREF voltage is not exceeding $AV_{DD}/2$.

Register 62-1: DACxCON: DAC CONTROL REGISTER (Continued)

bit 6-2 **DACTSEL<4:0>:** DAC Trigger Source Select bits[2]

11111
• • • = Reserved
00110
00101 = DAC Trigger 6
00100 = DAC Trigger 5
00011 = DAC Trigger 4
00010 = DAC Trigger 3
00001 = DAC Trigger 2
00000 = DAC Trigger 1

bit 1-0 **DACREF<1:0>:** Reference Source Select bits

11 = Reference connected to 2 * INTREF internal reference output[3]
10 = AV_{DD}
01 = DV_{REF+} Pin
00 = Reference not connected; analog portion of DAC consumes minimal reference current

Note 1: The DACOE bit is not implemented in all devices. For more information on DACOE bit, refer to the specific device data sheet. When implemented, it is recommended to set DACOE bit before enabling DACEN bit.

2: For more information on supported trigger inputs, refer to the specific device data sheet.

3: If 2 * INTREF is selected as a reference source, ensure that the INTREF voltage is not exceeding $AV_{DD}/2$.

Register 62-2: DACxDAT: DAC Data Register (DACFM = 0) – Data Right-Justified

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	DACDAT<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACDAT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **DACDAT<9:0>:** DAC Data bits
Data input register for DAC (right-justified)

Register 62-3: DACxDAT: DAC Data Register (DACFM = 1) – Data Left-Justified

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACDAT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
DACDAT<7:6>		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **DACDAT<15:6>:** DAC Data bits
Data input register for DAC (left-justified)

bit 5-0 **Unimplemented:** Read as '0'

62.4 DAC CONFIGURATION

62.4.1 DAC Input Data Format Selection

The 10-bit input data to DAC can either left-justified or right-justified. This can be selected using the DACFM (DACxCON<11>) bit.

62.4.2 DAC Reference Source Selection

There are three reference sources available for the DAC module. They are AVDD, DVREF+ pin and 2 * INTREF is selected as a reference source, ensure that the INTREF voltage is not exceeding AVDD/2. One of these can be selected using the DACREF<1:0> (DACxCON<1:0>) bits. These reference sources are only the upper reference and the lower reference is always fixed at AVSS.

62.4.3 DAC Trigger and Trigger Source Selection

The DAC input data is provided in two ways. When the DACTRIG (DACxCON<8>) bit is '0', the input data is provided as soon as DACxDAT register is updated. When the DACTRIG bit is '1', the last DACxDAT value is provided to DAC module when the selected trigger source triggers. The trigger source can be selected using the DACTSEL<4:0> (DACxCON<6:2>) bits.

When the Trigger mode is selected, the data shadow register is automatically enabled. This shadow register provides the data available in DACxDAT register to the DAC module, only on the occurrence of the selected trigger event. This triggering is synchronised with the system clock.

Figure 62-2 and Figure 62-3 illustrate the timing diagram for DAC input when the trigger is enabled or disabled.

Figure 62-2: Timing Diagram – Trigger Enabled (DACTRIG = 1)

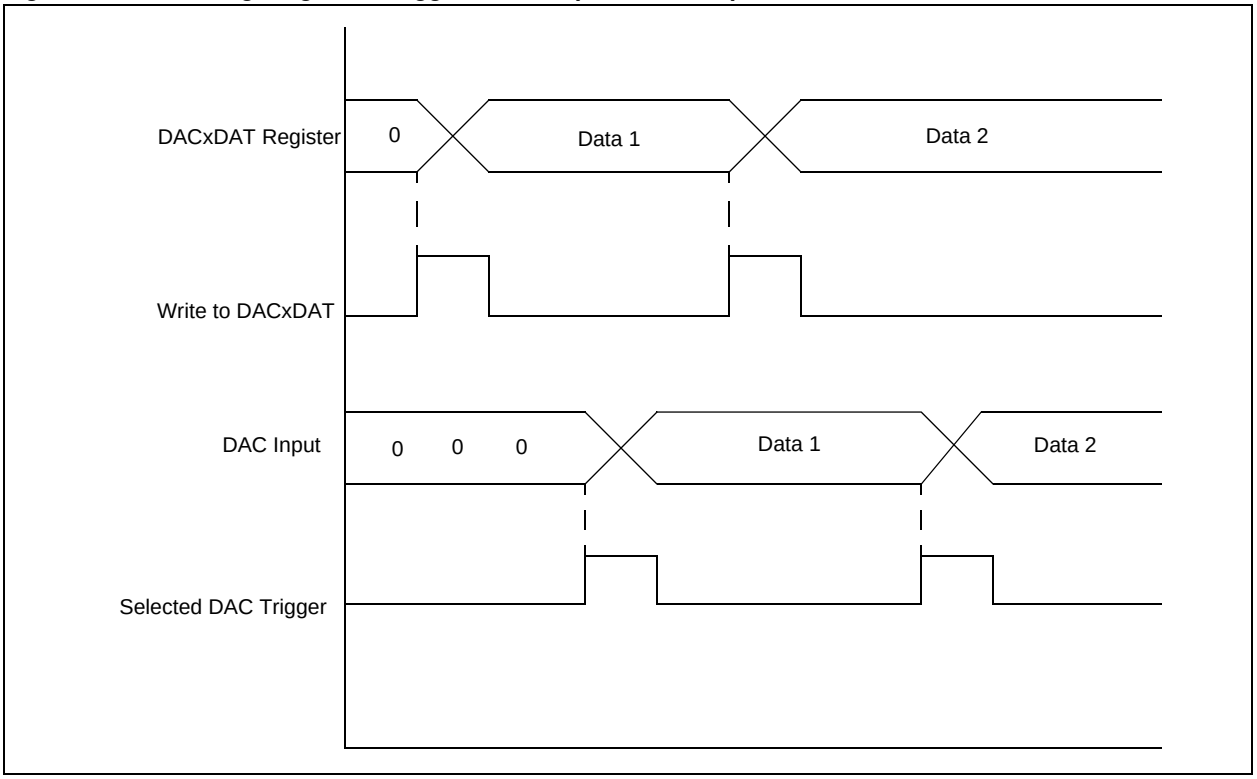
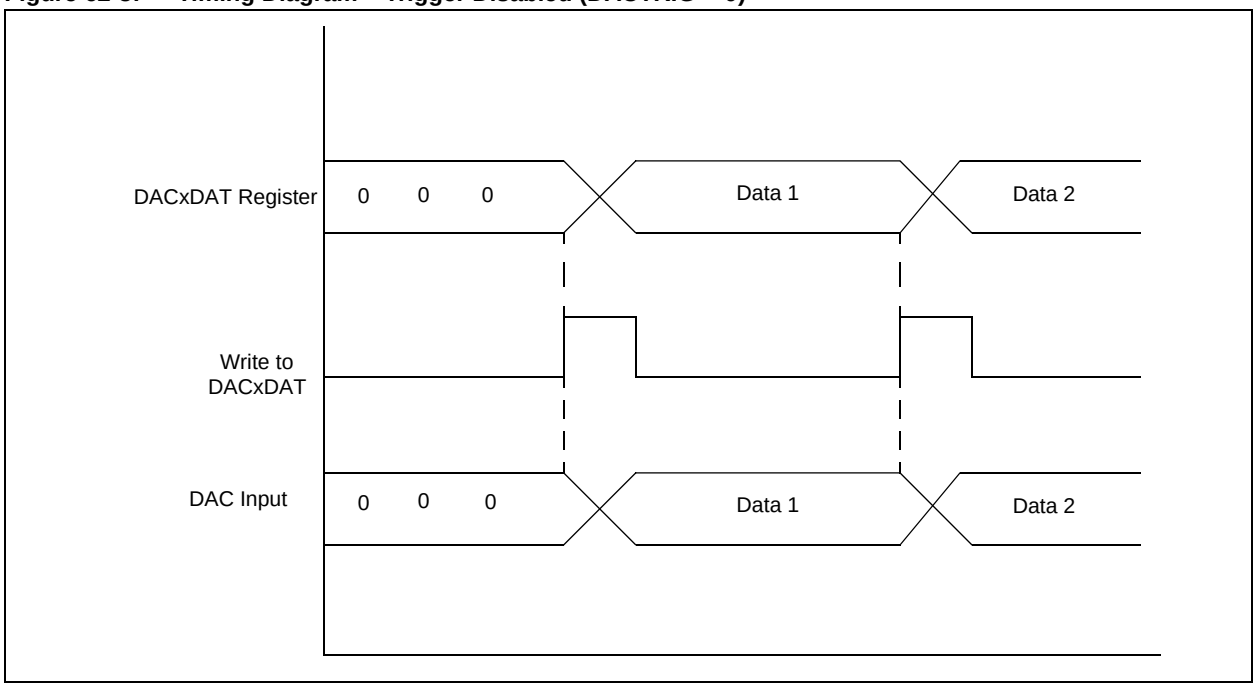


Figure 62-3: Timing Diagram – Trigger Disabled (DACTRIG = 0)



62.4.4 Enabling the DAC Module

The DAC module is enabled using the DACEN (DACxCON<15>) bit. When DACEN bit is '1', the DAC module is enabled and the module takes TON time to get warmed up. When DACEN bit is '0', the DAC module is disabled. When the DAC module is disabled the Reference Voltage Source is disconnected from the converter to optimize the power consumption.

62.4.5 Enabling DAC Output

The output of the DAC module can be enabled by using the DACOE (DACxCON<7>) bit. On enabling the output, an analog voltage corresponding to digital input data will be available on the pin as shown in Equation 62-1.

Equation 62-1: DAC OUTPUT VOLTAGE

$$V_{DAC} = \frac{(V_{DACREF}) \cdot (DACxDAT)}{1024}$$

Where,

V_{DAC} is the analog output voltage provided to the DACx pin.

V_{DACREF} is the reference voltage applied on DV_{REF+} pin, AV_{DD} or $2 * INTREF$, as per the selection.

62.5 DAC INTERRUPT GENERATION

DAC module generates interrupt only when the DAC Trigger mode is enabled (DACTRIG = 1). The interrupt is generated when the selected trigger source triggers the DAC conversion. Upon DAC interrupt generation DACxIF bit becomes '1'.

62.6 DAC CONFIGURATION EXAMPLE

The following steps should be followed to configure DAC module:

1. Select the DAC Reference Voltage (DACxCON<1:0>).
2. Select the Input Data Format (DACxCON<11>).
3. Select the Input Data Feed mode (DACxCON<8>).
4. Select Trigger Source, if Trigger mode is enabled (DACxCON<6:2>).
5. Configure the DAC interrupt (if required):
   a) Clear the DACxIF bit
   b) Select interrupt priority bit (DACxIP<2:0>)
   c) Set the DACxIE bit
   d) Enable DAC Output (DACxCON<7>)
6. If the DMA is used to provide input data to DAC then refer to the **"DMA"** section in the specific device data sheet for how to configure the DMA.
7. Turn-on DAC module (DACxCON<15>).

62.7 OPERATION IN POWER-SAVING MODES

62.7.1 DAC Operation during CPU Idle Mode

When the CPU enters Idle mode, the module behaves in one of two ways depending on the state of the DACSIDL (DACxCON<13>) bit.

- When DACSIDL = 0, the module operates without any change and the last output voltage remains on the pin.
- When DACSIDL = 1, the module shuts down, when device enters Idle mode tri-stating the DACO pin.

62.7.2 DAC Operation during CPU Doze Mode

When the CPU enters Doze mode, the DAC module is not affected and operates normally.

62.7.3 DAC Operation during CPU Sleep Mode

When the CPU enters Sleep mode, the module behaves in one of two ways depending on the state of the DACSLP ((DACxCON<12>) bit.

- When DACSLP = 1, the module operates without any change and the last output voltage remains on the pin.
- When DACSLP = 0, the module shuts down, when device enters Sleep mode tri-stating the DACO pin.

62.8 REGISTER MAP

TABLE 62-2: DACx REGISTER MAP

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DACxCON	DACEN	—	DACSIDL	DACSLP	DACFM	—	—	DACTRIG	DACOE	DACTSEL4	DACTSEL3	DACTSEL2	DACTSEL1	DACTSEL0	DACREF1	DACREF0	0000
DACxDAT	10-bit DACx Digital Input Value Register (right or left-justified)																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

62.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Digital-to-Analog Converter (DAC) are:

Title	Application Note #

No related application notes are available at this time.

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

62.10 REVISION HISTORY

Revision A (August 2012)

This is the initial released version of the document.

Note the following details of the code protection feature on Microchip devices:

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