Section 60. Capture/Compare/PWM Modules (CCP and ECCP)

HIGHLIGHTS

This section of the manual contains the following major topics:

60.1 INTRODUCTION

Select PIC24 family devices incorporate one or more combined Capture/Compare/PWM (CCP) modules. In addition, devices that use the CCP module may also include one or more Enhanced CCP (ECCP) modules. These modules are identical to their counterparts found in PIC18 microcontrollers, and provide many of the same features of the Input Capture and Output Compare modules used in other PIC24F devices.

CCP and ECCP modules are differentiated by their PWM features. The standard CCP module provides a single PWM output, while the ECCP module can drive up to four PWM outputs. The enhanced PWM features make the ECCP module suitable for a variety of power and motor control applications. Because the CCP and ECCP modules otherwise share identical features, both are described in this section.

Key features of all CCP modules include:

- 16-bit Input Capture for a range of edge events
- 16-bit Output Compare with multiple output options
- Single output Pulse-Width Modulation with up to 10 bits of resolution
- User-selectable time base from any available timer
- Special Event Trigger on Capture and Compare events to automatically trigger a range of peripherals

ECCP modules also include these features:

- Operation in Half-Bridge and Full-Bridge (Forward and Reverse) modes
- Pulse Steering Control across any or all Enhanced PWM pins, with user-configurable steering synchronization
- User-configurable External Fault Detect with Auto-Shutdown and Auto-Restart

As with other peripherals, CCP modules are numbered sequentially when more than one is included in a particular device. When CCP and ECCP modules occur together, the ECCP modules are assigned the lowest sequence numbers.

Note:	Throughout this section, generic references are used for register and bit names that are the same, except for an ‘x’ variable that indicates the item’s association to a specific CCP module. For the sake of clarity, all module operations are described generically, and are equally applicable to all CCP modules. Similarly, all generic descriptions of Enhanced PWM operations are equally applicable to all ECCP modules.

60.2 REGISTERS

Each CCP module contains at least three registers, one control register and two data registers that combine to form a single, 16-bit virtual register. ECCP modules contain three additional registers to control Enhanced PWM features. Additional control registers are used to allocate timer resources to the CCP and ECCP modules.

All registers are readable and writable.

60.2.1 Control Registers

Each CCP module is controlled by its CCPxCON register (Register 60-1). CCPxCON selects the module's operating mode with the CCPxM<3:0> bit field. It also stores the two Least Significant bits (LSbs) of the 10-bit PWM duty cycle (DCxB<1:0>) in bits 5 and 4.

ECCP modules use an extended version of the CCPxCON register (Register 60-2). In addition to all the bits described in the standard version of CCPxCON, the ECCPxCON register contains the PxM<1:0> bits (ECCPxCON<7:6>); these are used to select the Enhanced PWM mode.

In addition to ECCPxCON, each ECCP module implements three additional registers to control ECCP functionality:

- ECCPxAS, the Auto-Shutdown Control Register (Register 60-3)
- ECCPxDEL, the Enhanced PWM Control Register (Register 60-4)
- PSTRxCON, the Pulse Steering Control Register (Register 60-5)

The advanced features controlled by these three registers are described in **Section 60.7 "Enhanced PWM Mode"**.

60.2.2 CCPRx Registers

Each CCP or ECCP module incorporates a virtual 16-bit register that can function as a 16-bit Capture register, a 16-bit Compare register or a PWM Master/Slave Duty Cycle register. In PIC24 devices, this virtual 16-bit register is split between two physical registers: CCPRxL for the lower byte and CCPRxH for the upper byte. Data is stored in the lower byte of each physical register.

For Capture and Compare operations, CCPRxL and CCPRxH are used to capture a 16-bit timer value or store a 16-bit value for comparison, depending on the moduler's configuration. For all PWM operations, only the CCPRxL register is used to store the upper eight bits of the 10-bit Duty Cycle. The corresponding CCPRxH register is used as a slave buffer and is not available to the user.

60.2.3 CCPTMRS (Timer Resource) Registers

To allow the most flexibility in using timer resources, PIC24F devices that incorporate the CCP and ECCP modules use a dedicated set of control registers to match the available 8/16-bit timers to CCP modules. These registers are not actually part of the CCP modules or the timers, but provide device level integration. The registers take the generic name, "CCPTMRSn", where "n" represents a register number. Each CCPTMRS register controls timer assignments for more than one ECCP module, mapping different timers or timer pairs to different CCP modules.

The number of CCPTMRS registers present in a particular device is determined by the number of CCP modules, and the number and type of timers. As these combinations are device-specific and highly variable, each set of CCPTMRS registers has a device-specific bit mapping. Specific versions of the registers are provided in the specific device data sheet. A hypothetical example is shown in Register 60-6.

Additional information on timer and CCP module mapping is provided in **Section 60.3.1 "Timer Resources and Selection"**.

Register 60-1: CCPxCON: CCPx Control Register (Standard CCP Modules)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-4 **DCxB<1:0>**: PWM Duty Cycle bit 1 and bit 0 for the CCPx Module

Capture and Compare modes:
Unused.

PWM mode:
These bits are the two Least Significant bits (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight Most Significant bits (DCxB<9:2>) of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM<3:0>**: CCPx Module Mode Select bits

1111 = Reserved
1110 = Reserved
1101 = Reserved
1100 = PWM mode
1011 = Compare mode: Special Event Trigger; reset timer on CCPx match (CCPxIF bit is set)(1)
1010 = Compare mode: Generate software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)
1001 = Compare mode: Initialize CCPx pin high; on compare match, force CCPx pin low (CCPxIF bit is set)
1000 = Compare mode: Initialize CCPx pin low; on compare match, force CCPx pin high (CCPxIF bit is set)
0111 = Capture mode: Every 16th rising edge
0110 = Capture mode: Every 4th rising edge
0101 = Capture mode: Every rising edge
0100 = Capture mode: Every falling edge
0011 = Reserved
0010 = Compare mode: Toggle output on match (CCPxIF bit is set)
0001 = Reserved
0000 = Capture/Compare/PWM is disabled (resets CCPx module)

Note 1: CCPxM<3:0> = 1011 will only reset the timer and not start the A/D conversion on CCPx match.

Register 60-2: ECCPxCON: ECCPx Control Register (ECCP Modules Only)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxM1	PxM0	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **PxM<1:0>:** Enhanced PWM Output Configuration bits

If CCPxM<3:2> = 00, 01, 10:

xx = PxA is assigned as Capture input or Compare output; PxB, PxC and PxD are assigned as port pins

If CCPxM<3:2> = 11:

11 = Full-Bridge Output Reverse: PxB is modulated; PxC is active; PxA and PxD are inactive

10 = Half-Bridge Output: PxA, PxB are modulated with dead-band control; PxC and PxD are assigned as port pins

01 = Full-Bridge Output Forward: PxD is modulated; PxA is active; PxB, PxC are inactive

00 = Single Output: PxA, PxB, PxC and PxD are controlled by steering (see **Section 60.7.7 "Pulse Steering Mode"**)

bit 5-4 **DCxB<1:0>**: PWM Duty Cycle bit 1 and bit 0 for CCPx Module

Capture and Compare modes:

Unused.

PWM mode:

These bits are the two Least Significant bits (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight Most Significant bits (DCxB<9:2>) of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM<3:0>**: CCPx Module Mode Select bits

1111 = PWM mode: PA and PC are active-low; PB and PD are active-low

1110 = PWM mode: PA and PC are active-low; PB and PD are active-high

1101 = PWM mode: PA and PC are active-high; PB and PD are active-low

1100 = PWM mode: PA and PC are active-high; PB and PD are active-high

1011 = Compare mode: Special Event Trigger; reset timer on CCPx match (CCPxIF bit is set)(1)

1010 = Compare mode: Generate software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)

1001 = Compare mode: Initialize CCPx pin high; on compare match, force CCPx pin low (CCPxIF bit is set)

1000 = Compare mode: Initialize CCPx pin low; on compare match, force CCPx pin high (CCPxIF bit is set)

0111 = Capture mode: Every 16th rising edge

0110 = Capture mode: Every 4th rising edge

0101 = Capture mode: Every rising edge

0100 = Capture mode: Every falling edge

0011 = Reserved

0010 = Compare mode: Toggle output on match (CCPxIF bit is set)

0001 = Reserved

0000 = Capture/Compare/PWM is disabled (resets CCPx module)

Note 1: CCPxM<3:0> = 1011 will only reset the timer and not start the A/D conversion on CCPx match.

Register 60-3: ECCPxAS: ECCPx Auto-Shutdown Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPxASE	ECCPxAS2	ECCPxAS1	ECCPxAS0	PSSxAC1	PSSxAC0	PSSxBD1	PSSxBD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ECCPxASE:** ECCP Auto-Shutdown Event Status bit
1 = A shutdown event has occurred; ECCP outputs are in a shutdown state
0 = ECCP outputs are operating

bit 6-4 **ECCPxAS<2:0>:** ECCP Auto-Shutdown Source Select bits
111 = VIL on $\overline{FLT0}$ pin, or either C1OUT or C2OUT is high
110 = VIL on $\overline{FLT0}$ pin or comparator C2OUT output is high
101 = VIL on $\overline{FLT0}$ pin or comparator C1OUT output is high
100 = VIL on $\overline{FLT0}$ pin
011 = Either C1OUT or C2OUT is high
010 = Comparator C2OUT output is high
001 = Comparator C1OUT output is high
000 = Auto-shutdown is disabled

bit 3-2 **PSSxAC<1:0>:** PxA and PxC Pins Shutdown State Control bits
1x = PxA and PxC pins tri-state
01 = Drive pins PxA and PxC to '1'
00 = Drive pins PxA and PxC to '0'

bit 1-0 **PSSxBD<1:0>:** PxB and PxD Pins Shutdown State Control bits
1x = PxB and PxD pins tri-state
01 = Drive pins PxB and PxD to '1'
00 = Drive pins PxB and PxD to '0'

Note 1: The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

2: Writing to the ECCPxASE bit is disabled while an auto-shutdown condition persists.

3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

Register 60-4: ECCPxDEL: ECCPx Enhanced PWM Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxRSEN	PxDC6	PxDC5	PxDC4	PxDC3	PxDC2	PxDC1	PxDC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **PxRSEN:** PWM Restart Enable bit

1 = Upon auto-shutdown, the ECCPxASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically

0 = Upon auto-shutdown, ECCPxASE must be cleared by software to restart the PWM

bit 6-0 **PxDC<6:0>:** PWM Delay Count bits

PxDCn = Number of FCY (FOSC/2) cycles between the scheduled time when a PWM signal **should** transition active and the **actual** time it transitions active.

Register 60-5: PSTRxCON: Pulse Steering Control Register for ECCPx

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
CMPL1	CMPL0	—	STRSYNC	STRD(1)	STRC(1)	STRB(1)	STRA(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **CMPL<1:0>:** Complementary Mode Output Assignment Steering Sync bits
11 = PxA and PxD are the complementary pair
10 = PxA and PxC are the complementary pair
01 = PxA and PxB are the complementary pair
00 = Complementary output assignment is disabled; the STRD:STRA bits are used to determine Steering mode

bit 5 **Unimplemented:** Read as '0'

bit 4 **STRSYNC:** Steering Sync bit
1 = Output steering update occurs on the next PWM period
0 = Output steering update occurs at the beginning of the instruction cycle boundary

bit 3 **STRD:** Steering Enable D bit(1)
1 = PxD pin has the PWM waveform with polarity control from CCPxM<1:0>
0 = PxD pin is assigned to port pin

bit 2 **STRC:** Steering Enable C bit(1)
1 = PxC pin has the PWM waveform with polarity control from CCPxM<1:0>
0 = PxC pin is assigned to port pin

bit 1 **STRB:** Steering Enable B bit(1)
1 = PxB pin has the PWM waveform with polarity control from CCPxM<1:0>
0 = PxB pin is assigned to port pin

bit 0 **STRA:** Steering Enable A bit(1)
1 = PxA pin has the PWM waveform with polarity control from CCPxM<1:0>
0 = PxA pin is assigned to port pin

Note 1: The PWM Steering mode is available only when CCPxM<3:2> = 11 and PxM<1:0> = 00.

Register 60-6: CCPTMRS0: CCP Timer Select Control Register 0 (Example)(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C3TSEL1	C3TSEL0	—	C2TSEL1	C2TSEL0	C1TSEL2	C1TSEL1	C1TSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **C3TSEL<1:0>:** CCP3 Timer Selection bits
1x = Reserved; do not use
01 = CCP3 uses TMR3/TMR4
00 = CCP3 uses TMR3/TMR2

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **C2TSEL<1:0>:** CCP2 Timer Selection bits
1x = Reserved; do not use
01 = CCP2 uses TMR3/TMR4
00 = CCP2 uses TMR3/TMR2

bit 2-0 **C1TSEL<2:0>:** ECCP1 Timer Selection bits
1xx = Reserved; do not use
01x = Reserved; do not use
001 = ECCP1 uses TMR3/TMR4
000 = ECCP1 uses TMR3/TMR2

Note 1: This hypothetical configuration is based on a device with three CCP modules (one of which is an ECCP) and three 8/16-bit timers. Actual devices may vary substantially. Refer to the device data sheet for a specific family for the actual number of registers and their bit configuration.

60.3 MODULE CONFIGURATION

60.3.1 Timer Resources and Selection

The CCP modules may utilize any of the general purpose, 8/16-bit timers available on the microcontroller. Timer1, which can only operate as a 16-bit timer, is not available to CCP modules.

In general, the only limitation is that a module operating in one of the PWM modes must use a timer with its own period register; in standard device nomenclature, these are even numbered timers. In contrast, modules operating in Capture and Compare mode must use one of the odd numbered timers, which are configurable as 16-bit timers. This is summarized in Table 60-1.

Table 60-1: Examples of CCP/Timer Resource Pairing Options

CCP Mode	Timer Resource(1)
Capture	Timer3, Timer 5...
Compare	
PWM	Timer2, Timer4...

Note 1: Not all of the timers listed here may be available in all devices. Refer to the specific device data sheet for details.

The assignment of a particular timer to a module is determined by the Timer to CCP enable bits in the CCPTMRSn registers. Timers are assigned in fixed pairs to a CCP module, with one odd timer (for Capture and Compare) and one even timer (for PWM), selected by a particular bit configuration.

In theory, all of the modules for a particular device may be active at once and may share the same timer resource if they are configured to operate in the same mode (Capture/Compare or PWM), at the same time. In actual implementation, however, some CCP modules may be restricted to only selecting from one or two of the available timers. As a rule, ECCP modules will have more timer configuration options available for selection.

The number and configuration of the CCPTMRSn registers are dependent on the number of CCP and ECCP modules, and the number of timers; as such, they are always device-specific. Refer to the particular device data sheet for specific information on CCP, Timer and CCPTMRSn register implementation.

Note: Throughout this section, generic references are used for timers. “Timer a (TMRa)” and “Timer b (TMRb)” are used to represent odd numbered timers. “Timer c (TMRc)” represents even numbered timers.

60.3.2 CCP I/O Configuration

As PIC24 devices allow a peripheral to control a pin’s direction, rather than using the pin’s corresponding TRIS bit, configuring the TRIS bit will not ensure the proper pin function. A suggested start-up sequence for using the CCP module is as follows:

1. Disable the module by writing ‘0000’ to CCPxM<3:0> (CCPxCON<3:0>).
1. Set the TRIS bit on the CCPx pin, and any Px pins (for Enhanced PWM modes). This configures the pins as inputs.
2. Write any initial values to CCPRxL and CCPRxH. For Enhanced PWM modes, configure ECCPxCON<7:6> as well.
3. Enable the module by writing the appropriate mode select value to CCPxM<3:0>. When the module is enabled, it will assert control of the pins in the proper data direction.

The Enhanced CCP module may have up to four PWM outputs, depending on the selected operating mode. These outputs are designated PxA through PxD. The outputs that are active depend on the ECCP operating mode selected. The pin assignments are summarized in Table 60-3. To configure the I/O pins as PWM outputs, the proper PWM mode must be selected by setting the PM<1:0> and CCPxM<3:0> bits.

60.4 CAPTURE MODE

In Capture mode, the CCPRxH:CCPRxL register pair captures the 16-bit value of the selected Timer register when an event occurs on the CCPx pin. An event is defined as one of the following:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

The event is selected by the CCP Mode Select bits, CCPxM<3:0> (CCPxCON<3:0>). When a capture is made, the CCP Interrupt Request Flag bit, CCPxIF, is set. (It must be cleared in software.) If another capture occurs before the value in CCPRx is read, the old captured value is overwritten by the new captured value.

Figure 60-1 shows the Capture mode block diagram.

60.4.1 CCP Pin Configuration

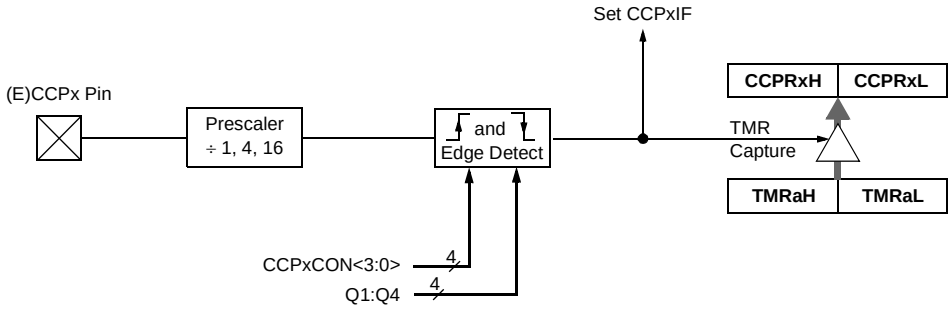
In Capture mode, the appropriate CCPx pin should be configured as an input by setting the corresponding TRIS direction bit.

60.4.2 Timer Mode Selection

To be used for the Capture feature, the selected timers must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work.

The timer to be used with each CCP module is selected in the CCPTMRSx registers (see **Section 60.3.1 "Timer Resources and Selection"** for more information). The timers available to each CCP module are device-specific. Refer to the particular device data sheet for specific information.

Figure 60-1: Generic Capture Mode Block Diagram



Note: TMRa and TMRb are generic references. The timers available to a specific CCP module are device-specific. See **Section 60.3.1 "Timer Resources and Selection"** for more information.

60.4.3 CCP Prescaler

There are four prescaler settings in Capture mode. They are specified as part of the operating mode selected by the CCPx Mode Select bits (CCPxM<3:0>). Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Doing that will also not clear the prescaler counter – meaning the first capture may be from a non-zero prescaler. Example 60-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the “false” interrupt.

Example 60-1: Changing Between Capture Prescalers

```
CCP4CON = 0;              // Turn CCP4 module off
CCP4CON = NEW_CAPT_PS;    // Load new prescaler mode value and turn CCP4 ON
```

60.4.4 Software Interrupt

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit clear to avoid false interrupts and should clear the CCPxIF interrupt flag when changing Capture modes.

60.5 COMPARE MODE

In Compare mode, the 16-bit CCPRx register value is constantly compared against the selected timer's register pair value. When a match occurs, the CCPx pin can be:

- Driven high
- Driven low
- Toggled (high-to-low or low-to-high)
- Unchanged (that is, reflecting the state of the I/O latch)

The action on the pin is based on the value of the CCPx Mode Select bits (CCPxM<3:0>). At the same time, the CCPx Interrupt Flag bit, CCPxIF, is set.

Figure 60-2 shows the Compare mode block diagram.

60.5.1 CCP Pin Configuration

The CCP module automatically configures the pin as an output when the module is enabled. See **Section 60.3.2 "CCP I/O Configuration"** for details.

60.5.2 Timer Mode Selection

To be used for the Compare features, the selected timers must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the Compare operation may not work.

60.5.3 Special Event Trigger

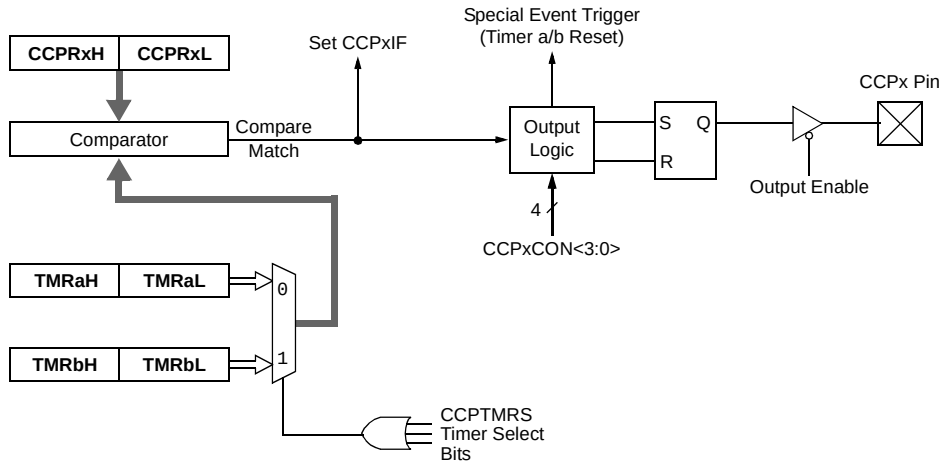
Both CCP modules are equipped with a Special Event Trigger. This is an internal hardware signal generated in Compare mode to trigger actions by other modules. The Special Event Trigger is enabled by selecting the Compare Special Event Trigger mode (CCPxM<3:0> = 1011).

For either CCP module, the Special Event Trigger resets the Timer register pair for whichever timer resource is currently assigned as the module's time base. This allows the CCPRx registers to serve as a programmable period register for either timer.

60.5.4 Software Interrupt Mode

When the Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the CCPx pin is not affected. Only a CCP interrupt is generated, if enabled, and the CCPxIE bit is set.

Figure 60-2: Generic Compare Mode Block Diagram



Note: TMRa and TMRb are generic references; the timers available to a specific CCP module are device-specific. See **Section 60.3.1 "Timer Resources and Selection"** for more information.

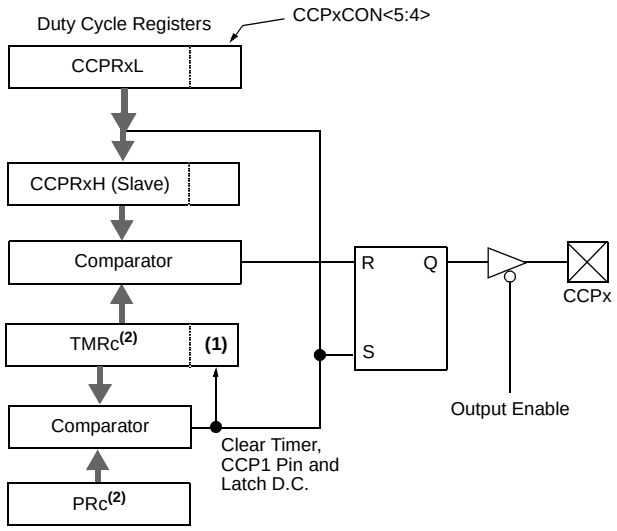
60.6 PWM MODE

In Pulse-Width Modulation (PWM) mode, the CCP pin produces a PWM output of up to a 10-bit resolution. Figure 60-3 shows a simplified block diagram of the module in PWM mode.

A PWM output (Figure 60-4) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 60.6.3 "Setup for PWM Operation"**.

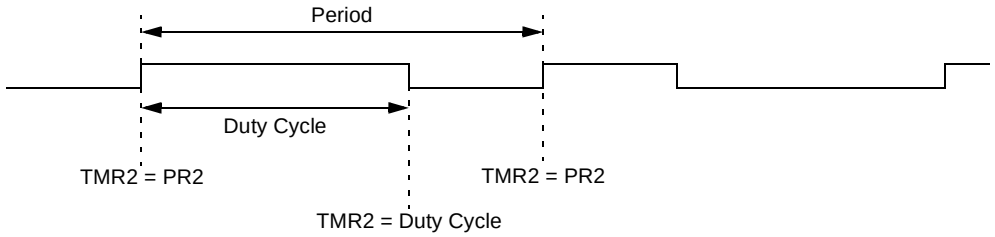
Figure 60-3: Simplified PWM Block Diagram



Note 1: The 8-bit TMRc value is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler, to create the 10-bit time base.

2: TMRc and PRc are generic timer references. See **Section 60.3.1 "Timer Resources and Selection"** for more information.

Figure 60-4: PWM Output



60.6.1 PWM Period

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

Equation 60-1:

$$\text{PWM Period} = [(\text{PR2}) + 1] \cdot 2 \cdot T_{OSC} \cdot (\text{TMR2 Prescale Value})$$

The PWM frequency is defined as 1/[PWM period]. When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP4 pin is set (Exception: If the PWM Duty Cycle = 0%, the CCPx pin will not be set)
- The PWM duty cycle is latched from CCPRxL into CCPRxH

Note:	The Timer2 postscalers are not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

60.6.2 PWM Duty Cycle

The PWM duty cycle is specified by writing to the CCPR4L register and to the CCP4CON<5:4> bits. Up to 10-bit resolution is available. The CCPR4L contains the eight MSbs and the CCP4CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR4L:CCP4CON<5:4>. The following equations are used to calculate the PWM duty cycle as a percentage or as time:

Equation 60-2:

PWM Duty Cycle (%) = (CCPRxL:CCPxCON<5:4>)/(4 • PR2)

PWM Duty Cycle (time in s) = (CCPRxL:CCPxCON<5:4>) • TOSC/2 • (TMR2 Prescale Value)

CCPR4L and CCP4CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR4H until after a match between PR2 and TMR2 occurs (that is, the period is complete). In PWM mode, CCPR4H is a read-only register.

The CCPR4H register and a two-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPR4H and two-bit latch match TMR2, concatenated with an internal two-bit Q clock or two bits of the TMR2 prescaler, the CCP4 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is shown in the following equation:

Equation 60-3:

$$\text{PWM Resolution (max)} = \frac{\log\left(\frac{2 \cdot \text{Fosc}}{\text{FPWM}}\right)}{\log(2)} \text{bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the CCP4 pin will not be cleared.

Table 60-2: Example PWM Frequencies and Resolutions at 32 MHz

PWM Frequency	3.906 kHz	62.5 kHz	125 kHz	250 kHz	500 kHz	1 MHz
Timer Prescaler	16	1	1	1	1	1
PR2 Value	FFh	FFh	7Fh	3Fh	1Fh	0Fh
Maximum Resolution (bits)	10	10	9	8	7	6

60.6.3 Setup for PWM Operation

To configure the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPRxL register and CCPxCON<5:4> bits.
3. Set the TMR2 prescale value, then enable Timer2 by writing to T2CON.
4. Configure the CCPxCON register for PWM operation.

60.7 ENHANCED PWM MODE

In ECCP modules, the Enhanced PWM mode can generate a PWM signal on up to four different output pins, with up to 10 bits of resolution. It can do this through four different PWM Output modes:

- Single PWM mode
- Half-Bridge PWM mode
- Full-Bridge PWM, Forward mode
- Full-Bridge PWM, Reverse mode

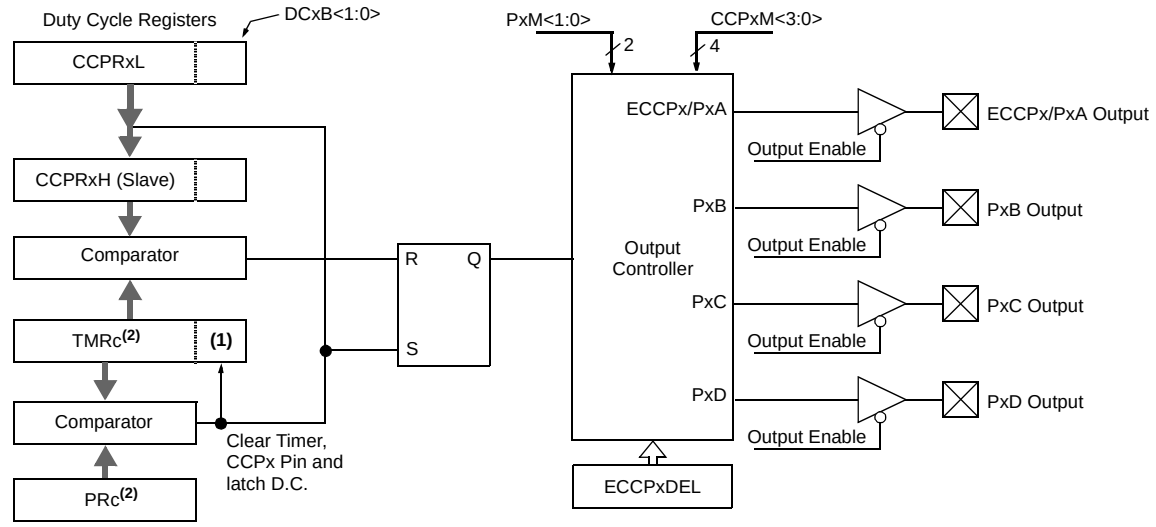
To select an Enhanced PWM mode, the PM<1:0> bits (ECCPxCON<7:6>) must be set appropriately.

The PWM outputs are multiplexed with I/O pins, and are designated PxA, PxB, PxC and PxD. The polarity of the PWM pins is configurable and is selected by setting the appropriate CCPxM bits in the ECCPxCON register. Table 60-3 provides the pin assignments for each Enhanced PWM mode.

Figure 60-5 provides an example of a simplified block diagram of the Enhanced PWM module.

Note:	To prevent the generation of an incomplete waveform when the PWM is first enabled, the ECCP module waits until the start of a new PWM period before generating a PWM signal.

Figure 60-5: Simplified Block Diagram of Enhanced PWM Mode



Note 1: The 8-bit TMR2 value is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler, to create the 10-bit time base.
2: TMRc and PRc are generic timer references. See **Section 60.3.1 "Timer Resources and Selection"** for more information.

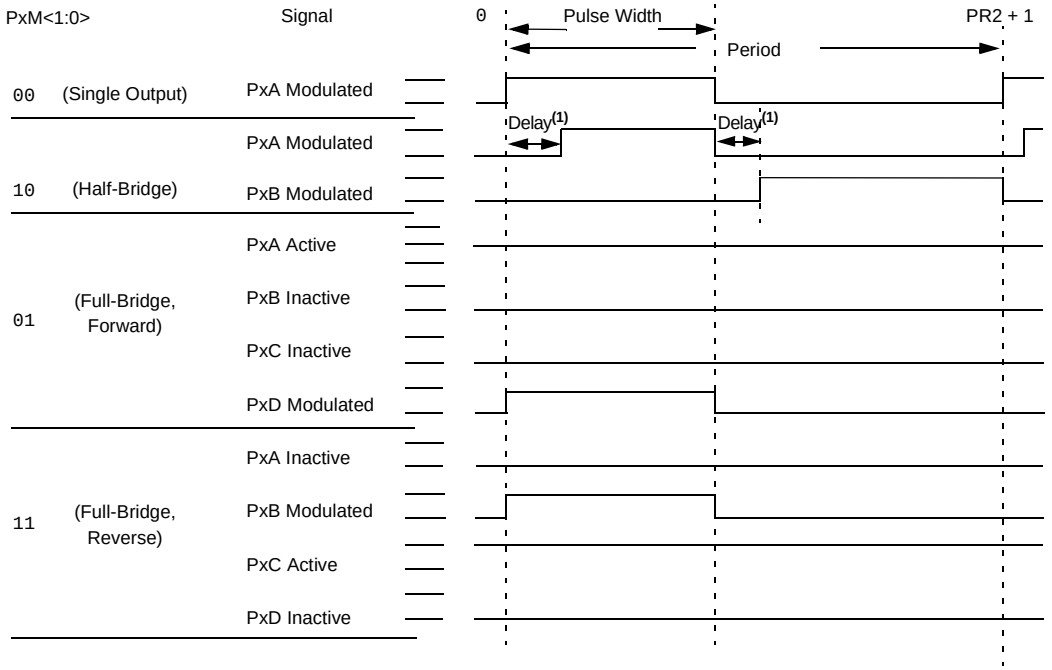
Table 60-3: Pin Assignments for Various PWM Enhanced Modes

ECCP Mode	PxM<1:0>	PxA	PxB	PxC	PxD
Single	00	Yes(1)	Yes(1)	Yes(1)	Yes(1)
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

Note 1: Individual outputs in Single mode are enabled by pulse steering, controlled by the PSTRxCON register (Register 60-5).

Note 1:	The STR<D:A> bits in the PSTRxCON register, for each PWM output, must be configured appropriately.
2:	Any pin not used by an Enhanced PWM mode is available for alternate pin functions.

Figure 60-6: Enhanced PWM Output Relationships (Active-High State) Example

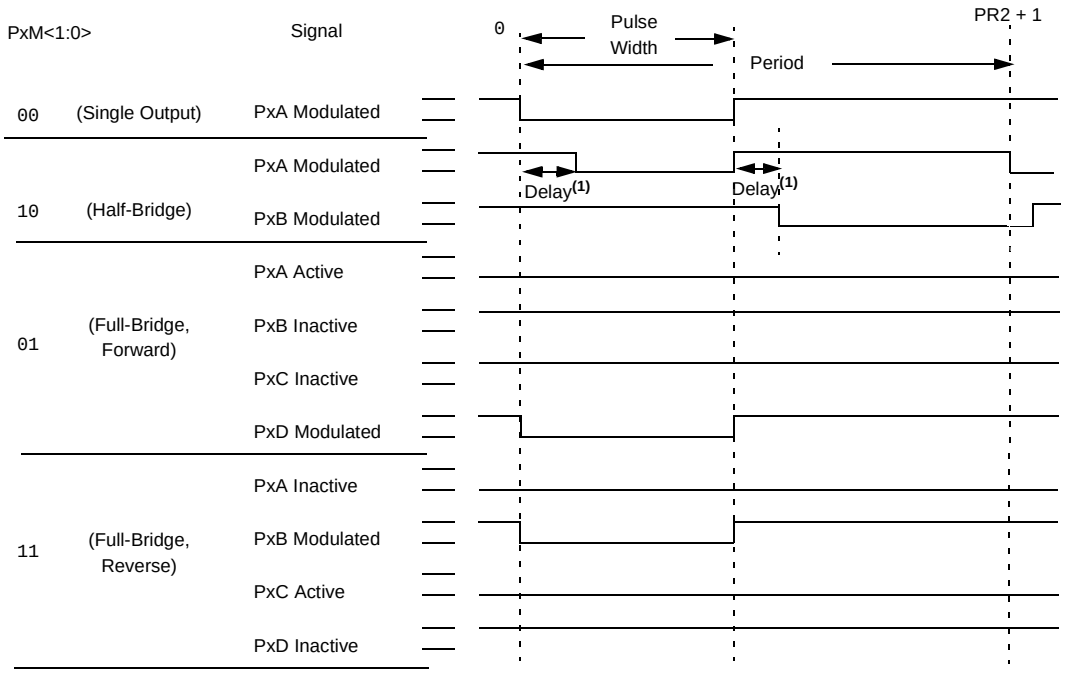


Relationships:

- Period = 2 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc/2 * (CCPRxL<7:0>:ECCPxCON<5:4>) * (TMR2 Prescale Value)
- Delay = 2 * Tosc * (ECCPxDEL<6:0>)

Note 1: Dead-band delay is programmed using the ECCPxDEL register (see **Section 60.7.6 "Programmable Dead-Band Delay Mode"**).

Figure 60-7: Enhanced PWM Output Relationships (Active-Low State) Example



Relationships:

- Period = 2 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc/2 * (CCPRxL<7:0>:ECCPxCON<5:4>) * (TMR2 Prescale Value)
- Delay = 2 * Tosc * (ECCPxDEL<6:0>)

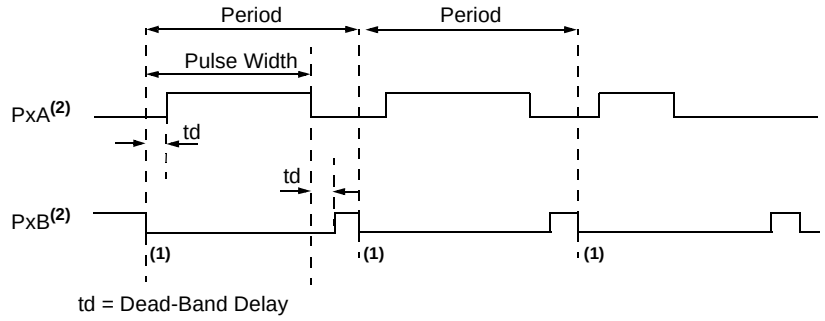
Note 1: Dead-band delay is programmed using the ECCPxDEL register (see **Section 60.7.6 "Programmable Dead-Band Delay Mode"**).

60.7.1 Half-Bridge Mode

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the PxA pin, while the complementary PWM output signal is output on the PxB pin (see Figure 60-8). This mode can be used for half-bridge applications, or for full-bridge applications, where four power switches are being modulated with two PWM signals (Figure 60-9).

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in half-bridge power devices. The value of the PxDC<6:0> bits of the ECCPxDEL register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. For more details on the dead-band delay operations, see **Section 60.7.6 "Programmable Dead-Band Delay Mode"**.

Figure 60-8: Example of Half-Bridge PWM Output

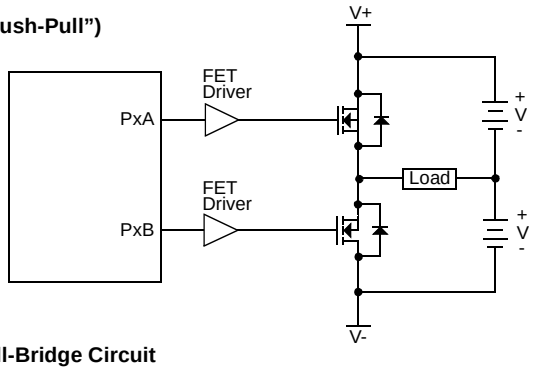


Note 1: At this time, the TMR2 register is equal to the PR2 register.

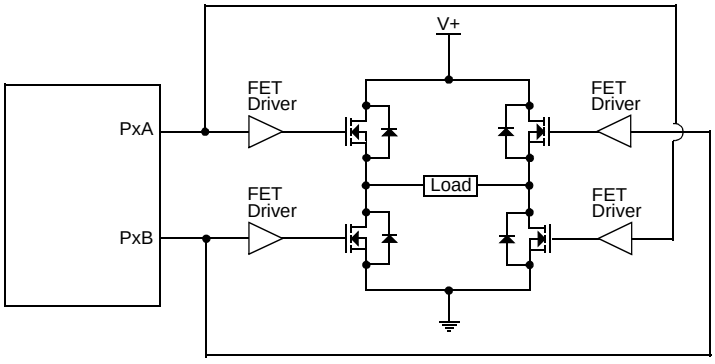
2: Output signals are shown as active-high.

Figure 60-9: Example of Half-Bridge Applications

Standard Half-Bridge Circuit ("Push-Pull")



Half-Bridge Output Driving a Full-Bridge Circuit



60.7.2 Full-Bridge Mode

In Full-Bridge mode, all four pins are used as outputs. An example of a full-bridge application is provided in Figure 60-10.

In the Forward mode, the PxA pin is driven to its active state and the PxD pin is modulated, while the PxB and PxC pins are driven to their inactive state, as shown in Figure 60-11.

In the Reverse mode, the PxC pin is driven to its active state and the PxB pin is modulated, while the PxA and PxD pins are driven to their inactive state, as shown in Figure 60-11.

Figure 60-10: Example of Full-Bridge Application

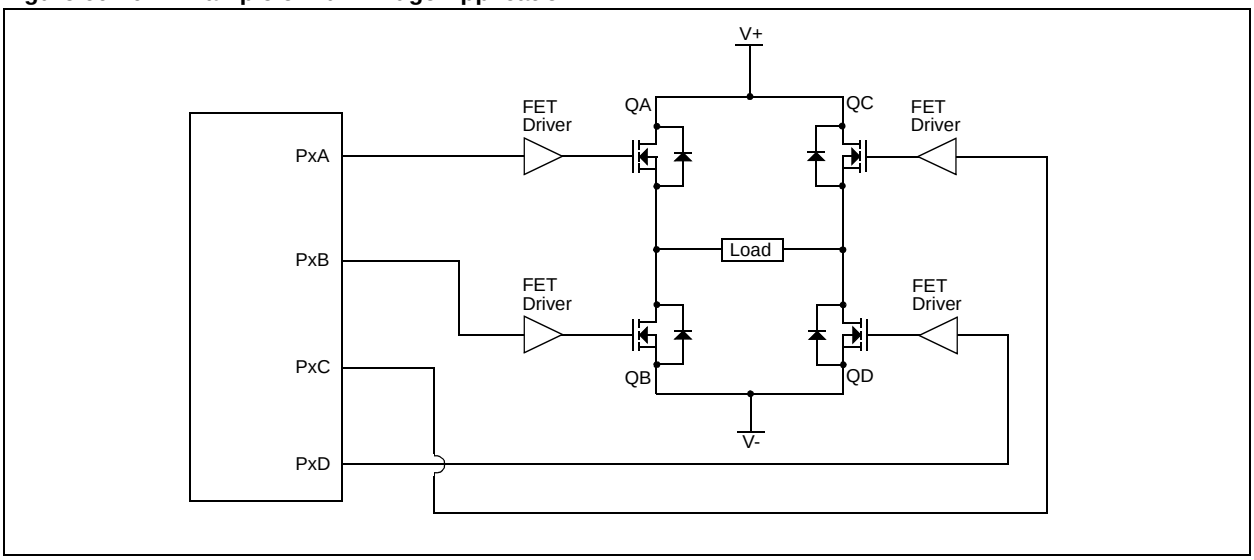
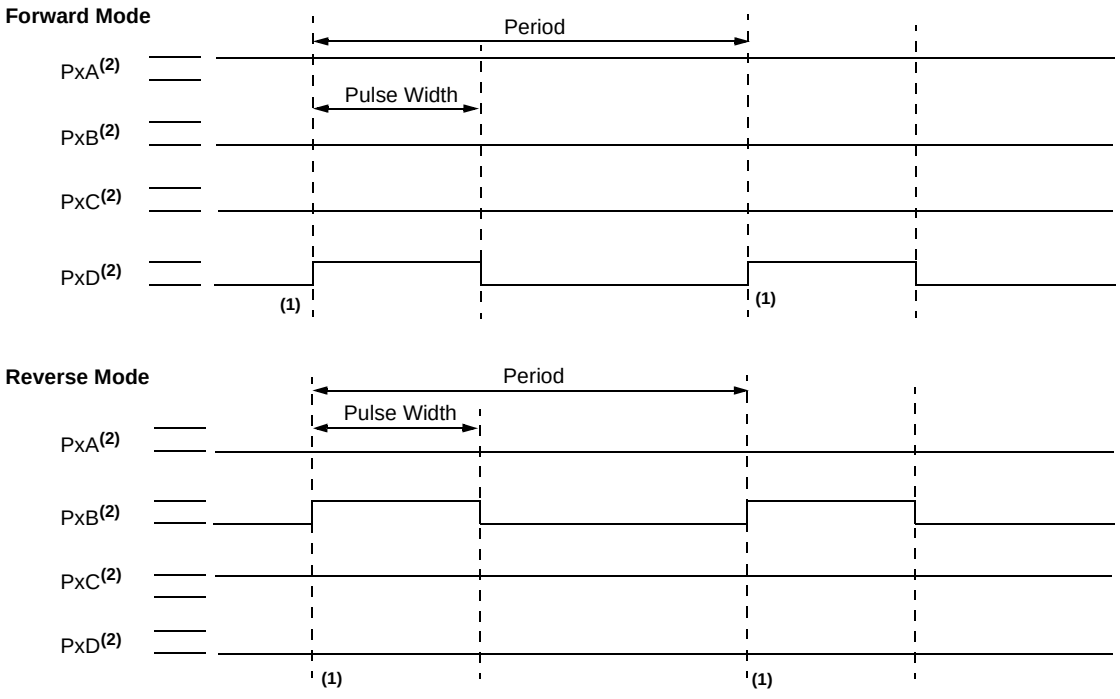


Figure 60-11: Example of Full-Bridge PWM Output



Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: The output signal is shown as active-high.

60.7.2.1 DIRECTION CHANGE IN FULL-BRIDGE MODE

In the Full-Bridge mode, the PxM1 bit in the ECCPxCON register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle.

A direction change is initiated in software by changing the PxM1 bit of the ECCPxCON register. The following sequence occurs prior to the end of the current PWM period:

- The modulated outputs (PxB and PxD) are placed in their inactive state.
- The associated unmodulated outputs (PxA and PxC) are switched to drive in the opposite direction.
- PWM modulation resumes at the beginning of the next period.

For an illustration of this sequence, see Figure 60-12.

The Full-Bridge mode does not provide a dead-band delay. As one output is modulated at a time, a dead-band delay is generally not required. There is a situation where a dead-band delay is required. This situation occurs when both of the following conditions are true:

- The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
- The turn-off time of the power switch, including the power device and driver circuit, is greater than the turn-on time.

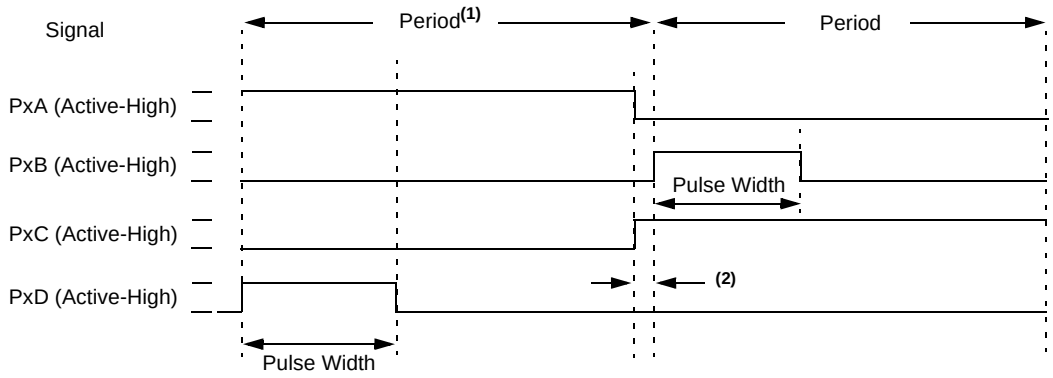
Figure 60-13 shows an example of the PWM direction changing from forward to reverse at a near 100% duty cycle. In this example, at time t1, the PxA and PxD outputs become inactive, while the PxC output becomes active. Since the turn-off time of the power devices is longer than the turn-on time, a shoot-through current will flow through power devices, QC and QD (see Figure 60-10), for the duration of 't'. The same phenomenon will occur to power devices, QA and QB, for PWM direction change from reverse to forward.

If an application requires changing PWM direction at high duty cycle, two possible solutions for eliminating the shoot-through current are:

- Reduce PWM duty cycle for one PWM period before changing directions.
- Use switch drivers that can drive the switches off faster than they can drive them on.

Other options to prevent shoot-through current may exist.

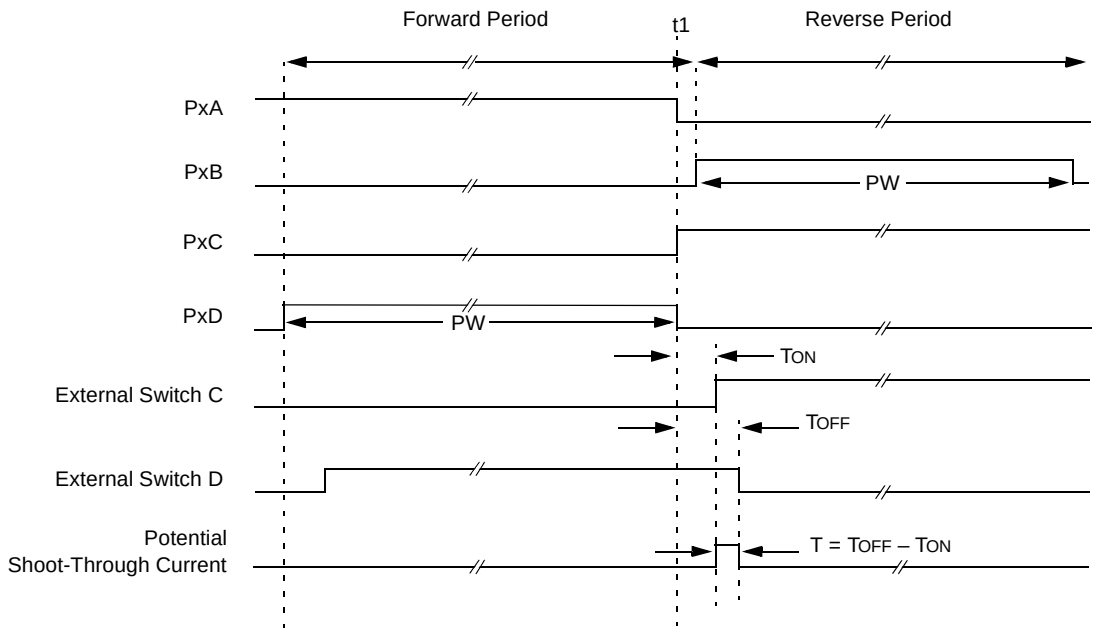
Figure 60-12: Example of PWM Direction Change



Note 1: The direction bit, PxM1 of the ECCPxCON register, is written any time during the PWM cycle.

2: When changing directions, the PxA and PxC signals switch before the end of the current PWM cycle. The modulated PxB and PxD signals are inactive at this time. The length of this time is: (1/FOSC) • TMR2 Prescale Value.

Figure 60-13: Example of PWM Direction Change at Near 100% Duty Cycle



Note 1: All signals are shown as active-high.

2: TON is the turn-on delay of power switch, QC, and its driver.

3: TOFF is the turn-off delay of power switch, QD, and its driver.

60.7.3 Start-up Considerations

When any PWM mode is used, the application hardware must use the proper external pull-up and/or pull-down resistors on the PWM output pins.

Note:	When the microcontroller is released from Reset, all of the I/O pins are in the high-impedance state. The external circuits must keep the power switch devices in the OFF state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s).

The PxM<1:0> bits of the ECCPxCON register allow the user to choose whether the PWM output signals are active-high or active-low for each pair of PWM output pins (PxA/PxC and PxB/PxD). The PWM output polarities must be selected before the PWM pin output drivers are enabled. Changing the polarity configuration while the PWM pin output drivers are enabled is not recommended, since it may result in damage to the application circuits.

The PxA, PxB, PxC and PxD output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pin output drivers at the same time as the Enhanced PWM modes may cause damage to the application circuit. The Enhanced PWM modes must be enabled in the proper Output mode and complete a full PWM cycle before enabling the PWM pin output drivers. The completion of a full PWM cycle is indicated by the T2IF or T4IF bit of the IFS0 or IFS1 register being set, as the second PWM period begins.

60.7.4 Enhanced PWM Auto-Shutdown Mode

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the ECCPxAS<6:4> bits. A shutdown event may be generated by:

- A logic '0' on the pin that is assigned to the $\overline{\text{FLT0}}$ input function
- Comparator C1
- Comparator C2
- Setting the ECCPxASE bit in firmware

A shutdown condition is indicated by the ECCPxASE (Auto-Shutdown Event Status) bit (ECCPxAS<7>). If the bit is set to '0', the PWM pins are operating normally. If the bit is set to '1', the PWM outputs are in the shutdown state.

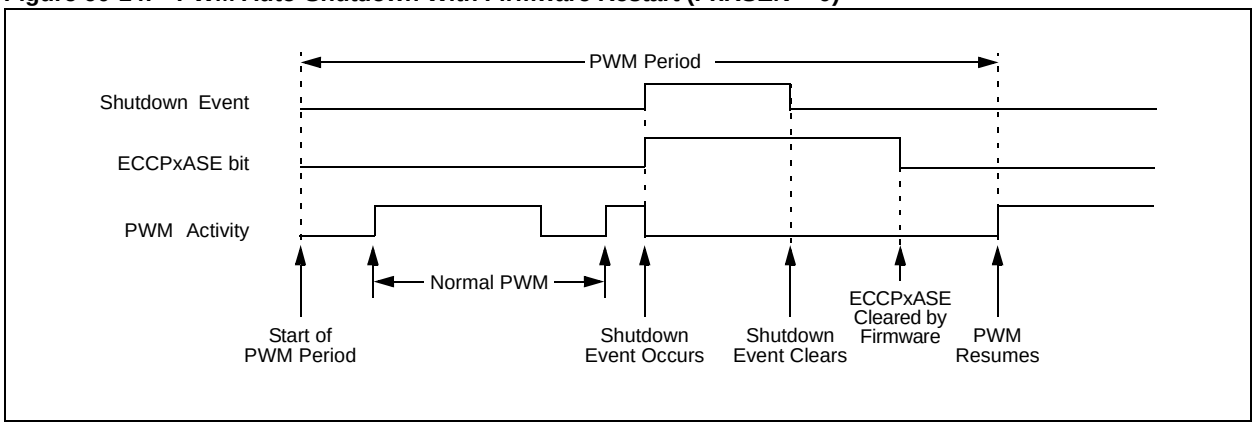
When a shutdown event occurs, two things happen:

- The ECCPxASE bit is set to '1'. The ECCPxASE bit will remain set until cleared in firmware or an auto-restart occurs. (See **Section 60.7.5 "Auto-Restart Mode"**.)
- The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs (PxA/PxC) and (PxB/PxD). The state of each pin pair is determined by the PSSxAC and PSSxBD bits (ECCPxAS<3:0>).

Each pin pair may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

Figure 60-14: PWM Auto-Shutdown With Firmware Restart (PxRSEN = 0)



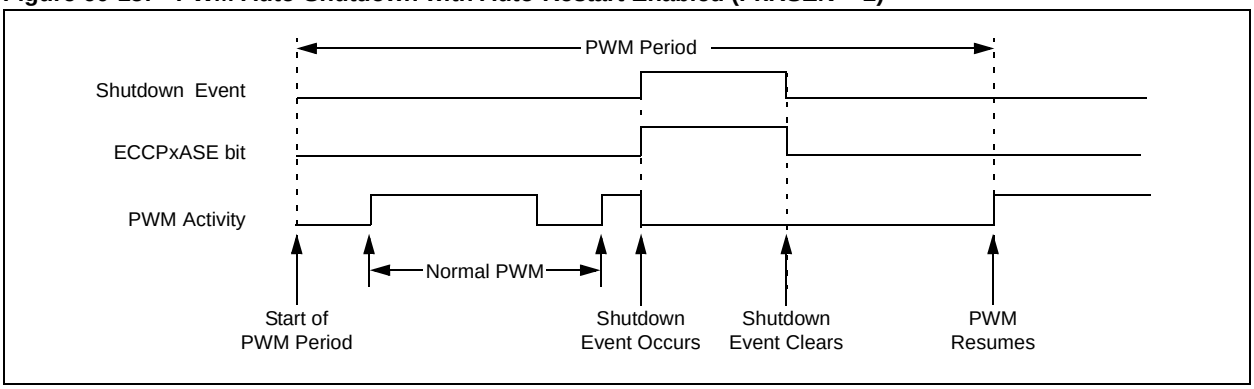
60.7.5 Auto-Restart Mode

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PxRSEN bit (ECCPxDEL<7>).

If auto-restart is enabled, the ECCPxASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPxASE bit will be cleared via hardware and normal operation will resume.

The module will wait until the next PWM period begins before re-enabling the output pin. This behavior allows the auto-shutdown with auto-restart features to be used in applications based on the current mode of PWM control.

Figure 60-15: PWM Auto-Shutdown with Auto-Restart Enabled (PxRSEN = 1)



60.7.6 Programmable Dead-Band Delay Mode

In half-bridge applications (see Figure 60-9), where all power switches are modulated at the PWM frequency, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on and the other turned off), both switches may be on for a short period until one switch completely turns off. During this brief interval, a very high current (shoot-through current) will flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In Half-Bridge mode, a digitally programmable, dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state (interval td, Figure 60-8). The lower seven bits of the associated ECCPxDEL register (Register 60-4) set the delay period in terms of microcontroller instruction cycles (TCY or 2 TOSC).

60.7.7 Pulse Steering Mode

In Single Output mode, pulse steering allows any of the PWM pins to be the modulated signal. Additionally, the same PWM signal can simultaneously be available on multiple pins.

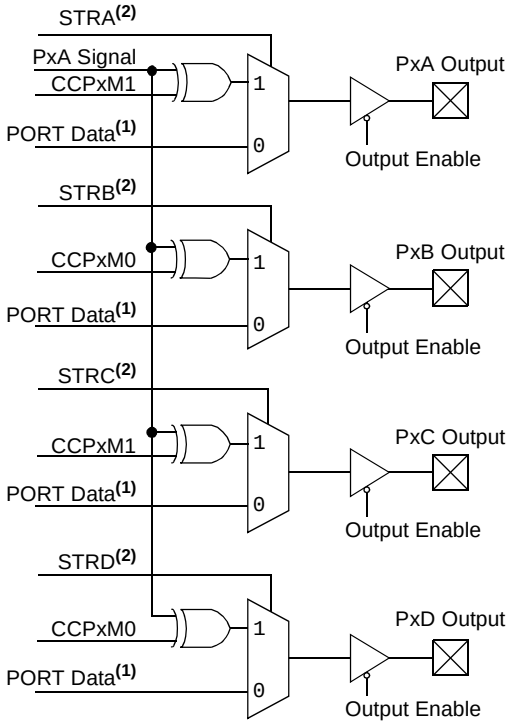
Once the Single Output mode is selected (CCPxM<3:2> = 11 and PxM<1:0> = 00 of the ECCPxCON register), the user firmware can bring out the same PWM signal to one, two, three or four output pins by setting the appropriate STR<D:A> bits (PSTRxCON<3:0>), as provided in Table 60-3.

Note:	The associated STR<D:A> bits in the PSTRxCON register must be set to output ('0') to enable the pin output driver, in order to see the PWM signal on the pin.

While the PWM Steering mode is active, the CCPxM<1:0> bits (ECCPxCON<1:0>) select the PWM output polarity for the Px<D:A> pins.

The PWM auto-shutdown operation also applies to PWM Steering mode, as described in **Section 60.7.4 "Enhanced PWM Auto-Shutdown Mode"**. An auto-shutdown event will only affect pins that have PWM outputs enabled.

Figure 60-16: Simplified Steering Block Diagram



Note 1: Port outputs are configured as displayed when the ECCPxCON register bits, PxM<1:0> = 00 and CCPxM<3:2> = 11.
2: Single PWM output requires setting at least one of the STR<D:A> bits.

60.7.7.1 STEERING SYNCHRONIZATION

The STRSYNC bit of the PSTRxCON register gives the user two choices for when the steering event will happen. When the STRSYNC bit is '0', the steering event will happen at the end of the instruction that writes to the PSTRxCON register. In this case, the output signal at the Px<D:A> pins may be an incomplete PWM waveform. This operation is useful when the user firmware needs to immediately remove a PWM signal from the pin.

When the STRSYNC bit is '1', the effective steering update will happen at the beginning of the next PWM period. In this case, steering on/off the PWM output will always produce a complete PWM waveform.

Figure 60-17 and Figure 60-18 illustrate the timing diagrams of the PWM steering, depending on the STRSYNC setting.

Figure 60-17: Example of Steering Event at End of Instruction (STRSYNC = 0)

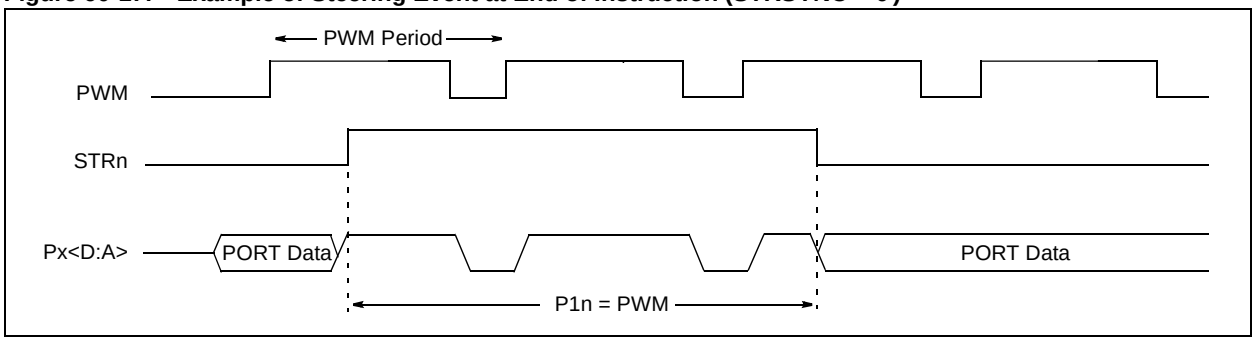
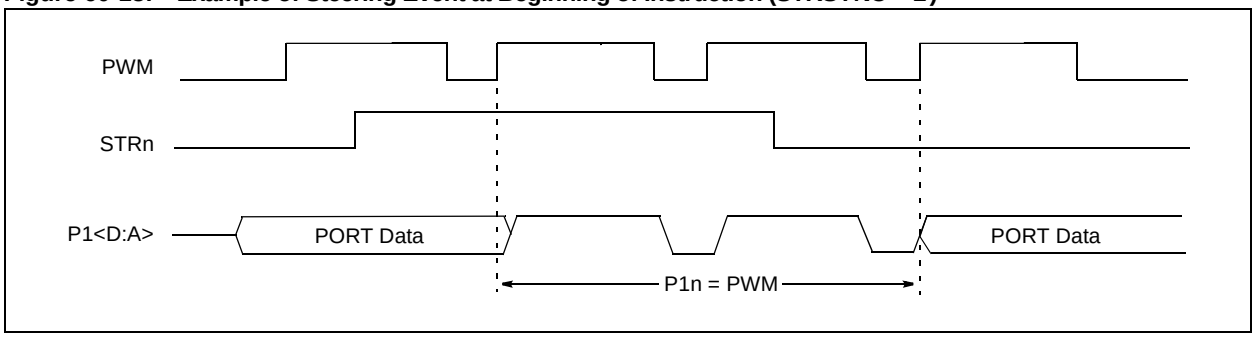


Figure 60-18: Example of Steering Event at Beginning of Instruction (STRSYNC = 1)



60.8 OPERATION IN POWER-MANAGED MODES

In Sleep mode, all clock sources are disabled. Timers will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, it will continue from this state. If Two-Speed Start-ups are enabled, the initial start-up frequency of the FRC oscillator may not be the same as the primary oscillator.

In Idle mode, the primary clock will continue to clock the module without change.

60.8.1 Operation with Fail-Safe Clock Monitor (FSCM)

If the Fail-Safe Clock Monitor (FSCM) is enabled, a clock failure will force the device to run from the FRC oscillator and also set the OSCFAIL bit. The module will then be clocked from the internal oscillator clock source, which may have a different clock frequency than the primary clock.

60.9 EFFECTS OF A RESET

Any Reset event will force all I/O ports to Input mode and the CCP registers to their Reset states.

60.10 REGISTER MAPS

Summaries of the registers associated with the PIC24F Capture/Compare/PWM (CCP and ECCP) modules are provided in Table 60-4 and Table 60-5.

Table 60-4: Generic CCP Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
CCPxCON	—	—	—	—	—	—	—	—	—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0	0000
CCPRxL	—	—	—	—	—	—	—	—	Capture/Compare/PWM Register Low Byte								0000
CCPRxH	—	—	—	—	—	—	—	—	Capture/Compare/PWM Register High Byte								0000
CCPTMRS0	—	—	—	—	—	—	—	—	C3TSEL1	C3TSEL0	—	C2TSEL1	C2TSEL0	C1TSEL2	C1TSEL1	C1TSEL0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Table 60-5: Generic ECCP Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
ECCPxCON	—	—	—	—	—	—	—	—	PxM1	PxM0	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0	0000
ECCPRxL	—	—	—	—	—	—	—	—	Capture/Compare/PWM Register Low Byte								0000
ECCPRxH	—	—	—	—	—	—	—	—	Capture/Compare/PWM Register High Byte								0000
ECCPxDEL	—	—	—	—	—	—	—	—	PxRSEN	PxDC6	PxDC5	PxDC4	PxDC3	PxDC2	PxDC1	PxDC0	0000
ECCPxAS	—	—	—	—	—	—	—	—	ECCPxASE	ECCPxAS2	ECCPxAS1	ECCPxAS0	PSSxAC1	PSSxAC0	PSSxBD1	PSSxBD0	0000
PSTRxCON	—	—	—	—	—	—	—	—	CMPL1	CMPL0	—	STRSYNC	STRD	STRC	STRB	STRA	0001

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

60.11 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations.

The current application notes related to the Capture/Compare/PWM (CCP and ECCP) modules are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the PIC24F family of devices.

60.12 REVISION HISTORY

Revision A (November 2011)

Original version of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2009

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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