Section 59. General Purpose 8/16-Bit Timers

HIGHLIGHTS

This section of the manual contains the following major topics:

59.1 INTRODUCTION

PIC24F devices that use the MSSP and CCP/ECCP modules require dedicated 8-bit timers for the proper operation of these peripherals. To accomplish this, these devices replace many of the standard PIC24 16-bit timers with two or more 8-bit and 8/16-bit timers. These timers are substantially identical to those offered in PIC18 microcontrollers.

The 8-bit and 8/16-bit timers are instantiated in a specific manner. Even numbered timers (Timer2, Timer4, etc.) are simple 8-bit timers with programmable period registers; these are used as a clock source for the MSSP modules and the PWM mode of the CCP/ECCP modules. Odd numbered modules, above Timer1 (Timer3, Timer5, etc.), are 8/16-bit timers with user-configurable gating features, which are used for CCP/ECCP Capture and Compare modes. All even numbered timers are essentially identical to each other and all odd numbered timers are essentially identical to each other. The minor differences between timer modules of the same type are noted in the following sections.

Note:	All PIC24F devices require at least one standard 16-bit timer to maintain compatibility with other PIC24 family peripherals. For devices with multiple types of timers, Timer1 is always a standard PIC24 16-bit (“Type A”) timer. Timer1 is NOT available for use with MSSP or CCP/ECCP modules. See **Section 14.0 “Timers”** (DS39704) for a complete description of the module.

The timers are individually described in the following sections. For clarity, “Timer2” is used generically to describe all even numbered (8-bit) timers, and “Timer3” is used generically to describe all odd numbered (8/16-bit) timers. References to other timer numbers (e.g., Timer4) are used to indicate additional features implemented in only certain timers and not generically in all timers.

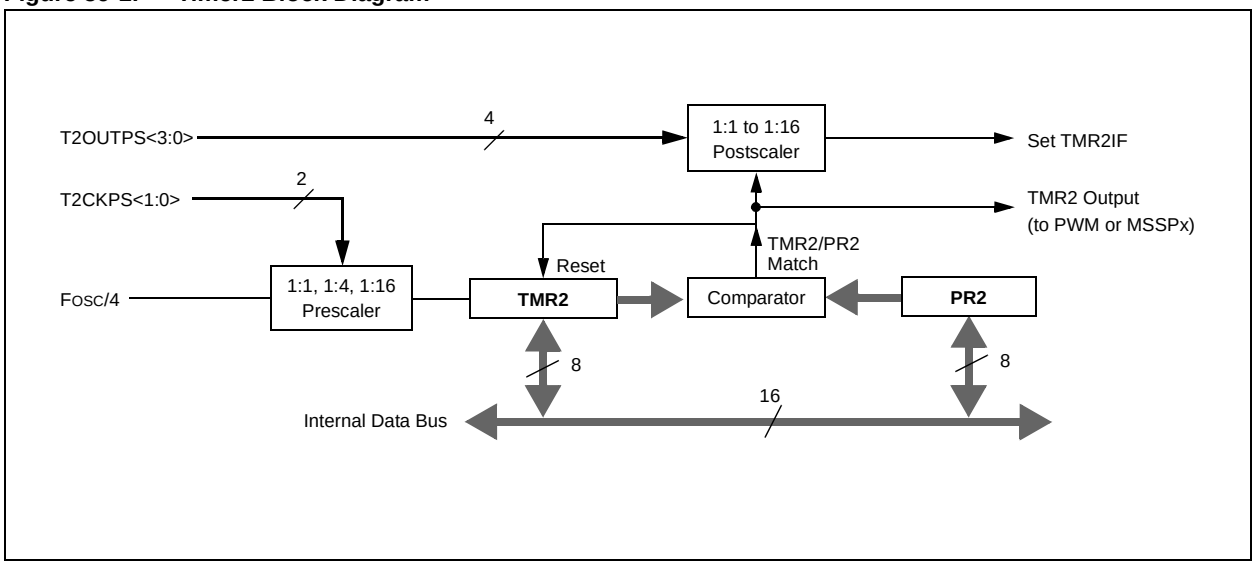
59.2 TIMER2 MODULE

The Timer2 module incorporates the following features:

- 8-Bit Timer and Period Registers (TMR2 and PR2, respectively)
- Readable and Writable (both registers)
- Software Programmable Prescaler (1:1, 1:4 and 1:16)
- Software Programmable Postscaler (1:1 through 1:16)
- Interrupt on TMR2 to PR2 Match
- Optional Use as the Shift Clock for the MSSP Modules

A simplified block diagram of the module is shown in Figure 59-1.

Figure 59-1: Timer2 Block Diagram



59.2.1 Registers

The Timer2 module uses three register: T2CON, TMR2 and PR2.

The module is controlled entirely through the T2CON register (Register 59-1), which enables or disables the timer and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

The TMR2 and PR2 registers contain the 8-bit timer/counter and 8-bit period register values, respectively. The values for TMR2 and PR2 are stored in the lower byte of the word-wide registers.

Register 59-1: T2CON: Timer2 Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-3 **T2OUTPS<3:0>:** Timer2 Output Postscale Select bits

0000 = 1:1 Postscale
0001 = 1:2 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2 **TMR2ON:** Timer2 On bit

1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
10 = Prescaler is 16

59.2.2 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock (FOSC/2). A 4-bit counter/prescaler on the clock input gives direct input, divide-by-4 and divide-by-16 prescale options. These are selected by the prescaler control bits, T2CKPS<1:0> (T2CON<1:0>). The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see **Section 59.2.3 "Timer2 Interrupt"**).

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR2 register
- A write to the T2CON register
- Any device Reset (Power-on Reset (POR), $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset (WDTR) or Brown-out Reset (BOR))

TMR2 is not cleared when T2CON is written.

59.2.3 Timer2 Interrupt

Timer2 can also generate an optional device interrupt. The Timer2 output signal (TMR2 to PR2 match) provides the input for the 4-bit output counter/postscaler. This counter generates the TMR2 Match Interrupt Flag, which is latched in T2IF. The interrupt is enabled by setting the TMR2 Match Interrupt Enable bit, T2IE.

A range of 16 postscaler options (from 1:1 through 1:16 inclusive) can be selected with the Timer2 Output Postscale Select bits, T2OUTPS<3:0> (T2CON<6:3>).

59.2.4 Timer2 Output

The unscaled output of TMR2 is available primarily to the ECCP modules, where it is used as a time base for operations in PWM mode.

Timer2 can be optionally used as the shift clock source for the MSSP modules operating in SPI mode. Additional information is provided in the *"PIC24F Family Reference Manual"*, **Section 58. "Master Synchronous Serial Port (MSSP)"** (DS30627).

59.2.5 Timer Match Gate Operation

For even numbered timer modules, a TMR-to-PR register match event results in a low-to-high pulse that can serve as a gate signal to Timer3 (or other odd numbered timers). The gate pulse is generated on the very next cycle after the match, as the TMR register is reset to 00h. See **Section 59.3.5 "Timer3 Gates"** for more information.

When more than one of the 8-bit timers is instantiated (e.g., Timer4, etc.), the higher numbered timers are usually equipped with the Match Gate feature. However, the Match Gate feature may be incorporated on any even numbered timer, including Timer2. Refer to the specific device data sheet for implementation details.

59.3 TIMER3 MODULE

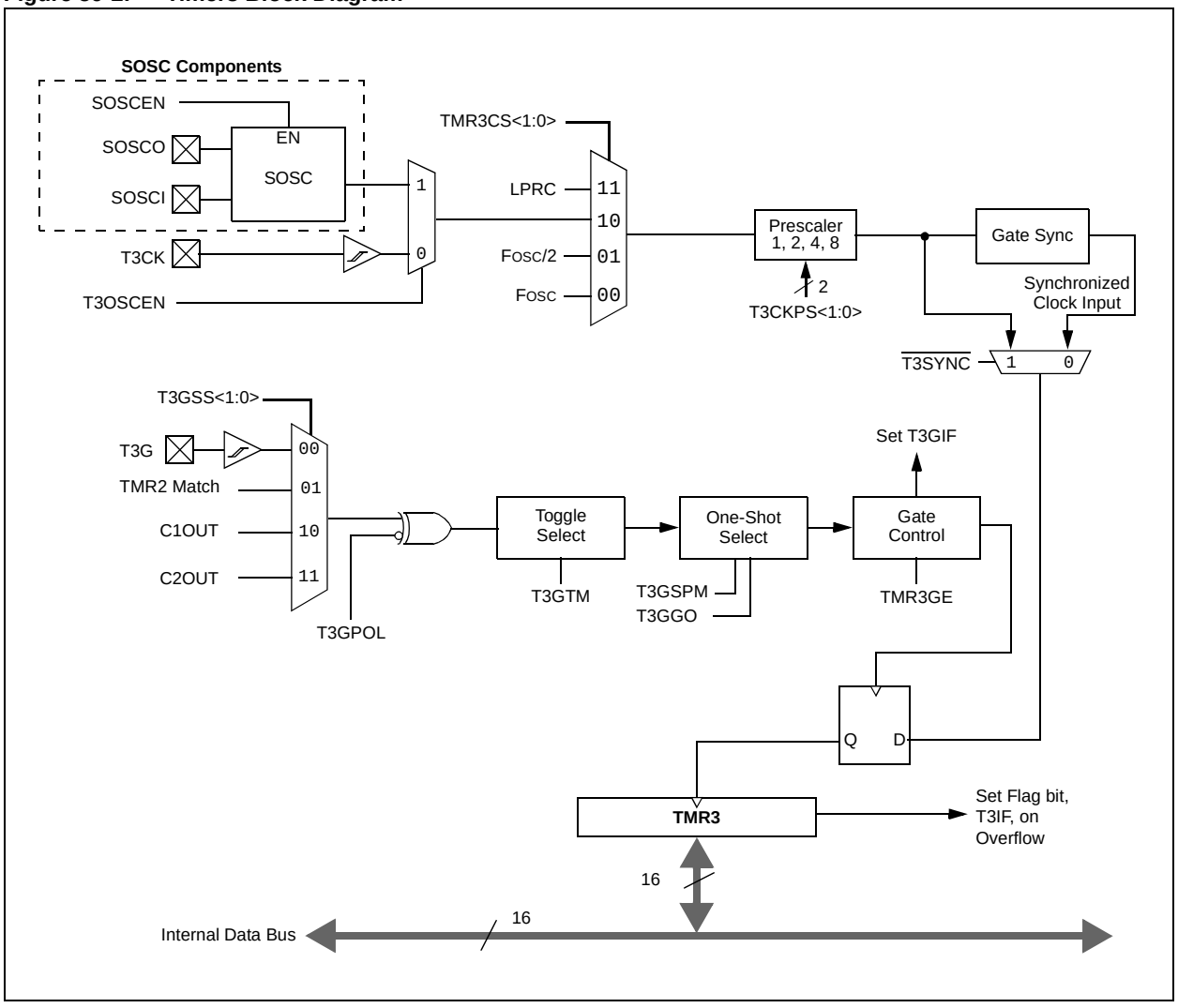
The Timer3 timer/counter modules incorporate these features:

- Software-selectable operation as a 16-bit timer or counter
- One 16-bit readable and writable Timer Value register
- Selectable clock source (internal or external) with device clock or SOSC/LPRC options
- Interrupt-on-overflow
- Multiple timer gating options, including:
  - User-selectable gate sources and polarity
  - Gate toggle operation
  - Single Pulse (One-Shot) mode
- Module Reset on ECCP Special Event Trigger

A simplified block diagram of the Timer3 module is shown in Figure 59-2.

The FOSC clock source should not be used with the ECCP capture/compare features. If the timer will be used with the capture or compare features, always select one of the other timer clocking options.

Figure 59-2: Timer3 Block Diagram



59.3.1 Registers

The Timer3 module uses three registers: T3CON, T3GCON and TMR3.

The Timer3 module is controlled through the T3CON register (Register 59-2), which also selects the clock source options for the ECCP modules. The T3GCON register (Register 59-3) controls the timer's gating options.

The TMR3 register is the 16-Bit Timer/Counter Value register. Although the upper and lower bytes are read and written to differently, the entire value is stored in a single Word-Wide register.

Register 59-2: T3CON: Timer3 Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
TMR3CS1	TMR3CS0	T3CKPS1	T3CKPS0	T3OSCEN	$\overline{\text{T3SYNC}}$	—	TMR3ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **TMR3CS<1:0>:** Clock Source Select bits
11 = Low-Power RC oscillator (LPRC)
10 = External clock source (selected by T3CON<3>)
01 = Instruction clock (FOSC/2)
00 = System clock (FOSC)(1)

bit 5-4 **T3CKPS<1:0>**: Timer3 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T3OSCEN**: Timer Oscillator Enable bit
1 = SOSC (Secondary) Oscillator is used as the clock source
0 = T3CK digital input pin is used as the clock source

bit 2 **$\overline{\text{T3SYNC}}$:** External Clock Input Synchronization Control bit
When TMR3CS<1:0> = 10:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
When TMR3CS<1:0> = 0x:
This bit is ignored; Timer3 uses the internal clock.

bit 1 **Unimplemented:** Read as '0'

bit 0 **TMR3ON:** Timer On bit
1 = Enables timer
0 = Stops timer

Note 1: The FOSC clock source should not be selected if the timer will be used with the ECCP capture or compare features.

Register 59-3: T3GCON: Timer3 Gate Control Register(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-x	R/W-0	R/W-0
TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/$\overline{\text{T3DONE}}$	T3GVAL	T3GSS1	T3GSS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **TMR3GE:** Timer Gate Enable bit

If TMR3ON = 0:
This bit is ignored.

If TMR3ON = 1:
1 = Timer counting is controlled by the Timer3 gate function
0 = Timer counts regardless of the Timer3 gate function

bit 6 **T3GPOL:** Gate Polarity bit

1 = Timer gate is active-high (Timer3 counts when the gate is high)
0 = Timer gate is active-low (Timer3 counts when the gate is low)

bit 5 **T3GTM:** Gate Toggle Mode bit

1 = Timer Gate Toggle mode is enabled.
0 = Timer Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer3 gate flip-flop toggles on every rising edge.

bit 4 **T3GSPM:** Timer Gate Single Pulse Mode bit

1 = Timer Gate Single Pulse mode is enabled and is controlling Timerx gate
0 = Timer Gate Single Pulse mode is disabled

bit 3 **T3GGO/$\overline{\text{T3DONE}}$:** Timer Gate Single Pulse Acquisition Status bit

1 = Timer gate single pulse acquisition is ready, waiting for an edge
0 = Timer gate single pulse acquisition has completed or has not been started
This bit is automatically cleared when T3GSPM is cleared.

bit 2 **T3GVAL:** Timer Gate Current State bit

Indicates the current state of the timer gate that could be provided to TMR3. It is unaffected by the Timer Gate Enable bit (TMR3GE).

bit 1-0 **T3GSS<1:0>:** Timer Gate Source Select bits

11 = Comparator 2 output
10 = Comparator 1 output
01 = TMR2 to match PR2 output
00 = T3G input pin

Note 1: Initializing the T3GCON prior to T3CON is recommended.

59.3.2 Timer3 Operation

Timer3 can operate in these modes:

- Timer
- Synchronous Counter
- Asynchronous Counter
- Timer with Gated Control

The operating mode is determined by the clock select bits, TMRxCS<1:0> (TxCON<7:6>). When the TMRxCS bits are cleared (= 00), the system clock (FOSC) is the Timer3 clock source. When TMRxCS<1:0> = 01, Timer3 increments on every instruction cycle (FOSC/2).

When TMRxCS<1:0> = 10, Timer3 works as a counter from the external clock on the T3CLK pin (on the rising edge after the first falling edge) or the Secondary Oscillator (SOSC). When TMRxCS<1:0> = 11, the Low-Power RC Oscillator (LPRC) is the Timer3 clock source.

59.3.3 Read/Write Operations

Timer3 operates natively as a 16-bit timer and counter. All read and write operations on the TMR3 register occur as a single 16-bit operation. This is in contrast to the equivalent module in PIC18 devices, where the Timer registers could be accessed in a single 16-bit, or two 8-bit, read or write operations. When migrating applications from PIC18 devices, users should verify that Timer3 (and other odd numbered timers) are using 16-bit read/write access for maximum compatibility.

59.3.4 Using the Secondary Oscillator as the Timer3 Clock Source

The Secondary Oscillator (SOSC) may be used as the clock source for Timer3. SOSC is enabled by setting the SOSCEN (OSCCON<1>) bit. To use it as the Timer3 clock source, the TMRxCS<1:0> bits must also be set to '10'. This also configures Timer3 to increment on every rising edge of the oscillator source.

59.3.5 Timer3 Gates

Timer3 can be configured to count freely, or the count can be enabled and disabled using the Timer3 gate circuitry. This is also referred to as the Timer3 gate count enable.

The Timer3 gate can also be driven by multiple selectable sources.

59.3.5.1 TIMER3 GATE COUNT ENABLE

The Timer3 Gate Enable mode is enabled by setting the TMR3GE bit (T3GCON<7>). The polarity of the Timer3 Gate Enable mode is configured using the T3GPOL bit (T3GCON<6>).

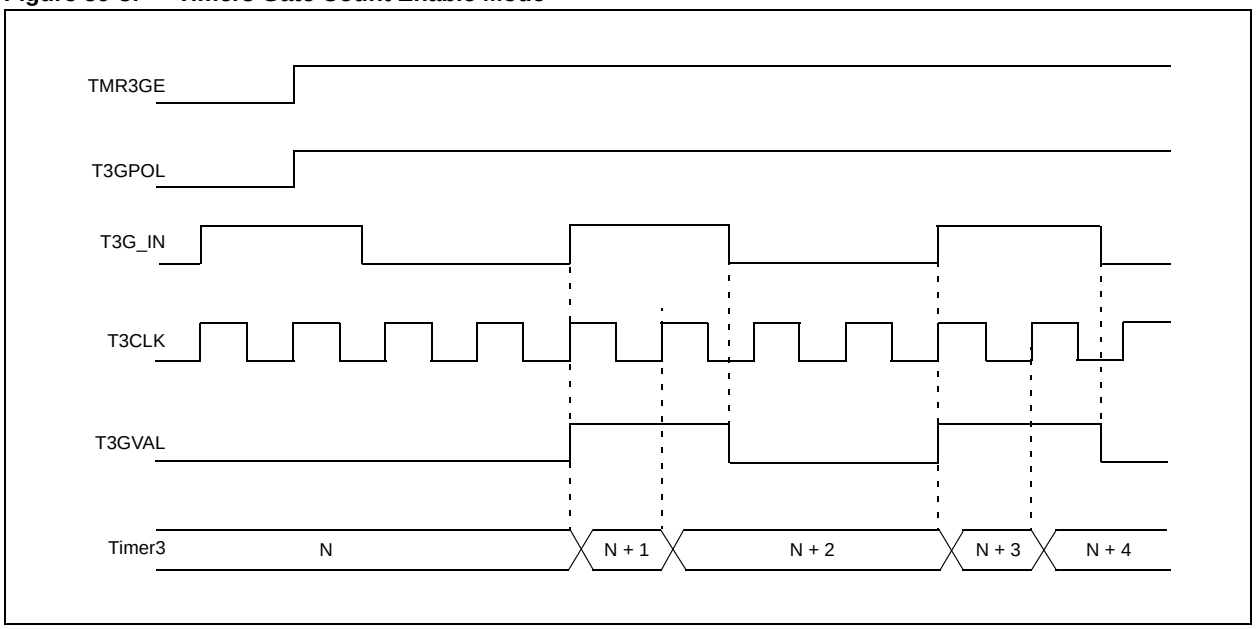
When Timer3 Gate Enable mode is enabled, Timer3 will increment on the rising edge of the Timer3 clock source. When Timer Gate Enable mode is disabled, no incrementing occurs and Timer3 holds the current count. See Figure 59-3 for timing details.

Table 59-1: TIMER3 GATE ENABLE SELECTIONS

T3CLK(1)	T3GPOL (T3GCON<6>)	T3G Pin	Timer3 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

Note 1: This is the TMR3 clock source. For more information, see Figure 59-2.

Figure 59-3: Timer3 Gate Count Enable Mode



59.3.5.2 TIMER3 GATE SOURCE SELECTION

The Timer3 gate source can be selected from one of four different sources. Source selection is controlled by the T3GSS<1:0> bits (T3GCON<1:0>). The polarity for each available source is also selectable and is controlled by the T3GPOL bit (T3GCON<6>).

Table 59-2: TIMER3 GATE SOURCES

TxGSS<1:0>	Timerx Gate Source
00	T3G Timer Gate Pin
01	TMR2 Matches PR2
10	Comparator 1 Output
11	Comparator 2 Output

59.3.5.2.1 T3G Pin Gate Operation

The T3G pin is one source for Timer3 gate control. It can be used to supply an external source to the gate circuitry.

59.3.5.2.2 Timer2 Match Gate Operation

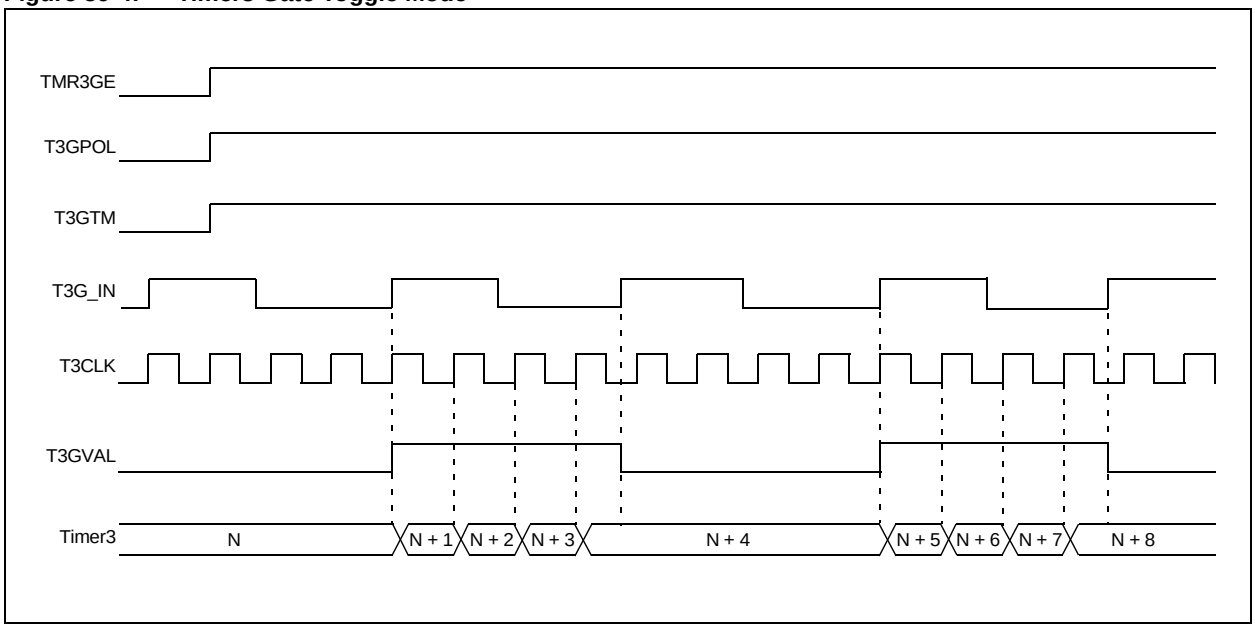
The TMR2 register will increment until it matches the value in the PR2 register. On the very next increment cycle, TMR2 will be reset to 00h. When this Reset occurs, a low-to-high pulse will automatically be generated and internally supplied to the Timer3 gate circuitry.

59.3.5.3 TIMER3 GATE TOGGLE MODE

When Timer3 Gate Toggle mode is enabled, it is possible to measure the full cycle length of a Timer3 gate signal, as opposed to the duration of a single level pulse.The Timer3 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. (For timing details, see Figure 59-4.) The T3GVAL bit indicates when the Toggled mode is active and the timer is counting.

Timer3 Gate Toggle mode is enabled by setting the T3GTM bit (T3GCON<5>). When the T3GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Figure 59-4: Timer3 Gate Toggle Mode



59.3.5.4 TIMER3 GATE SINGLE PULSE MODE

When Timer3 Gate Single Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer3 Gate Single Pulse mode is first enabled by setting the T3GSPM bit (T3GCON<4>), then setting the T3GGO/$\overline{\text{T3DONE}}$ bit (T3GCON<3>).

The timer is fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T3GGO/$\overline{\text{T3DONE}}$ bit is automatically cleared. No other gate events will be allowed to increment Timer3 until the T3GGO/$\overline{\text{T3DONE}}$ bit is once again set in software.

Clearing the T3GSPM bit also clears the T3GGO/$\overline{\text{T3DONE}}$ bit. (For timing details, see Figure 59-5.)

Simultaneously enabling the Toggle mode and the Single Pulse mode permits both sections to work together. This allows the cycle times on the Timer3 gate source to be measured. (For timing details, see Figure 59-6.)

Figure 59-5: Timer3 Gate Single Pulse Mode

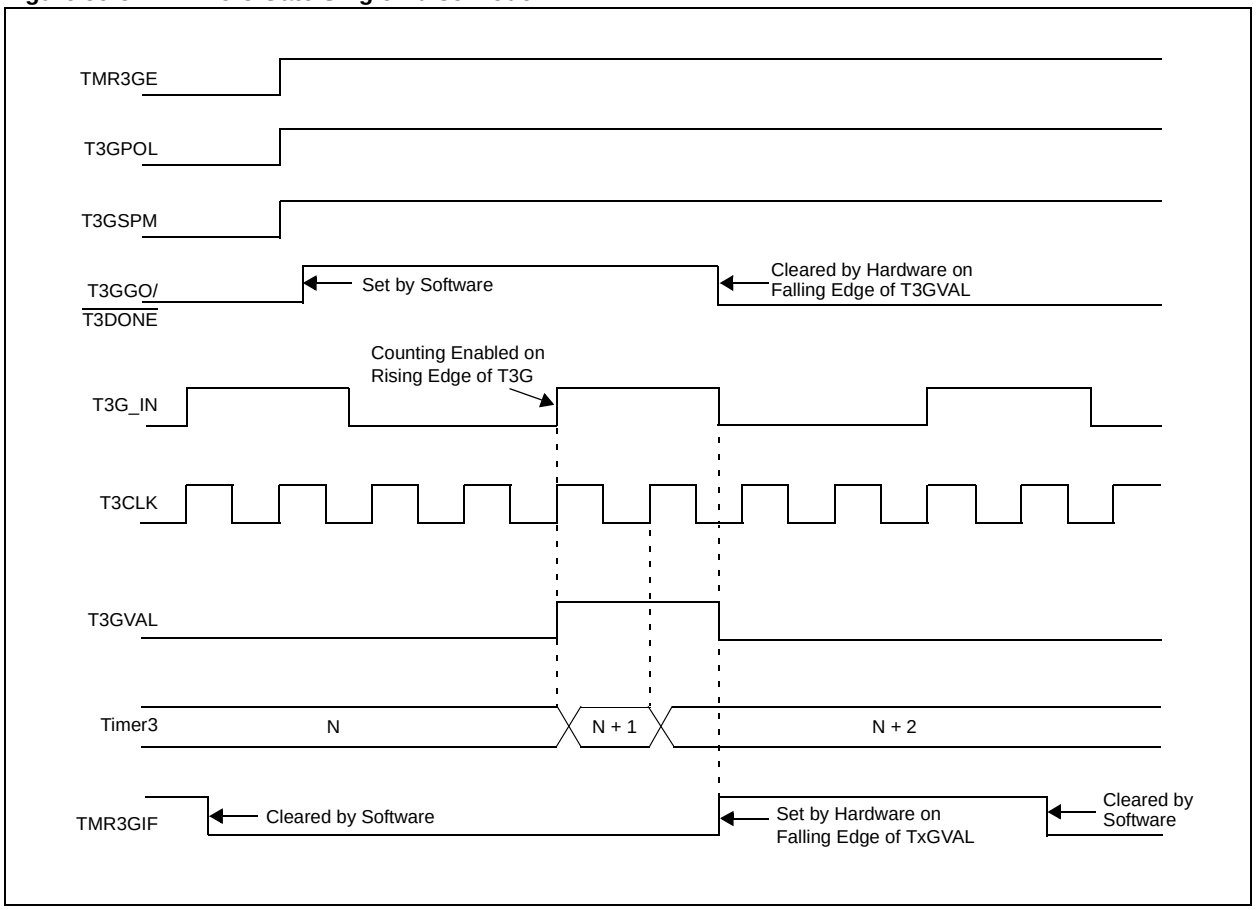
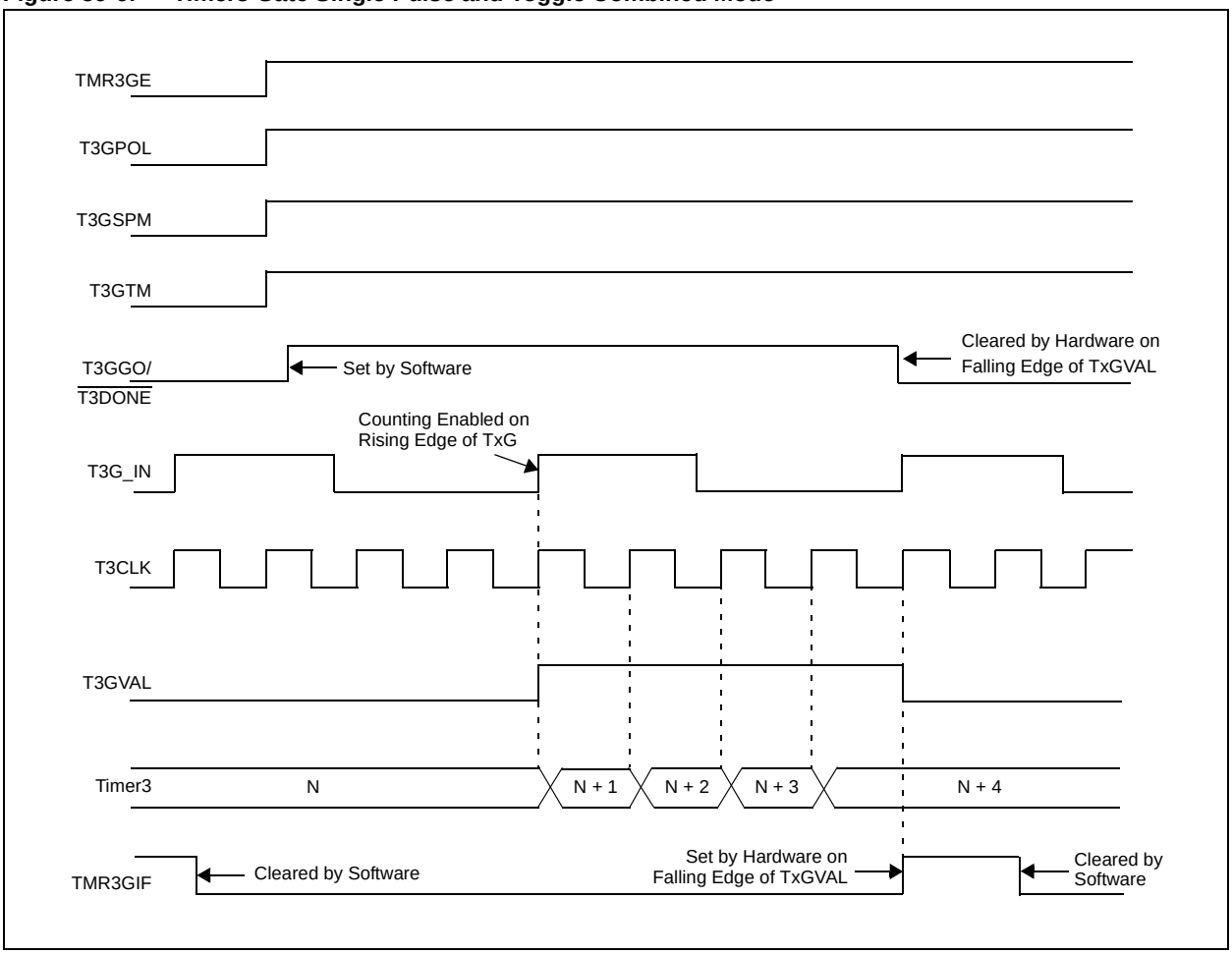


Figure 59-6: Timer3 Gate Single Pulse and Toggle Combined Mode



59.3.5.5 TIMER3 GATE VALUE STATUS

When Timer3 gate value status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the T3GVAL bit (T3GCON<2>). The T3GVAL bit is valid even when the Timer3 gate is not enabled (TMR3GE bit is cleared).

59.3.6 Timer3 Interrupt

The TMR3 register increments from 0000h to FFFFh and overflows to 0000h. The Timer3 interrupt, if enabled, is generated on overflow and is latched in the Timer3 Interrupt Flag bit, T3IF. This interrupt can be enabled or disabled by setting or clearing the T3IE bit, respectively.

59.3.6.1 TIMER3 GATE EVENT INTERRUPT

When the Timer3 gate event interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T3GVAL occurs, the T3GIF flag bit in the IFSx register will be set. If the T3GIE bit is set, then an interrupt will be recognized.

The T3GIF flag bit operates even when the Timer3 gate is not enabled (TMR3GE bit is cleared).

59.3.7 Resetting Timer3 Using the ECCP Special Event Trigger

If the ECCP modules are configured to use Timer3 and to generate a Special Event Trigger in Compare mode (CCPxM<3:0> = 1011), this signal will reset Timer3. The module must be configured as either a timer, or synchronous counter, to take advantage of this feature. When used this way, the CCPRxH:CCPRxL register pair effectively becomes a Period register for the timer.

If Timer3 is running in Asynchronous Counter mode, the Reset operation may not work.

In the event that a write to Timer3 coincides with a Special Event Trigger from an ECCP module, the write will take precedence.

Note:	The Special Event Triggers from the ECCP module will clear the TMR3 register's content, but not set the T3IF interrupt flag bit.

59.4 OPERATION DURING SLEEP/IDLE MODES

59.4.1 Sleep Mode

All even numbered timers are disabled in Sleep mode.

Odd numbered timers are generally disabled in Sleep mode, as their on-chip clock sources are also disabled. However, they may continue to run in Sleep mode if an external clock is provided on the external clock input pin (T3CLK). In this case, the timer can continue to count in Asynchronous Counter mode, and can still generate interrupts and wake the device.

59.4.2 Idle Mode

All timers continue to operate in Idle mode.

59.5 EFFECTS OF A RESET

In any mode, a device Reset disables all 8/16-bit timers. For even numbered timers, the Period register resets to FFh.

59.6 REGISTER MAPS

Summaries of the registers associated with the PIC24F General Purpose 8/16-Bit Timer modules are provided in Table 59-3.

Table 59-3: General Purpose Timer Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR2(1)	—	—	—	—	—	—	—	—	Timer2 Register								0000
PR2(1)	—	—	—	—	—	—	—	—	Timer2 Period Register								00FF
T2CON(1)	—	—	—	—	—	—	—	—	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	0000
TMR3(2)	Timer3 Register																xxxx
T3GCON(2)	—	—	—	—	—	—	—	—	TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/$\overline{\text{T3DONE}}$	T3GVAL	T3GSS1	T3GSS0	0000
T3CON(2)	—	—	—	—	—	—	—	—	TMR3CS1	TMR3CS0	T3CKPS1	T3CKPS0	T3OSCEN	$\overline{\text{T3SYNC}}$	—	TMR3ON	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Register and bit naming conventions apply for any additional 8-bit timers (e.g., T4CON and PR4 for Timer4, etc.).

2: Register and bit naming conventions apply for any additional 8/16-bit timers (e.g., T5CON, T5GCON and TMR5 for Timer5, etc.).

59.7 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the General Purpose 8/16-Bit Timers of PIC24F devices are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

59.8 REVISION HISTORY

Revision A (October 2011)

Original version of this document.

Note the following details of the code protection feature on Microchip devices:

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