# Section 57. Power-Saving Features with VBAT

## HIGHLIGHTS

This section of the manual contains the following major topics:

## 57.1 INTRODUCTION

All PIC24F devices offer a number of built-in strategies for reducing power consumption. These strategies can be particularly useful in applications, which are both power-constrained (such as battery operation), yet require periods of full-power operation for timing-sensitive routines (such as serial communications).

In addition, some families of PIC24F devices offer an extended range of power-saving strategies. Aside from their low-power architecture, these devices include an expanded range of dedicated hardware features that allow the microcontroller to reduce power consumption to even lower levels when long-term hibernation is required, and still be able to resume operation on short notice. For convenience, this expanded feature set is referred to as “Power-Saving Features with VBAT”, for their new hardware-based features.

Devices that include Power-Saving features with VBAT use five power reduction strategies:

- Instruction-Based Power-Saving Modes
- Hardware-Based Power Reduction Features
- Microcontroller Clock Manipulation
- Software Controlled Doze Mode
- Selective Peripheral Control

Combinations of these methods can be used to selectively tailor an application’s power consumption, while still maintaining critical or timing-sensitive application features. However, it is more convenient to discuss the strategies separately.

## 57.2 OVERVIEW OF POWER-SAVING MODES

In addition to full-power operation, otherwise known as Run mode, PIC24F devices that include the VBAT feature, offer three instruction-based power-saving modes and one hardware-based mode. In descending order of power consumption, they are:

- Idle
- Sleep (including Low-Voltage Sleep)
- Deep Sleep (with and without retention)
- VBAT (with and without RTCC)

By powering down all four modes, different functional areas of the microcontroller allow progressive reductions of operating and Idle power consumption. In addition, three of the modes can be tailored for more power reduction, at a trade-off of some operating features. Table 57-1 lists all of the operating modes (including Run mode, for comparison), in order of increasing power savings, and summarizes how the microcontroller exits the different modes.

**Table 57-1: Summary of Operating Modes for PIC24F Family Devices with VBAT Power-Saving Features(5)**

| Mode | Entry | Active Systems | | | | | Exit Conditions | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Interrupts | | Resets | | | | | | |
| | | Core | Peripherals | Data RAM Retention | RTCC(1) | DSGPRn(2) | All | INT0 only | All | POR | MCLR | RTCC Alarm | (DS)WDT(3) | VDD Restore | Code Execution Resumes |
| Run (default) | N/A | Y | Y | Y | Y | Y | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Idle | Instruction | N | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | N/A | Next Instruction |
| Sleep modes: | | | | | | | | | | | | | | | |
| Sleep | Instruction | N | S(4) | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | N/A | Next Instruction |
| Low-Voltage Sleep | Instruction + RETEN/LVREN bit | N | S(4) | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | N/A | |
| Deep Sleep modes: | | | | | | | | | | | | | | | |
| Retention Deep Sleep | Instruction + DSEN bit + RETEN/LVREN bit | N | N | Y | Y | Y | N | Y | N | Y | Y | Y | Y | N/A | Next Instruction |
| Deep Sleep | Instruction + DSEN bit | N | N | N | Y | Y | N | Y | N | Y | Y | Y | Y | N/A | Reset Vector |
| VBAT: | | | | | | | | | | | | | | | |
| with RTCC | Hardware | N | N | N | Y | Y | N | N | N | N | N | N | N | Y | Reset Vector |

**Note 1:** If RTCC is otherwise enabled in firmware.

**2:** Data retention in the DSGPR0 and DSGPR1 registers.

**3:** Deep Sleep WDT in Deep Sleep modes; WDT in all other modes.

**4:** Some select peripherals may continue to operate in this mode, using either the LPRC or an external clock source.

**5:** Verify with the device-specific data sheet if all the modes are supported.

## 57.3 INSTRUCTION-BASED POWER-SAVING MODES

PIC24F devices have three instruction-based power-saving modes; two of these have additional features that allow for additional tailoring of power consumption. All three modes are entered through the execution of the PWRSAV instruction. In descending order of power consumption, they are:

- Idle Mode: The CPU is disabled, but the system clock source continues to operate. Peripherals continue to operate, but can optionally be disabled.
- Sleep Modes: The CPU, system clock source and any peripherals that operate on the system clock source are disabled.
- Deep Sleep Modes: The CPU system clock source, and all the peripherals except RTCC and DSWDT, are disabled. This is the lowest power mode for the device. The power to RAM and Flash is also disabled. Deep Sleep modes represent the lowest power modes available without removing power from the application.

Idle and Sleep modes are entered directly with the #IDLE_MODE and #SLEEP_MODE arguments. For Deep Sleep mode, it is necessary to set the DSEN bit (DSCON<15>) bit, executing the PWRSAV instruction. To prevent inadvertent entry into Deep Sleep mode and possible loss of data, the DSEN bit must be written to twice (the repeat sequence). The PWRSAV instruction is then executed immediately after the second write. The writes to DSEN do not need to be back-to-back, but this is recommended as a preferred practice.

Examples of the assembly syntax for the PWRSAV instruction are provided in Example 57-1.

**Note:** SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

**Example 57-1: PWRSAV Assembly Syntax**

```
//Put the device into Idle mode
PWRSAV     #IDLE_MODE;
//
//Put the device into Sleep mode
PWRSAV     #SLEEP_MODE;
//
//Put the device into Deep Sleep mode
//Note the repeat sequence to set the DSEN bit
MOV        #8000, W2
MOV        W2, DSCON
MOV        W2, DSCON
PWRSAV     #SLEEP_MODE;
//Alternate procedure
CLR        DSCON
CLR        DSCON
BSET       DSCON DSEN
NOP                  //Writes to the DSEN bit do not need
NOP                  //to be sequential (back-to-back)
NOP
BSET       DSCON DSEN
PWRSAV     #SLEEP_MODE;
```

The instruction-based power-saving modes are exited as a result of several different hardware triggers. When the device exits one of these three operating modes, it is said to ‘wake-up’. The characteristics of the power-saving modes are described in the subsequent sections.

| | |
|---|---|
| **Note:** | A repeat sequence is required to set the DSEN bit. The repeat sequence (repeating the instruction twice) is required to write into any of the Deep Sleep registers (DSCON, DSWAKE, DSGPR0, DSGPR1). This is required to avoid the user from entering Deep Sleep by mistake. Any write to these registers has to be done twice to actually complete the write (see Example 57-2).<br><br>To enter Deep Sleep mode correctly, the DSCON<0> bit needs to be cleared prior to executing the SLEEP instruction (see Example 57-1). Before setting the DSEN bit, the DSCON is cleared, or alternately, the DSCON is loaded by 0x8000. |

**Example 57-2: The Repeat Sequence**

Example 1:

```
mov   #8000, w2           ; enable DS
mov   w2, DSCON
mov   w2, DSCON           ; second write required to
actually write to DSCON
```

Example 2:

```
bset  DSCON, #15
nop
nop
nop
bset  DSCON, #15          ; enable DS (two writes required)
```

### 57.3.1 Interrupts Coincident with Power Save Instructions

Any interrupt that coincides with the execution of a PWRSAV instruction will be held off until entry into Sleep, Idle or Deep Sleep mode is completed. The device will then wake up from the power-managed mode.

### 57.3.2 Low-Voltage Regulator

For select PIC24F device families, a second on-chip voltage regulator is used for power management in Sleep and Deep Sleep modes. This regulator, also known as the low-voltage regulator, supplies core logic and other circuits with power at a lower VCORE level, about 1.2V nominal. Running these circuits at a lower voltage allows for an additional incremental power saving over the normal minimum VCORE level.

| | |
|---|---|
| **Note:** | Refer to the device data sheet for device-specific regulator output values. These are typically specified as VLVR and VRGOUT for the low-voltage and main (on-chip) regulator, respectfully. |

In Sleep and Deep Sleep modes, using the regulator maintains the entire data RAM and its contents, instead of just a few protected registers. This allows the device to exit a power-saving mode and resume code execution as its previous state.

The low-voltage regulator is controlled by the $\overline{\text{LPCFG}}$/LVRCFG Configuration bit (also designated as LVRCFG is some devices), and the RETEN/LVREN bit (RCON<12>). The $\overline{\text{LPCFG}}$/LVRCF bit makes the low-voltage regulator available for software control. By default ($\overline{\text{LPCFG}}$/LVRCFG = 1), the regulator is disabled and the RETEN/LVREN bit has no effect. Programming $\overline{\text{LPCFG}}$/LVRCFG (= 0) allows the RETEN/LVREN bit to control the regulator's operation, leaving its use in power-saving modes at the user's discretion.

Setting the RETEN/LVREN bit prior to executing the PWRSAV #SLEEP_MODE instruction puts the device into Retention Sleep mode. If the DSEN bit was also unlocked and set prior to the instruction, the device will enter Retention Deep Sleep mode.

The low-voltage regulator is not available outside of Sleep or Deep Sleep modes. Enabling it while the device is operating in Run, Idle or Doze modes does not allow the device to operate at a lower level of VCORE.

### 57.3.3 Idle Mode

When the device enters Idle mode, the following events occur:

- The CPU will stop executing instructions.
- The WDT is automatically cleared.
- The system clock source will remain active and the peripheral modules, by default, will continue to operate normally from the system clock source. Peripherals can optionally be shut down in Idle mode using their 'Stop in Idle' control bit. (See peripheral descriptions for further details.)
- If the WDT or FSCM is enabled, the LPRC will also remain active.

The processor will wake-up from Idle mode on the following events:

- On any interrupt that is individually enabled.
- On any source of device Reset.
- On a WDT time-out.

Upon wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the PWRSAV instruction, or the first instruction in the Interrupt Service Routine (ISR).

#### 57.3.3.1 TIME DELAYS ON WAKE-UP FROM IDLE MODE

Unlike a wake-up from Sleep mode, there are no additional time delays associated with wake-up from Idle mode. The system clock is running during Idle mode, therefore, no start-up times are required at wake-up.

#### 57.3.3.2 WAKE-UP FROM IDLE ON INTERRUPT

User interrupt sources that are assigned to CPU Priority Level 0 cannot wake-up the CPU from Idle mode because the interrupt source is effectively disabled. To use an interrupt as a wake-up source, the CPU priority level for the interrupt must be assigned to CPU Priority Level 1 or greater.

Any source of interrupt that is individually enabled using the corresponding IE control bit in the IECx register, and exceeds the current CPU priority level, will be able to wake-up the processor from Idle mode. When the device wakes from Idle mode, one of two options may occur:

- If the assigned priority for the interrupt is less than or equal to the current CPU priority, the device will wake-up and continue code execution from the instruction following the PWRSAV instruction that initiated Idle mode.
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device will wake-up and the CPU exception process will begin. Code execution will continue from the first instruction of the ISR.

The IDLE status bit (RCON<2>) is set upon wake-up.

#### 57.3.3.3 WAKE-UP FROM IDLE ON RESET

Any Reset, other than a Power-on Reset (POR), will wake-up the CPU from Idle mode. On any device Reset, except a POR, the IDLE status bit is set (RCON<2>) to indicate that the device was previously in Idle mode; in a POR, the IDLE bit is cleared.

#### 57.3.3.4 WAKE-UP FROM IDLE ON WDT TIME-OUT

If the WDT is enabled, then the processor will wake-up from Idle mode on a WDT time-out and continue code execution with the instruction following the PWRSAV instruction that initiated Idle mode. Note that the WDT time-out does not reset the device in this case. The WDTO and IDLE status bits (RCON<4,2>) will both be set.

### 57.3.4 Sleep Modes

Most PIC24F devices that incorporate power-saving features and VBAT offer two distinct Sleep modes: Sleep mode and Low-Voltage Sleep mode. The characteristics of both Sleep modes are:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be optimum, provided no I/O pin is sourcing the current.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT is enabled.
- If the on-chip voltage regulator and Brown-out Reset (BOR) are enabled, the Brown-out Reset (BOR) circuit remains operational during Sleep mode.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some peripherals may continue to operate in Sleep mode. These peripherals include I/O pins that detect a change in the input signal or peripherals that use an external clock input. Any peripheral that operates from the system clock source will be disabled in Sleep mode.

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt source that is individually enabled
- On any form of device Reset
- On a WDT time-out

| **Note:** | The on-chip voltage regulator and the low-voltage regulator output voltages will vary based on the device. Refer to the device-specific data sheet for the on-chip/low-voltage regulator specifications. |
|---|---|

#### 57.3.4.1 LOW-VOLTAGE SLEEP MODE

Low-Voltage Sleep mode allows for additional power savings over Sleep mode by maintaining key systems from the lower power retention regulator. When the low-voltage regulator is used, the normal on-chip voltage regulator is turned off. By using a lower voltage, a lower total power consumption is achieved.

Low-Voltage Sleep also offers the advantage of maintaining the contents of the data RAM. As a trade-off, the wake-up time is slightly longer than that for Sleep mode.

Low-Voltage Sleep is controlled by the RETEN/LVREN bit (RCON<12>) and the $\overline{\text{LPCFG}}$/LVRCFG Configuration bit, as described in **Section 57.3.2 "Low-Voltage Regulator"**.

#### 57.3.4.2 CLOCK SOURCE CONSIDERATIONS

When the device wakes up from either of the Sleep modes, it will restart the same clock source that was active when Sleep mode was entered. Wake-up delays for the different oscillator modes are shown in Table 57-3 and Table 57-4, respectively.

If the system clock source is derived from a crystal oscillator and/or the PLL, the Oscillator Start-up Timer (OST) and/or PLL lock times must be applied before the system clock source is made available to the device. As an exception to this rule, no oscillator delays are necessary if the system clock source is the secondary oscillator and it was running while in Sleep mode.

##### 57.3.4.2.1 Slow Oscillator Start-up

The OST and PLL lock times may not have expired when the power-up delays have expired.

To avoid this condition, one can enable Two-Speed Start-up by the device that will run on FRC until the clock source is stable. Once the clock source is stable, the device will switch to the selected clock source.

#### 57.3.4.3 WAKE-UP FROM SLEEP ON INTERRUPT

User interrupt sources that are assigned to CPU Priority Level 0 cannot wake-up the CPU from Sleep mode because the interrupt source is effectively disabled. To use an interrupt as a wake-up source, the CPU priority level for the interrupt must be assigned to CPU Priority Level 1 or greater.

Any source of interrupt that is individually enabled, using its corresponding IE control bit in the IECx registers, can wake up the processor from Sleep mode. When the device wakes from Sleep mode, one of two following actions may occur:

- If the assigned priority for the interrupt is less than, or equal to, the current CPU priority, the device will wake-up and continue code execution from the instruction following the PWRSAV instruction that initiated Sleep mode.
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device will wake-up and the CPU exception process will begin. Code execution will continue from the first instruction of the ISR.

The SLEEP status bit (RCON<3>) is set upon wake-up. For RCON register values, refer to **Section 7. "Reset"** in the *"PIC24F Family Reference Manual"*.

#### 57.3.4.4 WAKE-UP FROM SLEEP ON RESET

All sources of device Reset will wake-up the processor from Sleep mode. Any source of Reset (other than a POR) that wakes the processor will set the SLEEP status bit (RCON<3>) to indicate that the device was previously in Sleep mode.

On a Power-on Reset (POR), the SLEEP bit is cleared.

#### 57.3.4.5 WAKE-UP FROM SLEEP ON WATCHDOG TIME-OUT

If the Watchdog Timer (WDT) is enabled and expires while the device is in Sleep mode, the processor will wake-up. The WDTO and SLEEP status bits (RCON<4:3>) are both set to indicate that the device resumed operation due to the WDT expiration. Note that this event does not reset the device. Operation continues from the instruction following the PWRSAV instruction that initiated Sleep mode.

#### 57.3.4.6 CONTROL BIT SUMMARY FOR SLEEP MODES

Table 57-2 shows the settings for the bits relevant to Sleep modes.

**Table 57-2: Bit Settings for All Sleep Modes**

| Mode | DSEN (DSCON<15>) | Low-Voltage Regulator | | |
|---|---|---|---|---|
| | | $\overline{\text{LPCFG}}$/LVRCFG (CW1<10>)(1) | RETEN/LVREN (RCON<12>) | State |
| Sleep | x | 1 | x | Disabled |
| | x | 0 | 0 | Disabled |
| Low-Voltage Sleep | x | 0 | 1 | Enabled |

**Note 1:** This bit is also designated as LVRCFG in some devices.

#### 57.3.4.7 WAKE-UP DELAYS

The restart delay associated with waking up from Sleep and Retention Sleep modes parallel each other in terms of clock start-up times; they differ in the time it takes to switch over from their respective regulators. The delays for the different oscillator modes are shown in Table 57-3 and Table 57-4, respectively.

| **Note:** | The PMSLP/VREGS bit (RCON<8>) may also be designated as the VREGS bit in certain PIC24F devices. The functionality of the bit, and its effect on wake-up times, remains constant regardless of the name. |
|---|---|

**Table 57-3: Delay Times for Exiting from Sleep Mode**

| Clock Source | | Exit Delay | Oscillator Delay | Notes |
|---|---|---|---|---|
| EC | | TPM | — | 1 |
| ECPLL | | TPM | TLOCK | 1, 3 |
| XT, HS | | TPM | TOST | 1, 2 |
| XTPLL, HSPLL | | TPM | TOST + TLOCK | 1, 2, 3, 4 |
| SOSC | (Off during Sleep) | TPM | TOST | 1, 2 |
| | (On during Sleep) | TPM | — | 1 |
| FRC, FRCDIV | | TPM | TFRC | 1, 5 |
| LPRC | (Off during Sleep) | TPM | TLPRC | 1, 5 |
| | (On during Sleep) | TPM | — | 1 |
| FRCPLL | | TPM | TLOCK | 1, 3 |

**Note 1:** TPM = Start-up delay for program memory stabilization; applicable only when PMSLP/VREGS (RCON<8>) = 0.

**2:** TOST = Oscillator Start-up Timer (OST); a delay of 1024 oscillator periods before the oscillator clock is released to the system.

**3:** TLOCK = PLL lock time.

**4:** HSPLL mode exceeds PIC24F maximum operating frequency.

**5:** TFRC and TLPRC are RC oscillator start-up times.

**Note:** Please refer to the **"Electrical Characteristics"** section of the specific product data sheet for detailed operating frequency and timing specification values.

**Table 57-4: Delay Times for Exiting from Low-Voltage Sleep Mode**

| Clock Source | | Exit Delay | Oscillator Delay | Notes |
|---|---|---|---|---|
| EC | | TLVR + TPM | — | 1, 2 |
| ECPLL | | TLVR + TPM | TLOCK | 1, 2, 4 |
| XT, HS | | TLVR + TPM | TOST | 1, 2, 3 |
| XTPLL, HSPLL | | TLVR + TPM | TOST + TLOCK | 1, 2, 3, 4, 5 |
| SOSC | (Off during Sleep) | TLVR + TPM | TOST | 1, 2, 3 |
| | (On during Sleep) | TLVR + TPM | — | 1, 2 |
| FRC, FRCDIV | | TLVR + TPM | TFRC | 1, 2, 6 |
| LPRC | (Off during Sleep) | TLVR + TPM | TLPRC | 1, 2, 6 |
| | (On during Sleep) | TLVR + TPM | — | 1, 2 |
| FRCPLL | | TLVR + TPM | TLOCK | 1, 2, 4 |

**Note 1:** TLVR = Low-voltage regulator start-up delay.

**2:** TPM = Start-up delay for program memory stabilization; applicable only when PMSLP/VREGS (RCON<8>) = 0.

**3:** TOST = Oscillator Start-up Timer; a delay of 1024 oscillator periods before the oscillator clock is released to the system.

**4:** TLOCK = PLL lock time.

**5:** HSPLL mode exceeds PIC24F maximum operating frequency.

**6:** TFRC and TLPRC are RC oscillator start-up times.

**Note:** Please refer to the **"Electrical Characteristics"** section of the specific product data sheet for detailed operating frequency and timing specification values.

### 57.3.5 Deep Sleep Modes

The Deep Sleep modes brings the device into its lowest power consumption state without requiring the use of external switches to remove power from the device. There are two modes available: Deep Sleep mode and Retention Deep Sleep mode.

During both Deep Sleep modes, the power to the microcontroller core is removed to reduce leakage current. Therefore, most peripherals and functions of the microcontroller become unavailable during Deep Sleep. However, a few specific peripherals and functions are powered directly from the VDD supply rail of the microcontroller, and therefore, can continue to function in Deep Sleep. In addition, two data memory locations, DSGPR0 and DSGPR1, are preserved for context information after an exit from Deep Sleep.

Devices that implement Deep Sleep mode have a dedicated Deep Sleep Brown-out Reset (DSBOR) and a Deep Sleep Watchdog Timer Reset (DSWDT) for monitoring voltage and time-out events in Deep Sleep mode. The DSBOR and DSWDT are independent of the standard BOR and WDT used with other power-managed modes (Run, Idle and Sleep).

Entering Deep Sleep mode clears the DSWAKE register. If enabled, the Real-Time Clock and Calendar (RTCC) continues to operate uninterrupted.

When a wake-up event occurs in Deep Sleep mode (by Reset, RTCC alarm, external interrupt (INT0) or DSWDT), the device will exit Deep Sleep mode and re-arm a Power-on Reset (POR). When the device is released from Reset, code execution will resume at the device's Reset vector.

#### 57.3.5.1 RETENTION DEEP SLEEP MODE

In Retention Deep Sleep, the low-voltage regulator is enabled, which allows the data RAM to retain data while all other systems are powered down. This also allows the device to return to code execution where it left off, instead of going through a POR-like Reset.

As a trade-off, Retention Deep Sleep mode has greater power consumption than Deep Sleep.

Retention Deep Sleep is controlled by the RETEN/LVREN bit (RCON<12>) and the $\overline{\text{LPCFG}}$/LVRCFG Configuration bit, as described in **Section 57.3.2 "Low-Voltage Regulator"**.

#### 57.3.5.2 ENTERING DEEP SLEEP MODES

Deep Sleep modes are entered by:

- Setting the DSEN bit (DSCON<15>)
- Executing the `PWRSAV #SLEEP_MODE` instruction

To enter Retention Deep Sleep, the RETEN/LVREN bit must also be set prior to setting the DSEN bit.

In order to minimize the possibility of inadvertently entering Deep Sleep, the DSEN bit must be set by two separate write operations. Before setting the DSEN bit, the DSCON<0> bit should be cleared by a repeat sequence. To enter Deep Sleep, the `PWRSAV` instruction must be executed after setting the DSEN bit (i.e., the next instruction). If DSEN is not set when Sleep is executed, the device will enter a Sleep mode instead.

#### 57.3.5.3 DEEP SLEEP WAKE-UP SOURCES

The device can be awakened from Deep Sleep modes by any of the following:

- $\overline{\text{MCLR}}$
- POR
- RTCC alarm
- INT0 interrupt
- I/O pin interrupt
- DSWDT event

After waking from Deep Sleep mode, the device performs a POR. When the device is released from Reset, code execution will begin at the device's Reset vector.

The software can determine if the wake-up was caused from an exit from Deep Sleep mode by reading the DPSLP bit (RCON<10>). If this bit is set, the POR was caused by a Deep Sleep exit. The DS bit must be manually cleared by the software.

The software can determine the wake-up event source by reading the DSWAKE register. These registers are cleared automatically when entering Deep Sleep mode, so software should read these registers after exiting Deep Sleep mode or before re-enabling this mode.

##### 57.3.5.3.1 Clock Selection on Wake-up from Deep Sleep Mode

For Deep Sleep mode, the processor will restart with the default oscillator source, selected with the FNOSC Configuration bits. On wake-up from Deep Sleep, a POR is generated internally, hence, the system resets to its POR state with exception of the RCON, DSCON and DSGPRn registers.

For Retention Deep Sleep, the processor restarts with the same clock source that was selected before entering Retention Deep Sleep mode. Wake-up is similar to that of Sleep and Retention Sleep modes.

#### 57.3.5.4 SAVING CONTEXT DATA WITH THE DSGPRn REGISTERS

As exiting Deep Sleep mode causes a POR, most Special Function Registers (SFRs) reset to their default POR values. In addition, because the core power is not supplied in Deep Sleep mode, information in data RAM may be lost when exiting this mode. Applications which require critical data to be saved prior to Deep Sleep may use the Deep Sleep General Purpose registers, DSGPR0 and DSGPR1, or data EEPROM (if available). Unlike other SFRs, the contents of these registers are preserved while the device is in Deep Sleep mode. After exiting Deep Sleep, software can restore the data by reading the registers and clearing the RELEASE bit (DSCON<0>).

Any data stored in the DSGPR registers must be written twice (the repeat sequence). Like other Deep Sleep control features, the write operations do not need to be sequential. However, back-to-back writes are a recommended programming practice.

Since the contents of data RAM are maintained in Retention Deep Sleep, the use of the DSGPR registers to store critical data is not necessary in this mode.

#### 57.3.5.5 I/O PINS DURING DEEP SLEEP

During Deep Sleep, general purpose I/O pins retain their previous states. Pins that are configured as inputs (TRIS bit is set), prior to entry into Deep Sleep, remain high-impedance during Deep Sleep.

Pins that are configured as outputs (TRIS bit is clear), prior to entry into Deep Sleep, will remain as output pins during Deep Sleep. While in this mode, they will drive the output level determined by their corresponding LAT bit at the time of entry into Deep Sleep.

Once the device wakes back up, all I/O pins will continue to maintain their previous states, even after the device has finished the POR sequence and is executing application code again. Pins configured as inputs during Deep Sleep will remain high-impedance and pins configured as outputs will continue to drive their previous value. After waking up, the TRIS and LAT registers will be reset. If firmware modifies the TRIS and LAT values for the I/O pins, they will not immediately go to the newly configured states. Once the firmware clears the RELEASE bit (DSCON<0>), the I/O pins are "released". This causes the I/O pins to take the states configured by their respective TRIS and LAT bit values.

If the Deep Sleep BOR (DSBOR) is enabled, and a DSBOR event occurs during Deep Sleep (or VDD is hard cycled to VSS), the I/O pins will be immediately released similar to clearing the RELEASE bit. All previous state information will be lost, including the general purpose DSGPR0 and DSGPR1 contents.

If a $\overline{\text{MCLR}}$ Reset event occurs during Deep Sleep, the I/O pins will also be released automatically, but in this case, the DSGPR0 and DSGPR1 contents will remain valid.

In case of $\overline{\text{MCLR}}$ Reset and all other Deep Sleep wake-up cases, application firmware needs to clear the RELEASE bit (DSCON<0>) in order to reconfigure the I/O pins.

#### 57.3.5.6 DEEP SLEEP WATCHDOG TIMER (DSWDT)

Deep Sleep has its dedicated WDT (DSWDT). It is enabled through the DSWDTEN Configuration bit. The DSWDT is equipped with a postscaler for time-outs of 2.1 ms to 25.7 days, configurable through the Configuration bits, DSWDTPS<3:0>. Entering Deep Sleep mode automatically clears the DSWDT.

The DSWDT also has a configurable reference clock source for selecting the LPRC or SOSC. The reference clock source is configured through the DSWDTOSC Configuration bit.

Under certain circumstances, it is possible for the DSWDT clock source to be off when entering Deep Sleep mode. In this case, the clock source is turned on automatically (if DSWDT is enabled), without the need for software intervention. However, this can cause a delay in the start of the DSWDT counters. In order to avoid this delay, when using SOSC as a clock source, the application can activate SOSC prior to entering Deep Sleep mode.

#### 57.3.5.7 DEEP SLEEP LOW-POWER BROWN-OUT RESET

Devices with a Deep Sleep power-saving mode also have a dedicated BOR for Deep Sleep modes (DSBOR). It has a trip point range of 1.7V-2.3V nominal, and is enabled through the DSBOREN Configuration bit.

When the device enters a Deep Sleep mode and receives a DSBOR event, the device will not wake-up and will remain in the Deep Sleep mode. When a valid wake-up event occurs and causes the device to exit Deep Sleep mode, software can determine if a DSBOR event occurred during Deep Sleep mode by reading the DSBOR (DSCON<1>) status bit.

#### 57.3.5.8 RTCC AND DEEP SLEEP

The RTCC can operate uninterrupted during Deep Sleep modes. It can wake-up the device from Deep Sleep by configuring an alarm. The RTCC clock source is configured with the RTCOSC Configuration bit. The available reference clock sources are the LPRC and SOSC. If the LPRC is used, the RTCC accuracy will directly depend on the LPRC tolerance.

If the RTCC is not required, Deep Sleep mode, with the RTCC disabled, affords the lowest power consumption of any of the instruction-based power-saving modes.

#### 57.3.5.9 CONTROL BIT SUMMARY FOR SLEEP MODES

Table 57-5 shows the settings for the bits relevant to Deep Sleep modes.

**Table 57-5: Bit Settings for All Deep Sleep Modes**

| Instruction-Based Mode | DSEN (DSCON<15>) | Low-Voltage Regulator | | |
|---|---|---|---|---|
| | | $\overline{\text{LPCFG}}$/LVRCFG (CW1<10>)(1) | RETEN/LVREN (RCON<12>) | State |
| Retention Deep Sleep | 1 | 0 | 1 | Enabled |
| Deep Sleep | 1 | 1 | x | Disabled |

**Note 1:** This bit is also designated as LVRCFG in some devices.

#### 57.3.5.10 WAKE-UP DELAYS

The Reset delay associated with wake-up from Deep Sleep and Retention Deep Sleep modes, in different oscillator modes, are provided in Table 57-6 and Table 57-7, respectively.

**Table 57-6: Delay Times for Exiting from Deep Sleep Mode**

| Clock Source | | Exit Delay | Oscillator Delay | Notes |
|---|---|---|---|---|
| EC | | TDSWU | — | |
| ECPLL | | TDSWU | TLOCK | 1, 3 |
| XT, HS | | TDSWU | TOST | 1, 2 |
| XTPLL, HSPLL | | TDSWU | TOST + TLOCK | 1, 2, 3, 4 |
| SOSC | (Off during Sleep) | TDSWU | TOST | 1, 2 |
| | (On during Sleep) | TDSWU | — | 1 |
| FRC, FRCDIV | | TDSWU | TFRC | 1, 5 |
| LPRC | (Off during Sleep) | TDSWU | TLPRC | 1, 5 |
| | (On during Sleep) | TDSWU | — | 1 |
| FRCPLL | | TDSWU | TFRC + TLOCK | 1, 3, 5 |

**Note 1:** TDSWU = Deep Sleep wake-up delay.
**2:** TOST = Oscillator Start-up Timer; a delay of 1024 oscillator periods before the oscillator clock is released to the system.
**3:** TLOCK = PLL lock time.
**4:** HSPLL mode exceeds PIC24F maximum operating frequency.
**5:** TFRC and TLPRC are RC oscillator start-up times.

**Table 57-7: Delay Times for Exiting Retention Deep Sleep Mode**

| Clock Source | | Exit Delay | Oscillator Delay | Notes |
|---|---|---|---|---|
| EC | | TLVR + TPM | — | 1, 2, 7 |
| ECPLL | | TLVR + TPM | TLOCK | 1, 2, 4, 7 |
| XT, HS | | TLVR + TPM | TOST | 1, 2, 3, 7 |
| XTPLL, HSPLL | | TLVR + TPM | TOST + TLOCK | 1, 2, 3, 4, 5, 7 |
| SOSC | Off during Sleep | TLVR + TPM | TOST | 1, 2, 3, 7 |
| | On during Sleep | TLVR + TPM | — | 1, 2, 7 |
| FRC, FRCDIV | | TLVR + TPM | TFRC | 1, 2, 6, 7 |
| LPRC: | Off during Sleep | TLVR + TPM | TLPRC | 1, 2, 6, 7 |
| | On during Sleep | TLVR + TPM | — | 1, 2, 7 |
| FRCPLL | | TLVR + TPM | TLOCK | 1, 2, 3, 7 |

**Note 1:** TPM = Start-up delay for program memory stabilization; applicable only when PMSLP/VREGS (RCON<8>) = 0.
**2:** TLVR = Low-voltage regulator start-up delay
**3:** TOST = Oscillator Start-up Timer (OST); a delay of 1024 oscillator periods before the oscillator clock is released to the system.
**4:** TLOCK = PLL lock time.
**5:** HSPLL mode exceeds PIC24F maximum operating frequency.
**6:** TFRC and TLPRC are RC oscillator start-up times.
**7:** TFLASH = Flash program memory ready delay. Setting the PMSLP/VREGS bit will provide a faster wake-up.

**Note 1:** The PMSLP/VREGS bit (RCON<8>) may also be designated as the VREGS bit in certain PIC24F devices. The functionality of the bit, and its effect on wake-up times, remains constant regardless of the name.

**2:** Refer to the **"Electrical Characteristics"** section of the specific product data sheet for maximum operating frequency, TDSWU, TFSCM, TLOCK and oscillator start-up specification values.

## 57.4 VBAT MODE

VBAT mode is a hardware-based power mode that maintains only the most critical operations when a power loss occurs on VDD. The mode does this by powering these systems from a back-up power source connected to the VBAT pin. In this mode, the RTCC can run even when there is no power on VDD.

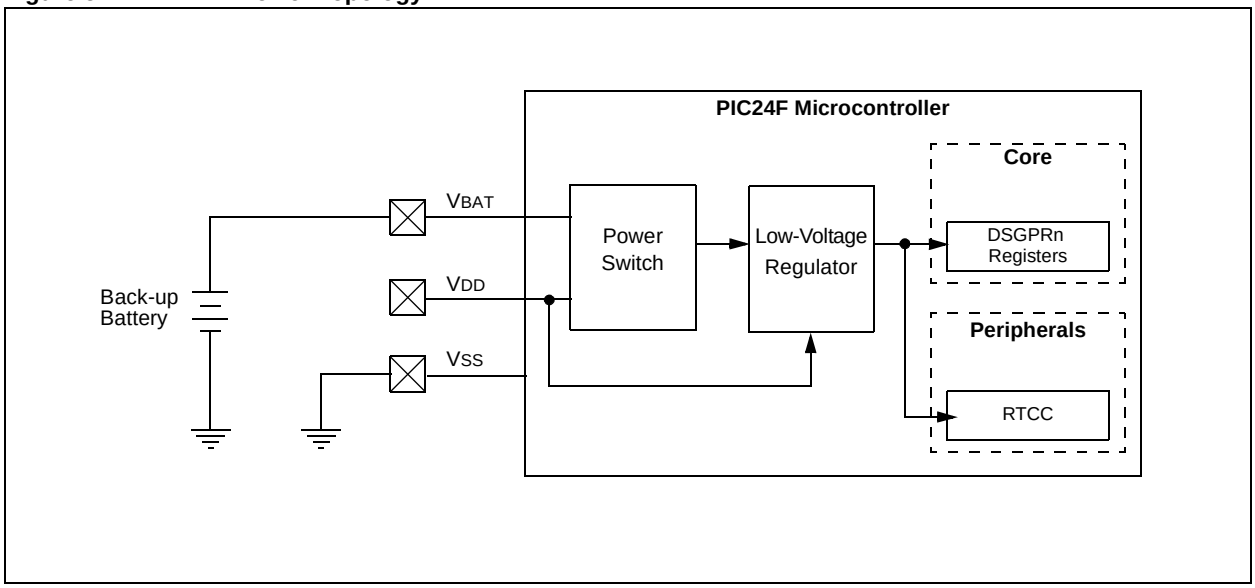
VBAT mode is entered whenever power is removed from VDD. An on-chip power switch detects the power loss from the VDD and connects the VBAT pin so it can supply the power. RTCC (if enabled) and the DSGPRn Deep Sleep Retention registers are powered in VBAT mode (Figure 57-1).

Entering VBAT mode requires that a power source, distinct from the main VDD power source, be available on VBAT and that VDD be completely removed from the VDD pin(s).

As with Deep Sleep modes, the contents of the Deep Sleep Retention (DSGPRn) registers' content are maintained. Since the power loss on VDD may be unforeseen, it is recommended to load any data to be saved in these registers in advance.

Any data stored in the DSGPR registers must be written twice (the repeat sequence). The write operations do not need to be sequential; however, back-to-back writes are a recommended programming practice.

**Figure 57-1: VBAT Power Topology**



### 57.4.1 Wake-up from VBAT Modes

When VDD is restored to the device, wake-up from VBAT mode is automatic. The device executes a POR and begins executing code from the Reset vector. If the RTCC was enabled, it will continue to run. Wake-up timing is similar to a normal Power on reset.

Wake-up from VBAT mode is identified by checking the state of the VBAT bit (RCON2<0>). If this bit is set when the device is awake and starting to execute the code from the Reset vector, it indicates that the exit was from VBAT mode. To identify future VBAT wake-up events, the bit must be cleared in software.

If a POR occurs without a power source connected to the VBAT pin, the VBPOR bit (RCON2<1>) is set. If this bit is set on a POR, it indicates that a battery needs to be connected to the VBAT pin.

In addition, if the VBAT power source falls below the level needed for Deep Sleep Semaphore operation, while in VBAT mode (e.g., the battery has been drained), the VBPOR bit will be set. VBPOR is also set when the microcontroller is powered up the very first time, even if power is supplied to VBAT

With VBPOR set, the user should clear it and the next time, this bit will only set when VDD = 0 and the VBAT pin has gone below the level (0.4V-0.6V).

If the battery on VBAT becomes depleted while the device is in VBAT mode, and falls below the threshold to maintain the Deep Sleep Retention Registers, VBPOR will also become set after VDD is restored.

### 57.4.2 Saving Context Data with the DSGPRn Registers

As exiting VBAT causes a POR, most Special Function Registers reset to their default POR values. In addition, because the core power is not supplied in VBAT mode, information in data RAM will be lost when exiting this mode. Applications which require critical data to be saved should be saved in DSGPR0 and DSGPR1. If the device has a data EEPROM, critical data can also be store there.

Any data stored to the DSGPR registers must be written twice (the repeat sequence). The write operations do not need to be sequential. However, back-to-back writes are a recommended programming practice.

After exiting VBAT mode, software can restore the data by reading the registers.

### 57.4.3 I/O Pins During VBAT Mode

All I/O pins should be maintained at VSS level; no I/O pins should be given VDD (refer to the **"Absolute Maximum Ratings"** in the **"Electrical Characteristics"** section of the device-specific data sheet) during VBAT mode. The only exceptions are the SOSCI and SOSCO pins, which maintain their states if the secondary oscillator is being used as the RTCC clock source. It is the user's responsibility to restore the I/O pins to their proper states, using the TRIS and LAT bits once VDD has been restored.

| | |
|---|---|
| **Note:** | If the VBAT mode is not used, the recommendation is to connect the VBAT pin to VDD.<br><br>When the VBAT mode is used (connected to the battery), as well as when it is not used, it is always recommended to connect a 0.1 µF capacitor from the VBAT pin to ground. The capacitor should be located very close to the VBAT pin. BOR should be enabled for reliable operation of VBAT. (It is recommended to have the BOR enabled to have reliable operation of VBAT.) |

**Register 57-1: RCON: Reset and System Control Register (Sleep and Deep Sleep Mode bits only)(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRAPR | IOPUWR | SBOREN | RETEN/LVREN | — | DPSLP(2) | CM | PMSLP/VREGS(3) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| EXTR | SWR | SWDTEN | WDTO | SLEEP(2) | IDLE(2) | BOR | POR |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 13 **SBOREN:** Software Enable/Disable of BOR bit
1 = BOR is turned on in software
0 = BOR is turned off in software

bit 12 **RETEN/LVREN:** Low-Voltage Regulator Enable bit
1 = Regulator is enabled ($\overline{\text{LPCFG}}$/LVRCFG Configuration bit must also be programmed)
0 = Regulator is disabled

bit 10 **DPSLP:** Deep Sleep Mode Flag bit(2)
1 = Deep Sleep has occurred
0 = Deep Sleep has not occurred

bit 8 **PMSLP/VREGS:** Program Memory Power During Sleep bit(3)
1 = Program memory bias voltage remains powered during Sleep
0 = Program memory bias voltage is powered down during Sleep

bit 3 **SLEEP:** Wake from Sleep Flag bit(2)
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit(2)
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

**Note 1:** Only those bits relevant to the power-saving features are described here. See **Section 7. "Reset"** in the *"PIC24F Family Reference Manual"* for a complete description of the RCON register bits.

**2:** DPSLP, SLEEP and IDLE bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**3:** This bit is also designated as VREGS in certain PIC24F devices, with the same functionality. See **Section 7. "Reset"** in the *"PIC24F Family Reference Manual"* for additional details.

**Register 57-2: RCON2: Reset and System Control Register 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | r-0 | R/CO-1 | R/CO-1 | R/CO-1 | R/CO-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | r | VDDBOR(1) | VDDPOR(1,2) | VBPOR(1,3) | VBAT(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | r = Reserved | CO = Clearable Only bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **Reserved:** Maintain as '0'

bit 3 **VDDBOR:** VDD Brown-out Reset Flag bit(1)
- 1 = A VDD Brown-out Reset has occurred (set by hardware)
- 0 = A VDD Brown-out Reset has not occurred

bit 2 **VDDPOR: VDD Power-on Reset Flag bit(1,2)**
- 1 = A VDD Power-up Reset has occurred (set by hardware)
- 0 = A VDD Power-up Reset has not occurred

bit 1 **VBPOR:** Wake from Sleep Flag bit(1,3)
- 1 = A VBAT POR has occurred (no battery is connected to the VBAT pin or VBAT power is below the Deep Sleep Semaphore retention level, set by hardware)
- 0 = A VBAT POR has not occurred

bit 0 **VBAT:** VBAT Flag bit(1)
- 1 = A POR exit has occurred while power was applied to the VBAT pin (set by hardware)
- 0 = A POR exit from VBAT has not occurred

**Note 1:** This bit is set in hardware only; it can only be cleared in software.

**2:** Indicates a VDD POR. Setting the POR bit (RCON<0>) indicates a VCORE POR.

**3:** This bit is set when the device is originally powered up, even if power is present on VBAT.

**Register 57-3: DSCON: Deep Sleep Control Register**

| R/W-0, HC | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| DSEN(1) | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HCS(2) | R/W-0, HS(2) |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | DSBOR | RELEASE(4) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | HCS = Hardware Clearable/Settable bit |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **DSEN:** Deep Sleep Mode Enable bit(1)
1 = Deep Sleep mode is entered on a SLEEP command
0 = Sleep mode is entered on a SLEEP command

bit 14-2 **Unimplemented:** Read as '0'

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit(2)
1 = DSBOREN was enabled and VDD dropped below the DSBOR threshold during Deep Sleep(3)
0 = DSBOREN was disabled, or VDD did not drop below the DSBOR threshold during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit(2,4)
1 = Upon waking from Deep Sleep, the I/O pins maintain their previous states
0 = Release I/O pins and allow their respective TRIS and LAT bits to control their states

**Note 1:** In order to enter Deep Sleep, DSEN must be written to in two separate operations. The write operations do not need to be consecutive.

**2:** This is the value when VDD is initially applied.

**3:** Unlike all other events, a Deep Sleep BOR event will not cause a wake-up from Deep Sleep; this bit is present only as a status bit.

**4:** The RELEASE bit should be cleared before setting the DSEN bit.

**Register 57-4: DSWAKE: Deep Sleep Wake-up Source Register(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HS |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | DSINT0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0, HS | U-0 | U-0 | R/W-0, HS | R/W-0 | R/W-0, HS | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DSFLT | — | — | DSWDT | DSRTC | DSMCLR | — | DSPOR(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **DSINT0:** Interrupt-on-Change bit
1 = Interrupt-on-change was asserted during Deep Sleep
0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 **DSFLT:** Deep Sleep Fault Detected bit
1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted
0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **DSWDT:** Deep Sleep Watchdog Timer Time-out bit
1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep
0 = The Deep Sleep Watchdog Timer did not time-out during Deep Sleep

bit 3 **DSRTC:** Real-Time Clock and Calendar Alarm bit
1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep
0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 **DSMCLR:** $\overline{\text{MCLR}}$ Event bit
1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep
0 = The $\overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1 **Unimplemented:** Read as '0'

bit 0 **DSPOR:** Deep Sleep Fault Detected bit(2)
1 = The $V_{DD}$ supply POR circuit was active and a POR event was detected
0 = The $V_{DD}$ supply POR circuit was not active, or was active, but did not detect a POR event

**Note 1:** To be set in software, all bits in DSWAKE must be written to twice. The write operations do not need to be consecutive.

**2:** Unlike the other bits in this register, this bit can be set outside of Deep Sleep.

## 57.5 MICROCONTROLLER CLOCK MANIPULATION

In general, reducing the microcontroller clock speed for any application will result in a power saving that is roughly proportional to the clock frequency reduction. PIC24F devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can switch between low-power operation from an internal RC oscillator, or high-speed and high-precision operation from a crystal oscillator, by simply changing the NOSC Configuration bits. In fact, users can choose between up to five different oscillators at any time, allowing a maximum amount of flexibility in configuring application speed, frequency precision and power consumption.

The process of changing the system clock during operation, as well as restrictions on clock changes, are discussed in more detail in the *"PIC24F Family Reference Manual"*, **Section 6. "Oscillator"**.

| | |
|---|---|
| **Note:** | Oscillator availability varies by device. Refer to the device data sheet to determine what oscillators are available. |

## 57.6 DOZE MODE

Changing clock speed and invoking one of the Instruction-Based Power-Saving modes are effective strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a Power-Saving mode may stop communications completely.

Doze mode provides an alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the Special Function Registers (SFRs) while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default. For CLKDIV register values, refer to the appropriate oscillator section in the *"PIC24F Family Reference Manual"*.

### 57.6.1 Return from Doze on Interrupt

Doze mode can be configured to automatically return to full-speed CPU execution on an interrupt event. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, the ROI bit is cleared and interrupt events have no effect on Doze mode operation. When an interrupt event occurs in Doze mode, and ROI is set, the DOZEN bit is automatically cleared.

The return from Doze mode feature allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU executes at a much lower speed, waiting for an event to invoke an interrupt routine and resume processing.

## 57.7 SELECTIVE PERIPHERAL POWER CONTROL

Sleep, Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume some amount of power. There may be cases where the application needs what these modes do not provide: the ability to allocate limited power resources to the CPU while eliminating power consumption from the peripherals. PIC24F devices address this requirement by allowing peripheral modules to be selectively enabled or disabled, reducing or eliminating their power consumption.

### 57.7.1 Disabling Peripheral Modules

Most of the peripheral modules in the PIC24F family architecture can be selectively disabled, reducing or essentially eliminating their power consumption during all operating modes. Two different options are available to users, each with a slightly different effect.

#### 57.7.1.1 MODULE ENABLE BIT (XXXEN)

Many peripheral modules have a Module Enable bit, generically named, “XXXEN”, usually located in Bit Position 15 of their control registers (or primary control registers for more complex modules). Here, “XXX” represents the mnemonic form for the module of the module name. For example, the enable bit for an SPI module is “SPIEN”, and so on. The bit is provided for all serial and parallel communications modules and the Real-Time Clock (RTC). Clearing this bit disables the module’s operation; however, it continues to receive clock signals and draw a minimal amount of current.

As with all earlier PIC® MCU devices, timers continue to be under selective operation and are controlled by their own TON bit, also located in position 15. The A/D Converter also has a legacy enable bit, ADON, that has the same function as the XXXEN bits. I/O ports and features associated with them, such as input change notification and input capture, do not have their own module enable bits, since their operation is secondary to other modules.

Disabling modules not required for a particular application, in this manner, allows for the selective and dynamic adjusting power consumption, under software control, as the application is running.

#### 57.7.1.2 PERIPHERAL MODULE DISABLE BIT (XXMD)

All peripheral modules (except for I/O ports) also have a second control bit that can disable their functionality. These bits, known as the Peripheral Module Disable (PMD) bits, are generically named: “XXMD” (using “XX” as the mnemonic version of the module’s name, as shown in **Section 57.7.1.1 “Module Enable Bit (XXXEN)”**). These bits are located in the PMDx SFRs. In contrast to the module enable bits, the XXMD bit must be set (= 1) to disable the module.

While the PMD and module enable bits both disable a peripheral’s functionality, the PMD bit completely shuts down the peripheral, effectively powering down all circuits and removing all clock sources. This has the additional effect of making any of the module’s control and buffer registers, mapped in the SFR space, unavailable for operations. In other words, when the PMD bit is used to disable a module, the peripheral ceases to exist until the PMD bit is cleared. This differs from using the module enable bit, which allows the peripheral to be reconfigured and buffer registers preloaded, even when the peripheral’s operations are disabled.

The PMD bit is most useful in highly power-sensitive applications, where even tiny savings in power consumption can determine the ability of an application to function. In these cases, the bits can be set before the main body of the application to remove those peripherals that will not be needed at all.

### 57.7.2 Selective Disabling of Modules in Idle Mode

To achieve additional power savings, peripheral modules can be selectively disabled whenever the device enters Idle mode. This is done with the Stop in Idle (SIDL) control bit, which is generally located in Bit Position 13 of the control register of most peripheral modules. The generic name format is “XXXSIDL” (using “XXX” as the mnemonic version of the module’s name, as before). The Stop in Idle feature allows further reduction of power consumption during Idle mode, enhancing power savings for extremely critical power applications.

Almost all peripheral modules have a Stop in Idle bit, including modules that lack a module enable bit (e.g., input capture and output compare). The Real-Time Clock module is the exception, as it is assumed that an application involving a Real-Time Clock will need to keep the module running continuously.

## 57.8 REGISTER MAPS

A summary of the registers associated with the PIC24F power-saving features and Deep Sleep mode operation is shown in Table 57-8.

**Table 57-8: Power-Saving Features of Register Map**

| File Name | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RCON | TRAPR | IOPUWR | SBOREN | RETEN/LVREN | — | DPSLP | — | PMSL/VREGSP(1) | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | xxxx(2) |
| CLKDIV | ROI | DOZE2 | DOZE1 | DOZE0 | DOZEN | RCDIV2 | RCDIV1 | RCDIV0 | — | — | — | — | — | — | — | — | 0300 |
| PMDx(3) | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | XXMD | 0000 |
| DSCON | DSEN | — | — | — | — | — | — | — | — | — | — | — | — | — | DSBOR | RELEASE | xxxx |
| DSWAKE | — | — | — | — | — | — | — | DSINT0 | DSFLT | — | — | DSWDT | DSRTC | DSMCLR | — | DSPOR | xxxx |
| DSGPR0 | Deep Sleep Persistent General Purpose bits | | | | | | | | | | | | | | | | xxxx |
| DSGPR1 | Deep Sleep Persistent General Purpose bits | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is also designated as VREGS in certain PIC24F devices. See **Section 7. "Resets"** in the *"PIC24F Family Reference Manual"* for more information.

**2:** The RCON register Reset values are dependent on the type of Reset.

**3:** The number of PMD registers and the location of individual bits are device-specific. Refer to the specific device data sheet for information.

## 57.9 DESIGN TIPS

**Question 1:** ***What should my software do before entering Sleep, Deep Sleep or Idle mode?***

**Answer:** Make sure that the sources intended to wake-up the device have their IE bits set. In addition, make sure that the particular source of interrupt has the ability to wake up the device. Some sources do not function when the device is in Sleep mode.

If the device is to be placed in Idle mode, make sure that the 'Stop in Idle' control bit for each device peripheral is properly set. These control bits determine whether the peripheral will continue operation in Idle mode. See the individual peripheral sections of this manual for further details.

If entering Deep Sleep mode, remember that the SFRs, RAM and program counter will be lost. Be sure to store any relevant device state information in the DSGPRn registers. These are the only SFRs that will retain their value after the device wakes up. The stored data can be used to restore the state of the device.

**Question 2:** ***How can I tell which peripheral woke the device from Sleep, Deep Sleep or Idle mode?***

**Answer:** You can poll the IF bits for each enabled interrupt source to determine the source of wake-up. When waking up from Deep Sleep mode, poll the bits in the DSWAKE and RCON registers to determine the wake-up source.

## 57.10 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Power-Saving Features with Deep Sleep of PIC24F devices are:

| Title | Application Note # |
|---|---|
| Low-Power Design using PICmicro® Microcontrollers | AN606 |

**Note:** Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

## 57.11 REVISION HISTORY

### Revision A (November 2011)

This is the initial released revision of this document.

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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