Section 56. RTCC with External Power Control

HIGHLIGHTS

This section of the manual contains the following major topics:

56.1 INTRODUCTION

This section discusses the Real-Time Clock and Calendar (RTCC) hardware module with External Power Control. This module, available on select PIC24F devices, offers these key features:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (Military Time)
- Calendar: Weekday, Date, Month and Year
- Year Range: 2000 to 2099, with Leap Year Correction
- BCD Format for Compact Firmware
- Versatile Alarm Configuration
- Output Configurable for Alarm, Seconds Pulse or External Device Control
- Optimized for Low-Power Operation
- Configurable for Crystal-Controlled Oscillator Source or Mains Power for Time Base
- User Calibration with Auto-Adjust
- Calibration Range: ±2.64 Seconds Error per Month
- Alarm Pulse or Seconds Clock Output on RTCC pin

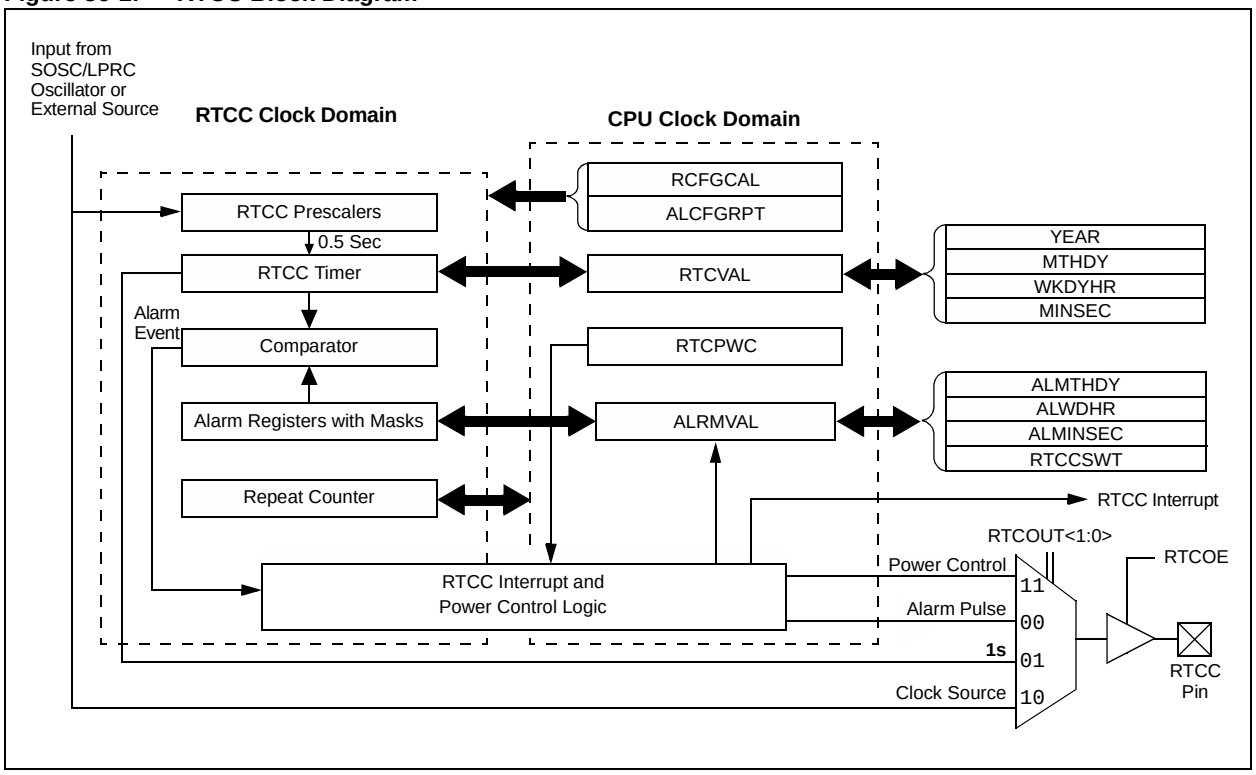
This module provides a Real-Time Clock and Calendar (RTCC) with extended control functions for applications where accurate time must be maintained, for extended periods of time, with minimum to no intervention from the CPU. It is optimized for low-power usage in order to provide extended battery lifetime while keeping track of time.

The RTCC is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099. The hours are available in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

In addition to the RTCC, the module provides the ability to directly control external devices with the configurable alarm output. This gives the option to periodically wake-up hardware without actually waking the microcontroller to execute code.

A simplified block diagram is shown in Figure 56-1.

Figure 56-1: RTCC Block Diagram



56.2 RTCC MODULE REGISTERS

The RTCC module uses five memory mapped, directly addressable registers. Eight additional registers, used to hold time and alarm values, are addressable only through the memory mapped registers.The registers are organized into three categories:

RTCC Control Registers

- RCFGCAL
- RTCPWC
- ALCFGRPT

RTCC Value Registers

- RTCVAL, which is used to address these virtual time registers:
  - YEAR
  - MTHDY
  - WKDYHR
  - MINSEC

Alarm Value Registers

- ALRMVAL, which is used to address these virtual alarm and Power Control registers:
  - ALMTHDY
  - ALWDHR
  - ALMINSEC
  - RTCCSWT

Note:	For reference purposes, the upper half of the RTCVAL register will be referred to as RTCVAL<15:8> and the lower half as RTCVAL<7:0>. The same applies to ALRMVAL, where the upper half is ALRMVALH and the lower half is ALRMVALL.

56.2.1 Register Write Lock

In order to perform a write to the RCFGCAL, RTCPWC or RTCVAL registers, the RTCWREN bit (RCFGCAL<13>) must be set first. This is required to prevent spurious changes to any time control or time value registers. Any attempt to write to any bits of the RCFGCAL register, including the module enable bit (RCFGCAL<15>), will be ignored as long as RTCWREN = 0.

Setting the RTCWREN bit requires an unlock sequence, writing two bytes consecutively to the NVMKEY register. A sample assembly sequence is shown in Example 56-1. Once set, RTCWREN remains set until it is cleared.

In general, writes to the ALCFGRPT and ALRMVAL registers are not affected by the RTCWREN bit. However, RTCWREN must be set when the ALRMVAL register points to the RTCCSWT (power stability/sampling) register.

Example 56-1: Setting the RTCWREN Bit

```
MOV    #NVMKEY, W1        ;move the address of NVMKEY into W1
MOV    #0x55, W2
MOV    W2, [W1]           ;start 55/AA sequence
MOV    #0xAA, W3
MOV    W3, [W1]
BSET   RCFGCAL, #13       ;set the RTCWREN bit
```

Note:	To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL<13>) is kept clear at any other time. For the RTCWREN bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN; therefore, it is recommended that the code example in Example 56-1 be followed.

56.2.2 RTCC Control Registers

Register 56-1: RCFGCAL: RTCC Calibration and Configuration Register(1)

R/W-0	U-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
RTCEN(2)	—	RTCWREN	RTCSYNC	HALFSEC(3)	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **RTCEN:** RTCC Enable bit(2)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
1 = RTCVAL and RTCPWC registers can be written to by the user
0 = RTCVAL and RTCPWC registers are locked out from being written to by the user

bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = RTCVAL<15:8>, RTCVAL<7:0> and ALCFGRPT registers can change while reading due to a rollover ripple resulting in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = RTCVAL<15:8>, RTCVAL<7:0> or ALCFGRPT registers can be read without concern over a rollover ripple

bit 11 **HALFSEC:** Half-Second Status bit(3)
1 = Second half period of a second
0 = First half period of a second

bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled
0 = RTCC clock output is disabled

bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Window Pointer bits
Points to the corresponding RTCC Value registers when reading RTCVAL<15:8> and RTCVAL<7:0> registers. The RTCPTR<1:0> value decrements on every read or write of RTCVAL<15:8> until it reaches '00'.
RTCVAL<15:8>:
00 = MINUTES
01 = WEEKDAY
10 = MONTH
11 = Reserved
RTCVAL<7:0>:
00 = SECONDS
01 = HOURS
10 = DAY
11 = YEAR

Note 1: The RCFGCAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

Register 56-1: RCFGCAL: RTCC Calibration and Configuration Register(1) (Continued)

bit 7-0 **CAL<7:0>:** RTC Drift Calibration bits

01111111 = Maximum positive adjustment; adds 127 RTC clock pulses every 15 seconds

...

00000001 = Minimum positive adjustment; adds 1 RTC clock pulses every 15 seconds
00000000 = No adjustment
11111111 = Minimum negative adjustment; subtracts 1 RTC clock pulses every 15 seconds

...

10000000 = Maximum negative adjustment; subtracts 128 RTC clock pulses every 15 seconds

Note 1: The RCFGCAL register is only affected by a POR.

2: A write to the RTCEN bit is only allowed when RTCWREN = 1.

3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

Register 56-2: RTCPWC: RTCC Power Control Register(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCEN	PWCPOL	PWCCPRE	PWCSPRE	RTCLK1(3)	RTCLK0(3)	RTCOUT1	RTCOUT0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWCEN:** Power Control Enable bit
1 = Power Control is enabled
0 = Power Control is disabled

bit 14 **PWCPOL:** Power Control Polarity bit
1 = Power Control output is active-high
0 = Power Control output is active-low

bit 13 **PWCCPRE:** Power Control Stability Prescaler bits
1 = PWC Stability Window Clock is divide-by-2 of source RTCC clock
0 = PWC Stability Window Clock is divide-by-1 of source RTCC clock

bit 12 **PWCSPRE:** Power Control Sample Prescaler bits
1 = PWC Sample Window Clock is divide-by-2 of source RTCC clock
0 = PWC Sample Window Clock is divide-by-1 of source RTCC clock

bit 11-10 **RTCLK<1:0>:** RTCC Clock Source Select bits(3)
11 = External Power Line Source (60 Hz)
10 = External Power Line Source (50 Hz)
01 = Internal LPRC Oscillator
00 = External Secondary Oscillator (SOSC)

bit 9-8 **RTCOUT<1:0>:** RTCC Output Source Select bits
11 = Power Control
10 = RTCC Clock
01 = RTCC Seconds Clock
00 = RTCC Alarm Pulse

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: A write to this register is only allowed when RTCWREN = 1.
2: The RTCPWC register is only affected by a POR.
3: When a new value is written to these register bits, the lower half of the MINSEC register should also be written to properly reset the clock prescalers in the RTCC.

Register 56-3: ALCFGRPT: Alarm Configuration Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 00 and CHIME = 0)
0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit

1 = Chime is enabled; ARPT<7:0> bits are allowed to roll over from 00h to FFh
0 = Chime is disabled; ARPT<7:0> bits stop once they reach 00h

bit 13-10 **AMASK<3:0>:** Alarm Mask Configuration bits

11xx = Reserved – do not use
101x = Reserved – do not use
1001 = Once a year (except when configured for February 29th, once every 4 years)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half second

bit 9-8 **ALRMPTR<1:0>:** Alarm Value Register Window Pointer bits

Points to the corresponding Alarm Value registers when reading the ALRMVALH and ALRMVALL registers; the ALRMPTR<1:0> value decrements on every read or write of ALRMVALH until it reaches '00'.

ALRMVAL<15:8>:
00 = ALRMMIN
01 = ALRMWD
10 = ALRMMNTH
11 = PWCSTAB

ALRMVAL<7:0>:
00 = ALRMSEC
01 = ALRMHR
10 = ALRMDAY
11 = PWCSAMP

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits

11111111 = Alarm will repeat 255 more times
...
00000000 = Alarm will not repeat

The counter decrements on any alarm event. The counter is prevented from rolling over from 00h to FFh unless CHIME = 1.

56.2.3 RTCVAL Register Mappings

Register 56-4: YEAR: Year Value Register(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit; Contains a value from 0 to 9

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit; Contains a value from 0 to 9

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

Register 56-5: MTHDY: Month and Day Value Register(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit; Contains a value of 0 or 1

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit; Contains a value from 0 to 9

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal value of Day's Tens Digit; Contains a value from 0 to 3

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit; Contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

Register 56-6: WKDYHR: Weekday and Hours Value Register(1)

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit; Contains a value from 0 to 6

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit; Contains a value from 0 to 2

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit; Contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

Register 56-7: MINSEC: Minutes and Seconds Value Register

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit; Contains a value from 0 to 5

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit; Contains a value from 0 to 9

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit; Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit; Contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

56.2.4 ALRMVAL Register Mappings

Register 56-8: ALMTHDY: Alarm Month and Day Value Register

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month’s Tens Digit; Contains a value of 0 or 1

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month’s Ones Digit; Contains a value from 0 to 9

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day’s Tens Digit; Contains a value from 0 to 3

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day’s Ones Digit; Contains a value from 0 to 9

Register 56-9: ALWDHR: Alarm Weekday and Hours Value Register

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit; Contains a value from 0 to 6

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour’s Tens Digit; Contains a value from 0 to 2

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour’s Ones Digit; Contains a value from 0 to 9

Register 56-10: ALMINSEC: Alarm Minutes and Seconds Value Register

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit; Contains a value from 0 to 5

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit; Contains a value from 0 to 9

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit; Contains a value from 0 to 5

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit; Contains a value from 0 to 9

Register 56-11: RTCCSWT: Power Control and Sample Window Timer Registers(1)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PWCSTAB7	PWCSTAB6	PWCSTAB5	PWCSTAB4	PWCSTAB3	PWCSTAB2	PWCSTAB1	PWCSTAB0
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PWCSAMP7	PWCSAMP6	PWCSAMP5	PWCSAMP4	PWCSAMP3	PWCSAMP2	PWCSAMP1	PWCSAMP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PWCSTAB<7:0>:** Power Control Stability Window Timer bits
11111111 = Stability Window is 255 TPWCCLK clock periods
11111110 = Stability Window is 254 TPWCCLK clock periods
...
00000001 = Stability Window is 1 TPWCCLK clock period
00000000 = No Stability Window; Sample Window starts when the alarm event triggers

bit 7-0 **PWCSAMP<7:0>:** Power Control Sample Window Timer bits(2)
11111111 = Sample Window is always enabled, even when PWCEN = 0
11111110 = Sample Window is 254 TPWCCLK clock periods
...
00000001 = Sample Window is 1 TPWCCLK clock period
00000000 = No Sample Window

Note 1: A write to this register is only allowed when RTCWREN = 1.

2: The Sample Window always starts when the Stability Window timer expires, except when its initial value is 00h. See **Section 56.5.2.2 "Modes of Operation"** for additional information.

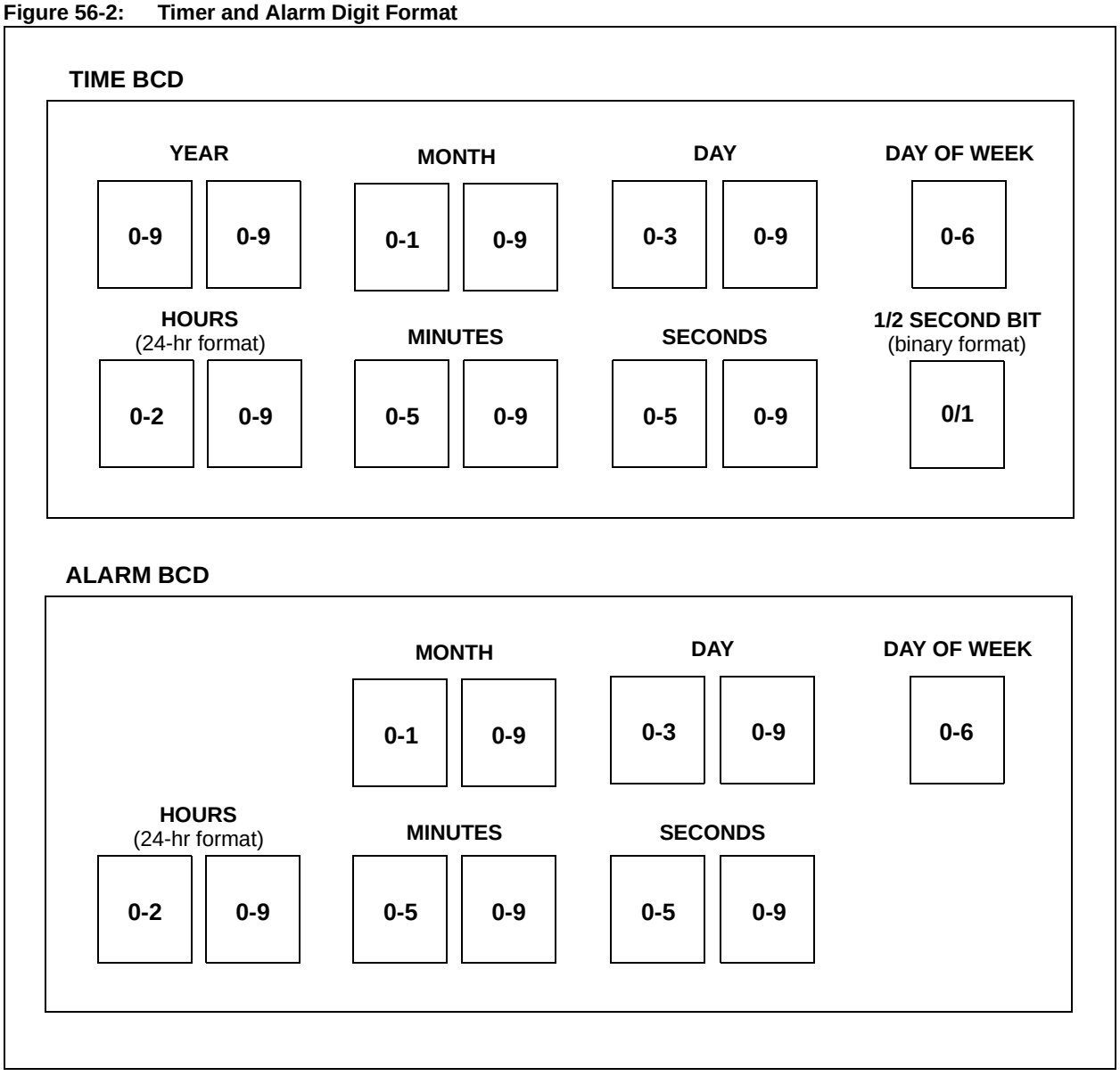
56.3 OPERATION

56.3.1 Register Interface

The register interface for the RTCC and alarm values is implemented using the Binary Coded Decimal (BCD) format. This simplifies the firmware, when using the module, as each of the digit values is contained within its own 4-bit value (see Figure 56-2).

Note:	When the ALRMVAL register points to the RTCCSWT register (PWCSTAB<7:0> and PWCSAMP<7:0>), the values reported are straight 8-bit binary and NOT 4-bit BCD.

Figure 56-2: Timer and Alarm Digit Format



56.3.2 Clock Source

The RTCC with Power Control is designed to operate from any one of three clock sources: the crystal-controlled Secondary Oscillator (SOSC), the internal RC 31 kHz oscillator (LPRC) or a clock signal derived from AC mains power. Each option provides users with choices of application component count and accuracy over time.

The clock source is selectable in software by using the RTCLK<1:0> bits (RTCPWC<11:10>). These bits select the correct prescaler for the clock divider chain, as shown in Figure 56-3.

When the crystal-controlled SOSC is used as the source, calibration of the crystal can be accomplished through this module yielding an error of 3 seconds or less, per month. See **Section 56.3.8 "Calibration"** for further details.

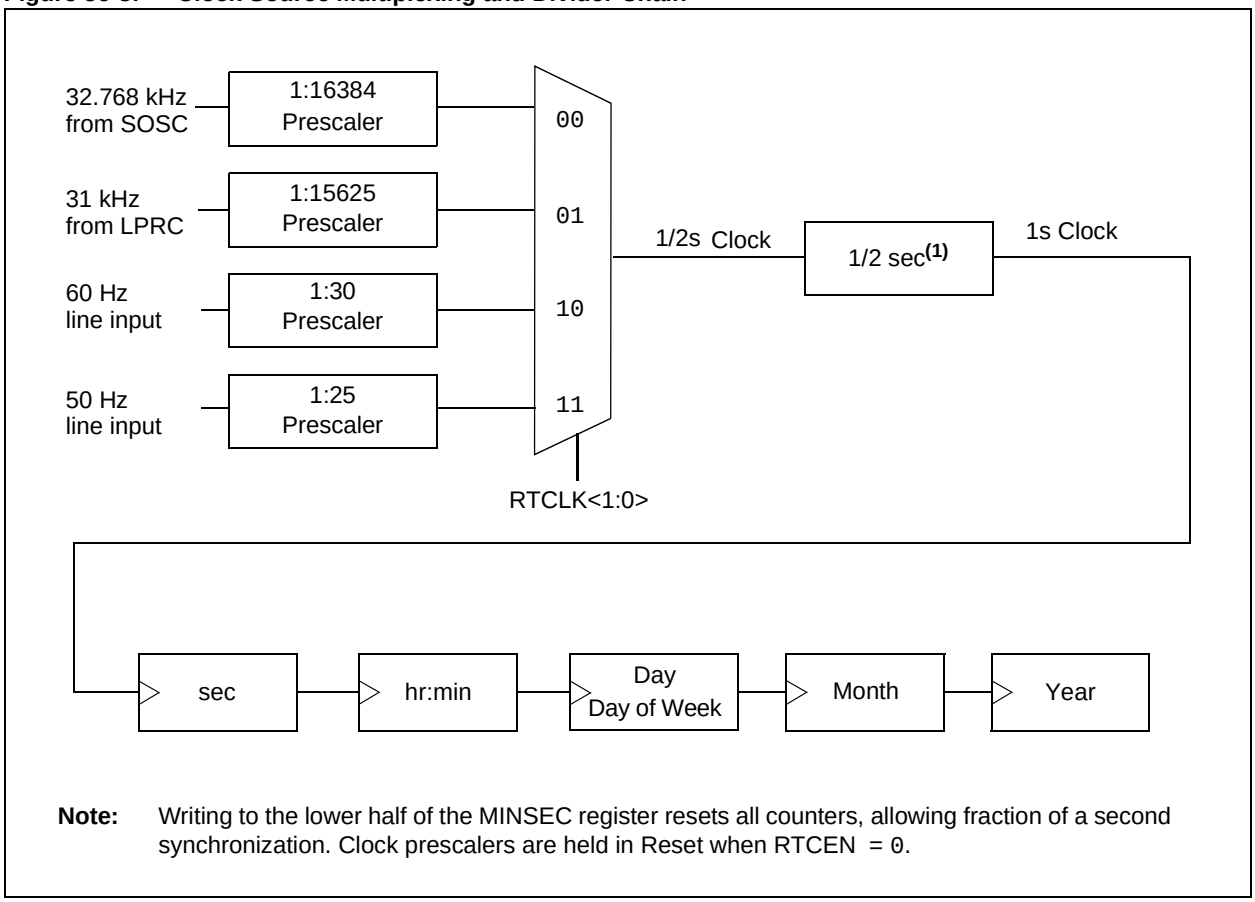
56.3.2.1 SECONDARY OSCILLATOR (SOSC) ENABLE

If the RTCC is configured to be clocked by the Secondary Oscillator, it will automatically be enabled when the RTCC is enabled. The SOSCEN bit (OSCON<1>) does not need to be set. For more information on the Secondary Oscillator, refer to **Section 6. "Oscillator"**.

56.3.2.2 LOW-POWER RC OSCILLATOR ENABLE

If the RTCC is configured to be clocked by LPRC, the LPRC will automatically be enabled. Refer to **Section 6. "Oscillator"** for more information on the LPRC.

Figure 56-3: Clock Source Multiplexing and Divider Chain



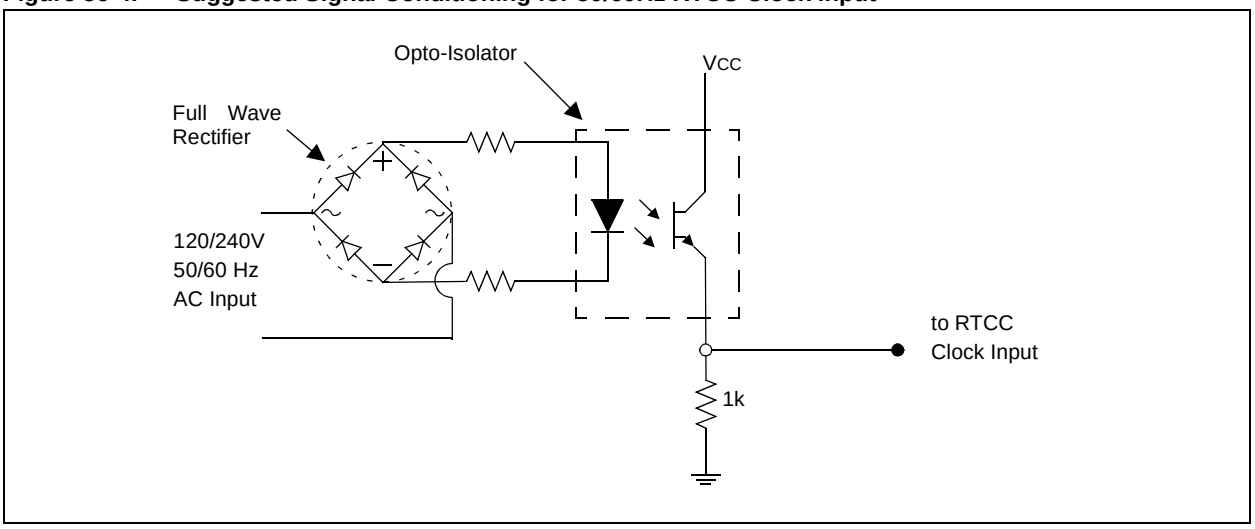
Note: Writing to the lower half of the MINSEC register resets all counters, allowing fraction of a second synchronization. Clock prescalers are held in Reset when RTCEN = 0.

56.3.2.3 CLOCK SOURCE FROM POWER LINE (50/60 Hz SIGNAL)

It is also possible to use the power mains as an external clock source for the RTCC. The module can use either 50 or 60 Hz AC, to accommodate local power in most locations throughout the world. The RTCLK<1:0> bits are used to configure the module for the correct line frequency.

Line voltage cannot be used directly to provide the clock reference; it must be conditioned to provide a logic level signal. Figure 56-4 shows the recommended signal conditioning circuit for such a clock source.

Figure 56-4: Suggested Signal Conditioning for 50/60Hz RTCC Clock Input



56.3.3 General Functionality

All Timer registers containing a time value of seconds or greater are writable. The user can configure the time by simply writing to these registers the desired year, month, day, hour, minutes and seconds via Register Pointers (see **Section 56.3.7 "Register Mapping"**). The timer will then use the newly written values and proceed with the count from the desired starting point. The RTCC module is enabled by setting the RTCEN bit (RCFGCAL<15>). If enabled while adjusting these registers, the timer will still continue to increment. However, any time the MINSEC register is written to, both of the timer prescalers are reset to '0'. This allows fraction of a second synchronization.

The Timer registers are updated in the same cycle as the write instruction is executed by the CPU. The user is responsible to assure that when RTCEN = 1, the updated registers will not be incremented at the same time. This can be accomplished in several ways:

- Checking the RTCSYNC bit (RCFGCAL<12>)
- Checking the preceding digits from which a carry can occur
- Updating the registers immediately following the seconds pulse (or alarm interrupt)

The user has visibility to the half-second field of the counter. This value is read-only and can only be reset by writing to the lower half of the MINSEC register.

56.3.4 Digit Carry Rules

This section explains which timer values are affected when there is a rollover.

- Time of Day: from 23:59:59 to 00:00:00 with a carry to the day field
- Month: from 12/31 to 01/01 with a carry to the year field
- Day of Week: from 6 to 0 with no carry (refer to Table 56-1)
- Year Carry: from 99 to 00; this also surpasses the use of the RTCC

Refer to Table 56-2 for the day to month rollover schedule.

Considering that the following values are in BCD format, the carry to the upper BCD digit will occur at a count of 10 and not a count of 16 (SECONDS, MINUTES, HOURS, WEEKDAY, DAYS, MONTHS).

Table 56-1: Day of Week Schedule

Day of Week	Value
Sunday	0
Monday	1
Tuesday	2
Wednesday	3
Thursday	4
Friday	5
Saturday	6

Table 56-2: Day to Month Rollover Schedule

Month	Maximum Day Field
01 (January)	31
02 (February)	28 or 29 (see **Section 56.3.5 “Leap Year”**)
03 (March)	31
04 (April)	30
05 (May)	31
06 (June)	30
07 (July)	31
08 (August)	31
09 (September)	30
10 (October)	31
11 (November)	30
12 (December)	31

56.3.5 Leap Year

Since the year range on the RTCC module is 2000 to 2099, the leap year calculation is determined by any year divisible by 4 in the above range. The only month to be affected in a leap year is February. The month of February will have 29 days in a leap year, while any other year, it will have 28 days.

56.3.6 Safety Window for Register Reads and Writes

The RTCSYNC bit indicates a time window during which the RTCC clock domain registers can be safely read and written without concern about a rollover. When RTCSYNC = 0, the registers can be safely accessed by the CPU. Whether RTCSYNC = 1 or 0, the user should employ a firmware solution to assure that the data read did not fall on a rollover boundary, resulting in an invalid or partial read. This firmware solution would consist of reading each register twice and then comparing the two values. If the two values match, then a rollover did not occur.

56.3.7 Register Mapping

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding Register Pointers. The RTCC Value register window (RTCVAL<15:8> and RTCVAL<7:0>) uses the RTCPTR bits (RCFGCAL<9:8>) to select the desired Timer register pair (see Table 56-3).

By reading or writing the RTCVAL<15:8> register, the RTCC Pointer value, RTCPTR<1:0>, decrements by one until it reaches '00'. Once it reaches '00', the MINUTES and SECONDS value will be accessible through RTCVAL<15:8> and RTCVAL<7:0> until the pointer value is manually changed.

Table 56-3: RTCVAL Register Mapping

RTCPTR<1:0>	RTCC Value Register Window	
	RTCVAL<15:8>	RTCVAL<7:0>
00	MINUTES	SECONDS
01	WEEKDAY	HOURS
10	MONTH	DAY
11	—	YEAR

The Alarm Value register window (ALRMVALH and ALRMVALL) uses the ALRMPTR bits (ALCFGRPT<9:8>) to select the desired Alarm register pair (see Table 56-4).

By reading or writing the ALRMVALH register, the Alarm Pointer value, ALRMPTR<1:0>, decrements by one until it reaches '00'. Once it reaches '00', the ALRMMIN and ALRMSEC value will be accessible through ALRMVALH and ALRMVALL until the pointer value is manually changed.

Table 56-4: ALRMVAL Register Mapping

ALRMPTR<1:0>	Alarm Value Register Window	
	ALRMVAL<15:8>	ALRMVAL<7:0>
00	ALRMMIN	ALRMSEC
01	ALRMWD	ALRMHR
10	ALRMMNTH	ALRMDAY
11	PWCSTAB	PWCSAMP

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL register, it will decrement the ALRMPTR<1:0> value. The same applies to the RTCVAL<15:8> or RTCVAL<7:0> register with the RTCPTR<1:0> being decremented.

Note: This only applies to read operations and not write operations. Write operations can be byte-specific.

56.3.8 Calibration

When SOSC is used as the clock source, the crystal input can be calibrated using the periodic auto-adjust feature. When properly calibrated, the RTCC can provide an error of less than 3 seconds per month. This is accomplished by finding the number of error clock pulses and storing the value into the lower half of the RCFGCAL register. The 8-bit signed value loaded into the lower half of RCFGCAL will be either added or subtracted from the RTCC timer, once every 15 seconds. Refer to the steps below for RTCC calibration:

1. Using another timer resource on the device, determine the actual frequency of the 32.768 kHz crystal.
2. Once the error is known, convert this figure to the number of error clock pulses per minute:

   (Ideal Frequency (32,758) – Measured Frequency) * 60 = Error Clocks per Minute

3. a) If the oscillator is *faster* than ideal (negative result from step 2), the RCFGCAL register value needs to be negative. This causes the specified number of clock pulses to be subtracted from the timer counter, once every 15 seconds.

   b) If the oscillator is *slower* than ideal (positive result from step 2), the RCFGCAL register value needs to be positive. This causes the specified number of clock pulses to be added to the timer counter, once every 15 seconds.
4. Load the RCFGCAL register with the correct value.

Writes to the lower half of the RCFGCAL register should only occur when the timer is turned off, or immediately after the rising edge of the seconds pulse.

Note:	It is up to the user to include in the error value the initial error of the crystal drift due to temperature and drift due to crystal aging.

56.4 ALARM

The alarm function of the RTCC has these features:

- Configurable for events from one-half second to one year
- One-time alarm and repeat alarm options available
- Enabled using the ALRMEN bit (ALCFGRPT<15>, Register 56-3)

56.4.1 Configuring the Alarm

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. This bit will not be cleared if the CHIME bit = 1, or if the lower half of ALCFGRPT ≠ 00.

The interval selection of the alarm is configured through the AMASK bits (ALCFGRPT<13:10>), see Figure 56-5. These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur. The alarm can also be configured to repeat based on a pre-configured interval. The amount of times this occurs, once the alarm is enabled, is stored in the lower half of the ALCFGRPT register.

Note:	Changing any of the registers, other then the RCFGCAL and ALCFGRPT registers and the CHIME bit while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0). It is recommended that the ALCFGRPT register and CHIME bit be changed when RTCSYNC = 0.

Figure 56-5: Alarm Mask Settings

Alarm Mask Setting AMASK<3:0>	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 – Every half second 0001 – Every second						
0010 – Every 10 seconds						s
0011 – Every minute						s s
0100 – Every 10 minutes					m	s s
0101 – Every hour					m m	s s
0110 – Every day				h h	m m	s s
0111 – Every week	d			h h	m m	s s
1000 – Every month			d d	h h	m m	s s
1001 – Every year(1)		m m	d d	h h	m m	s s

Note 1: Annually, except when configured for February 29.

When ALCFGRPT = 00 and the CHIME bit = 0 (ALCFGRPT<14>), the repeat function is disabled and only a single alarm will occur. The alarm can be repeated up to 255 times by loading the lower half of the ALCFGRPT register with FFh.

After each alarm is issued, the ALCFGRPT register is decremented by one. Once the register has reached '00', the alarm will be issued one last time, after which, the ALRMEN bit will be cleared automatically and the alarm will turn off. Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the ALCFGRPT register reaches '00', it will roll over to FF and continue counting indefinitely when CHIME = 1.

56.4.2 Alarm Interrupt

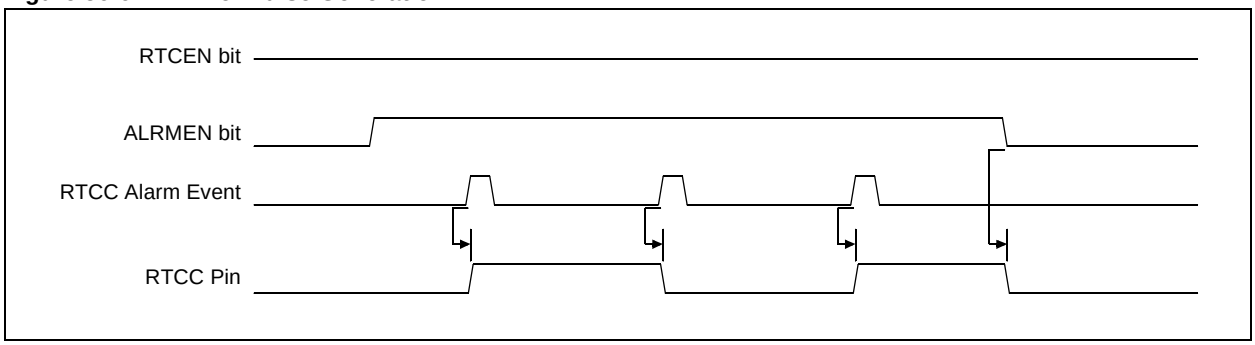
The RTCC module generates only one interrupt based on the alarm. At every alarm event, the RTCIF bit is set. The RTCIE bit determines if a device level interrupt is generated.

56.4.3 Alarm Output

When the RTCC output control bits are both cleared (RTCPWC<9:8> = 00), the RTCC output pin provides an alarm pulse output. The output pulse is a clock with a 50% duty cycle and a frequency half that of the alarm event (see Figure 56-6). This output is completely synchronous to the RTCC clock, and can be used as a trigger clock to other peripherals.

Note:	In earlier versions of PIC24F devices, the function of the RTCC output pin was controlled by the RTSECSEL bit in the PADCFG1 register. If an application is being migrated to a newer PIC24F device, it will be necessary to verify how the alarm output is controlled, and modify the application as required.

Figure 56-6: Timer Pulse Generation



The RTCC pin is also capable of outputting the seconds clock or RTCC clock. The user can select between the alarm pulse generated by the RTCC module, the RTCC clock source or the seconds clock output. The RTCOUT (RTCPWC<9:8>) bits select between these outputs. When RTCOUT = 00, the alarm pulse is selected. When RTCOUT = 01, the seconds clock is selected. When RTCOUT = 01, the RTCC is selected.

56.5 POWER CONTROL

In addition to the basic RTCC functionality previously described, the RTCC includes a Power Control feature. By using the RTCC output pin, the microcontroller can periodically wake up an external device. Beyond that, however, the Power Control feature can also be programmed to monitor the external device for a wake-up event, and can even be programmed to wait for a programmable interval before monitoring. Finally, the Power Control feature can then shut down the external device. All of this is done autonomously by the RTCC, without the need to wake from a lower power mode (Sleep, Deep Sleep, etc.) and execute code.

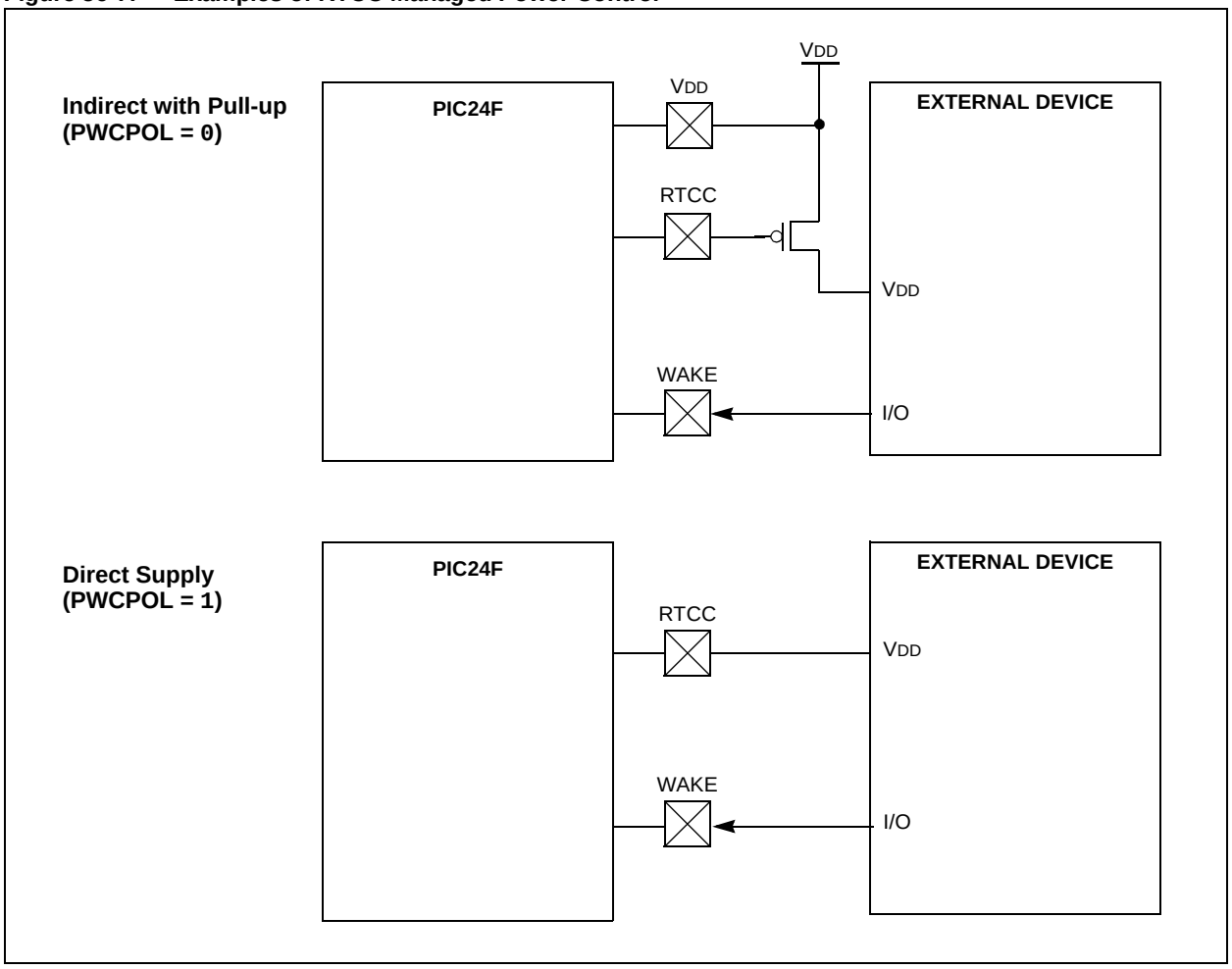
Two possible control circuits for this feature are shown in Figure 56-7. The WAKE pin in both examples represents an input that would wake up the device in the desired circumstances (e.g., INT0 in Deep Sleep, any enabled interrupt in Sleep, etc.).

The top figure illustrates a situation in which the external device requires more current than the I/O pin can reliably generate. Note that the Power Control Polarity is active-low in order to provide the external device power at the correct times.

A more straightforward approach is shown in the bottom figure. For external devices whose current consumption is within the range, an I/O pin can provide (approximately 20 mA), the device can be powered directly via the RTCC pin. If the device requires a stabilizing capacitor on VDD, this method could result in a significant current load. To use this layout, the capacitor would have to be very small (0.01 µF) or allowances for a greater time to reach operating stability may be required (see **Section 56.5.2 "Power Control Operation"** for more information).

To determine the best Power Control configuration for any given application, refer to the data sheets for both the Microchip device and the external device.

Figure 56-7: Examples of RTCC Managed Power Control



56.5.1 Initialization

To enable Power Control:

- The RTCC must be enabled (RPCFCAL<15> = 1)
- Power Control must be enabled (RTCPWC<15> = 1), and
- The RTCC pin must be enabled (RCFGCAL<10> = 1) and configured for Power Control (RTCPWC<9:8> = 11)

In addition, set the CHIME bit (ALCFGPRPT<15>) to enable the PWC periodicity.

The polarity of the PWC control signal may be chosen using the PWCPOL bit (RTCPWC<14>). Active-low or active-high may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the RTCC pad, in order to drive the GND pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches.

56.5.2 Power Control Operation

When the RTCC and PWC are enabled and running, the PWC logic generates a control output and a sample gate output. The control output is driven out on the RTCC pin (RCFGCAL<10> = 1 and RTCPWC<9:8> = 11) and is used to power up or down the external device.

Once the control output is asserted, the Stability Window begins. During this interval, the external device is given enough time to power up and provide a stable output. Once the output is (theoretically) stable, the Sample Window begins. In this interval, the RTCC monitors for the wake-up signal from the external device. Typically, a sample gate is used to mask out one or more wake-up signals from the external device.

Finally, both the Stability and Sample Windows close after the expiration of the Sample Window, and the external device is powered down.

56.5.2.1 STABILITY AND SAMPLE WINDOWS

The Stability and Sample Windows are controlled by the PWCSTAB and PWCSAMP bit fields in the RTCCSWT register (RTCCSWT<15:8> and <7:0>, respectively). This register is accessed through the ALRMVAL Value register when ALRMPTR<1:0> = 11.

As both the Stability and Sample Windows are defined in terms of the RTCC clock, their absolute values vary by the value of the PWC clock base period (TPWCCLK). The 8-bit magnitude of PWCSTAB and PWCSAMP allows for a window size of 0 to 255 TPWCCLK. The base period and the magnitudes of the window for each clock source are summarized in Table 56-5. Note that whenever the PWCCPRE or PWCSPRE bits are set, their corresponding window is doubled in size.

In addition, certain values for the PWCSTAB and PWCSAMP fields have specific control meanings in determining Power Control operations. If either bit field is 00h, the corresponding window is inactive. In addition, if the PWCSTAB field is FFh, the Stability Window remains active continuously, even if Power Control is disabled.

Table 56-5: Stability and Sample Window Size

Clock Source (RTCLK<1:0>)	Base Period (TPWCCLK, ms)	Stability Window		Sample Window	
		PWCCPRE = 0	PWCCPRE = 1	PWCSPRE = 0	PWCSPRE = 1
SOSC (00)	15.625	0 ms to ~3.98s	0 ms to ~7.97s	0 ms to ~3.98s	0 ms to ~7.97s
LPRC (01)	20	0 ms to 5.1s	0 ms to 10.2s	0 ms to 5.1s	0 ms to 10.2s
50 Hz Mains (10)	20	0 ms to 5.1s	0 ms to 10.2s	0 ms to 5.1s	0 ms to 10.2s
60 Hz Mains (11)	16.67	0 ms to 4.25s	0 ms to 8.5s	0 ms to 4.25s	0 ms to 8.5s

56.5.2.2 MODES OF OPERATION

56.5.2.2.1 Normal Operation (Stability and Sample Windows Active)

When PWCSTAB is not 0, and PWCSAMP is any value except 0 or 255, the PWC is configured for the normal mode of operation. In this mode, the external wake-up interrupt should be connected to the external device, controlled by the PWC power enable. Figure 56-8 shows operation with inverted (active-low) operation; Figure 56-9 shows normal (active-high) operation.

Figure 56-8: Power Control Timer (Normal Operation, PWCPOL = 0)

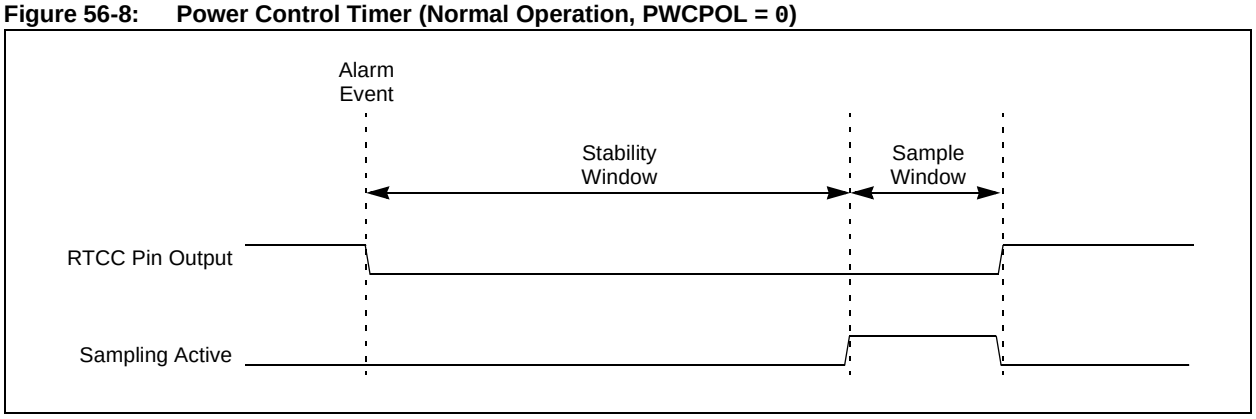
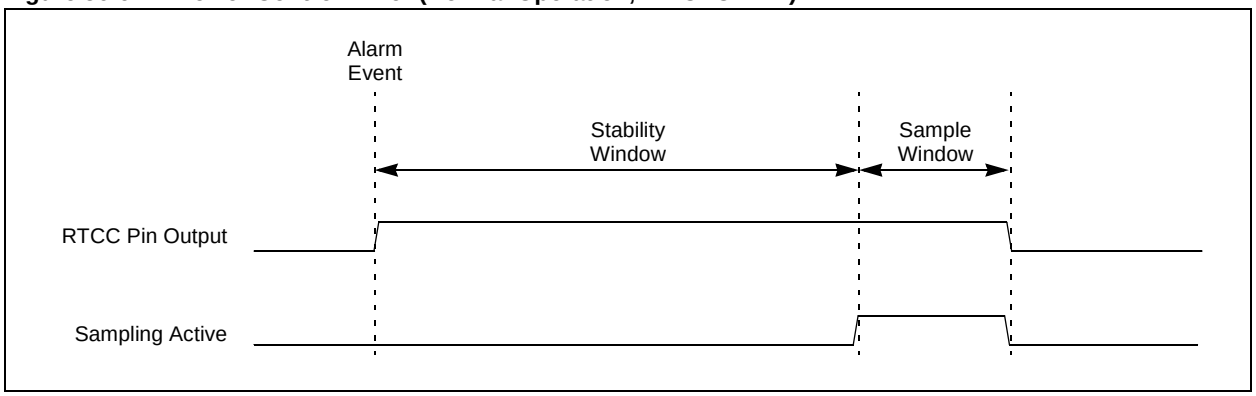


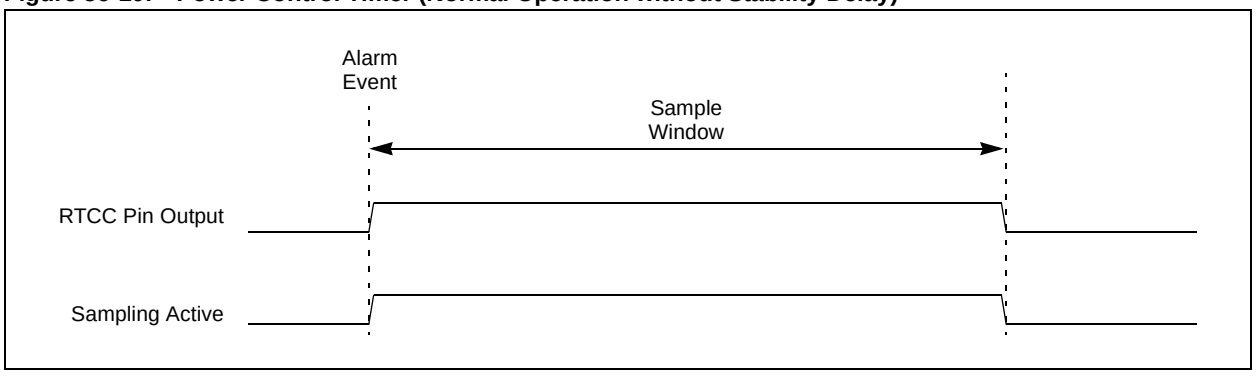
Figure 56-9: Power Control Timer (Normal Operation, PWCPOL = 1)



56.5.2.2.2 Normal Operation without Stability Delay (Stability Window Inactive)

When PWCSTAB is 0 and PWCSAMP is any value except 0 or 255, the PWC is configured for the normal mode of operation with no stability time, as shown in Figure 56-10. This mode is recommended when the external device, controlled by the PWC power enable, requires no time between when power is applied and when its wake-up or interrupt output is valid. Although a valid option, this case is considered to be unlikely.

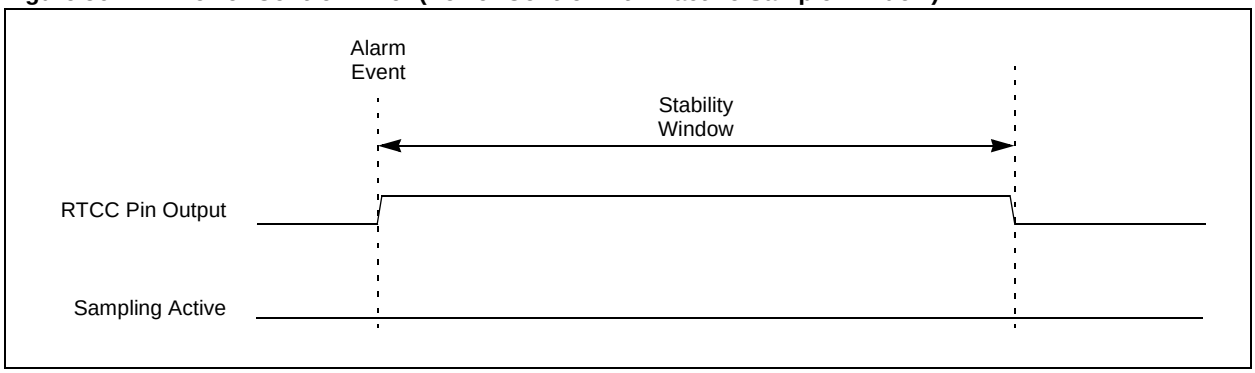
Figure 56-10: Power Control Timer (Normal Operation without Stability Delay)



56.5.2.2.3 Power Control without Sampling (Sample Window Inactive)

When PWCSTAB is any value but 0 and PWCSAMP is 0, the PWC is configured for Power Control only. No wake-up or interrupt sampling occurs, as shown in Figure 56-11. This mode is generally not used.

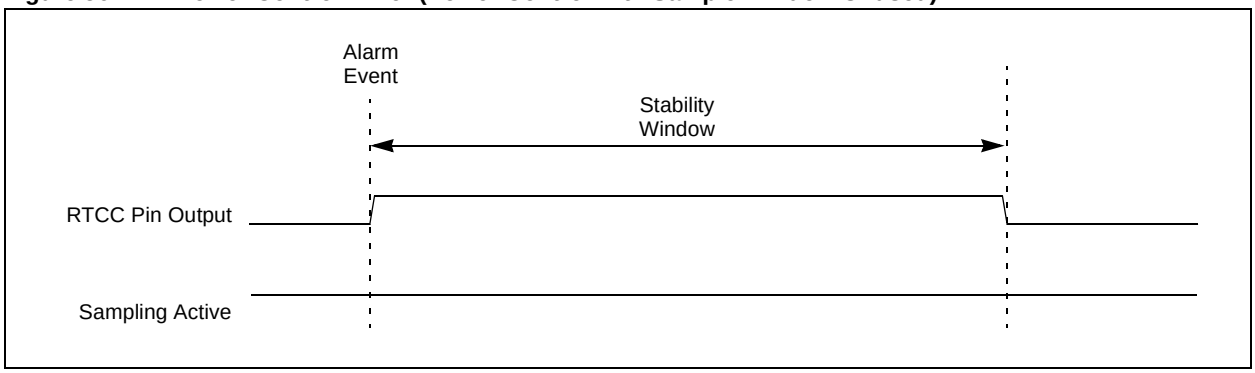
Figure 56-11: Power Control Timer (Power Control with Inactive Sample Window)



56.5.2.2.4 Power Control without Sampling (Sample Window Unused)

When PWCSTAB is any value but 0 and PWCSAMP is 255, the PWC is configured for Power Control only. The Sample Window, although always active, is not used. This is shown in Figure 56-12. This mode should be used when the external device, controlled by the PWC power enable, does not drive a wake-up or interrupt input directly. In this case, the sampling of external interrupts is disabled and the external interrupt may be driven by any source.

Figure 56-12: Power Control Timer (Power Control with Sample Window Unused)



56.5.2.2.5 PWC Disabled

When PWCEN is cleared (RTCPWC<15> = 0), the PWCSTAB and PWCSAMP fields have no effect. In this case, the sampling of external interrupts is disabled; the external interrupt may be driven by any source.

56.6 RESETS

56.6.1 Device Reset

When a device Reset occurs, the ALCFGRPT register is forced to its Reset state, causing the alarm to be disabled (if enabled prior to the Reset). If the RTCC was enabled, it will continue to operate when a basic device Reset occurs.

56.6.2 Power-on Reset (POR)

The RCFGCAL and RTCPWC registers are only reset on a POR. Once the device exits the POR state, the clock registers should be reloaded with the desired values.

The timer prescaler values can only be reset by writing to the SECONDS register. No device Reset can affect the prescalers.

56.7 OPERATION IN POWER-SAVING MODES

56.7.1 Sleep Modes

The timer and alarm continue to operate, while in both Sleep and Deep Sleep modes, if the module remains enabled. The operation of the alarm is not affected by Sleep, as an alarm event can always wake-up the CPU.

Idle mode does not affect the operation of the timer or alarm.

56.7.2 VBAT Mode

In PIC24F devices that include VBAT power-saving features, the RTCC is capable of continued operation during this mode. While the alarm still functions, it will not wake the device.

The RTCBAT Configuration bit controls this feature. By default (RTCBAT = 1), continued RTCC operation in VBAT mode is enabled.

While in VBAT mode, the RTCC clock source selected by the RTCLK<1:0> bits remains active. Users should remember to include the incremental current consumption required for the clock source when calculating a power budget for VBAT operation.

56.8 PERIPHERAL MODULE DISABLE (PMD) REGISTER

The Peripheral Module Disable (PMD) registers provide a method to disable the RTCC module by stopping all clock sources supplied to that module. When a peripheral is disabled via the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect and read values will be invalid. A peripheral module will only be enabled if the RTCCMD bit in the the PMDx register is cleared.

56.9 REGISTER MAPS

A summary of the registers associated with the PIC24F RTCC with External Power Control module is provided in Table 56-6.

Table 56-6: Real-Time Clock and Calendar Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	Alarm Value Register Window based on APTR<1:0>																xxxx
ALCFGRPT	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	0000
RTCVAL	RTCC Value Register Window based on RTCPTR<1:0>																xxxx
RCFGCAL(1)	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR1	RTCPTR0	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	0000
RTCPWC	PWCEN	PWCPOL	PWCCPRE	PWCSPRE	RTCLK1	RTCLK0	RTCOUT1	RTCOUT0	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: RCFGCAL register Reset value dependent on type of Reset.

56.10 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Real-Time Clock and Calendar (RTCC) module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

56.11 REVISION HISTORY

Revision A (May 2011)

This is the initial released revision of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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