Section 55. Data Signal Modulator (DSM)

HIGHLIGHTS

This section of the manual contains the following major topics:

55.1 INTRODUCTION

The Data Signal Modulator (DSM) is a peripheral which allows the user to mix a data stream (the “Modulator signal”) with a carrier signal to produce a modulated output.

Both the carrier and the Modulator signals are supplied to the DSM module, either internally from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical “AND” operation of both the carrier and Modulator signals and then it is provided to the MDOUT pin.

The carrier signal is comprised of two distinct and separate signals: a Carrier High (CARH) signal and a Carrier Low (CARL) signal. During the time in which the Modulator (MOD) signal is in a logic high state, the DSM mixes the Carrier High signal with the Modulator signal. When the Modulator signal is in a logic low state, the DSM mixes the Carrier Low signal with the Modulator signal.

Using this method, the DSM can generate the following types of key modulation schemes:

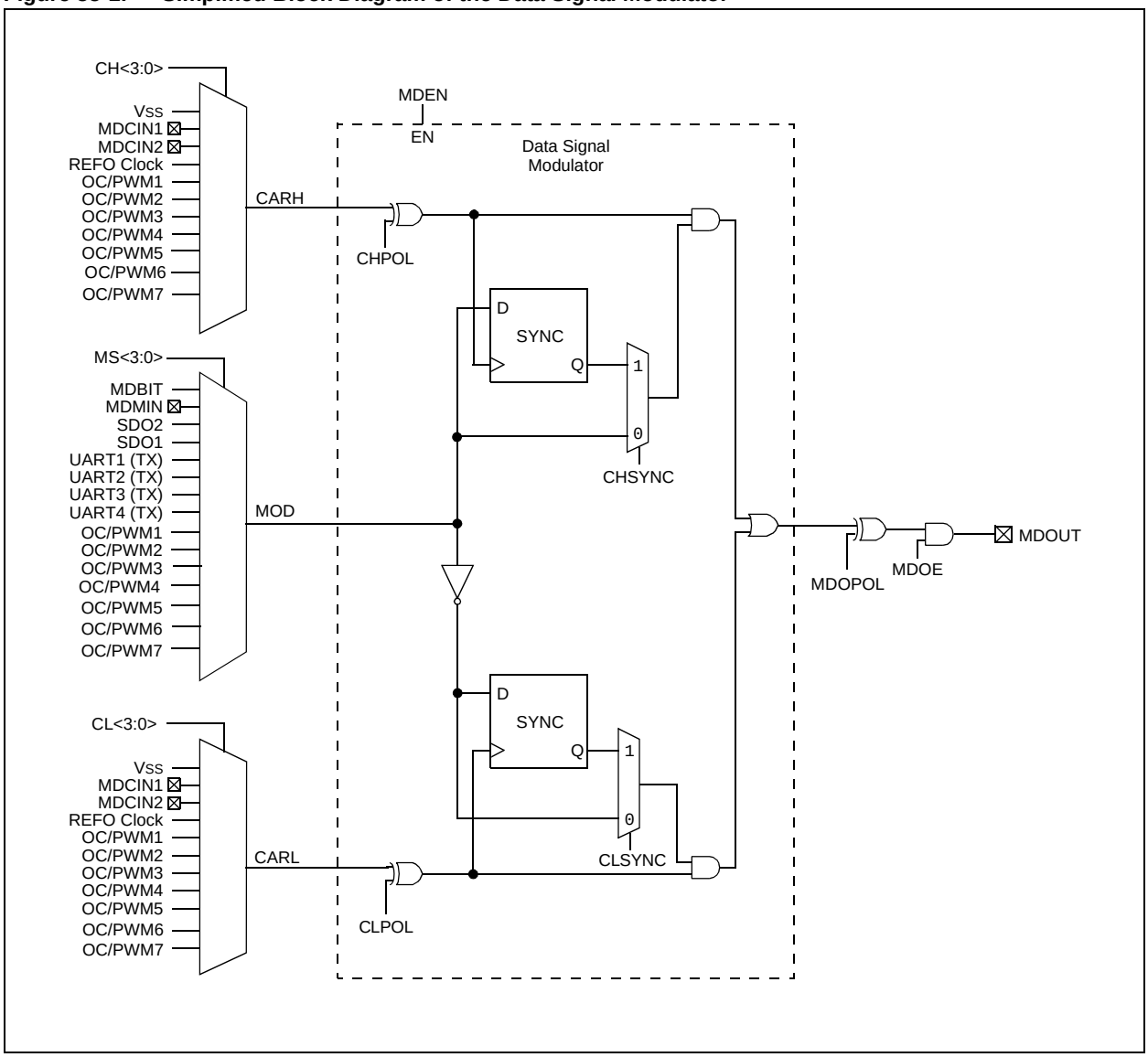
- Frequency Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Additionally, the following features are provided within the DSM module:

- Carrier Synchronization
- Carrier Source Polarity Select
- Carrier Source Pin Disable
- Programmable Modulator Data
- Modulator Source Pin Disable
- Modulated Output Polarity Select
- Slew Rate Control

Figure 55-1 shows a simplified block diagram of the Data Signal Modulator peripheral.

Figure 55-1: Simplified Block Diagram of the Data Signal Modulator



55.2 DSM OPERATION

The DSM module can be enabled by setting the MDEN bit in the MDCON register. Clearing the MDEN bit in the MDCON register disables the DSM module by automatically switching the Carrier High and Carrier Low signals to the VSS signal source. The Modulator signal source is also switched to the MDBIT in the MDCON register. This not only assures that the DSM module is inactive, but that it is also consuming the least amount of current.

The values used to select the Carrier High, Carrier Low and Modulator sources, held by the Modulation Source, Modulation High Carrier and Modulation Low Carrier Control registers, are not affected when the MDEN bit is cleared, and the DSM module is disabled. The values inside these registers remain unchanged while the DSM is inactive. The sources for the Carrier High, Carrier Low and Modulator signals will once again be selected when the MDEN bit is set and the DSM module is again enabled and active.

The modulated output signal can be disabled without shutting down the DSM module. The DSM module will remain active and continue to mix signals, but the output value will not be sent to the MDOUT pin. During the time that the output is disabled, the MDOUT pin will remain low. The modulated output can be disabled by clearing the MDOE bit in the MDCON register.

55.3 MODULATOR SIGNAL SOURCES

The Modulator signal can be supplied from the following sources:

- OC/PWM<1:7>
- SDO1 and SDO2
- UART<1:4> TX Signal
- External Signal on MDMIN Pin
- MDBIT bit in the MDCON Register

The Modulator signal is selected by configuring the MS<3:0> bits in the MDSRC register.

55.4 CARRIER SIGNAL SOURCES

The Carrier High signal and Carrier Low signal can be supplied from the following sources:

- OC/PWM<1:7>
- Reference Clock Module Signal (REFO)
- External Signal on MDCIN1 Pin (MDCIN1) and MDCIN2 Pin (MDCIN2)
- VSS

The Carrier High signal is selected by configuring the CH<3:0> bits in the MDCAR register. The Carrier Low signal is selected by configuring the CL<3:0> bits in the MDCAR register.

55.5 CARRIER SYNCHRONIZATION

During the time when the DSM switches between Carrier High and Carrier Low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the Modulator signal. When synchronization is enabled, the carrier pulse that is being mixed at the time of the transition is allowed to transition low before the DSM switches over to the next carrier source.

Synchronization is enabled separately for the Carrier High and Carrier Low signal sources. Synchronization for the Carrier High signal can be enabled by setting the CHSYNC bit and the synchronization for the Carrier Low signal can be enabled by setting the CLSYNC bit in the MDCAR register.

Figure 55-2 through Figure 55-6 show timing diagrams of using various synchronization methods.

Figure 55-2: On-Off Keying (OOK) Synchronization

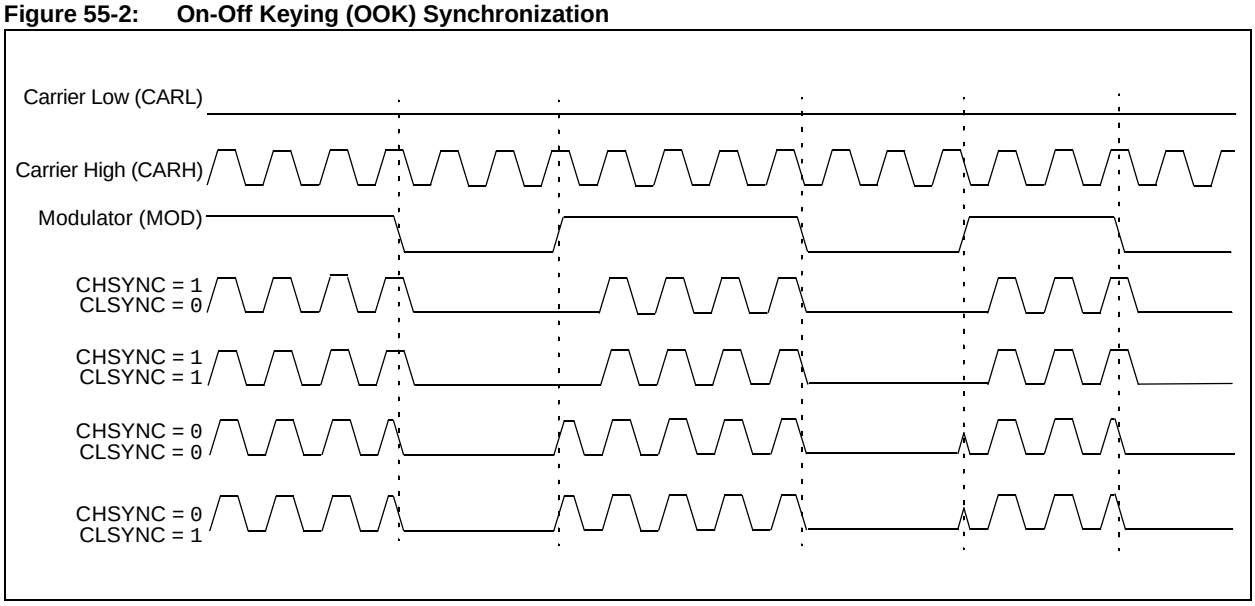


Figure 55-3: No Synchronization (CHSYNC = 0, CLSYNC = 0)

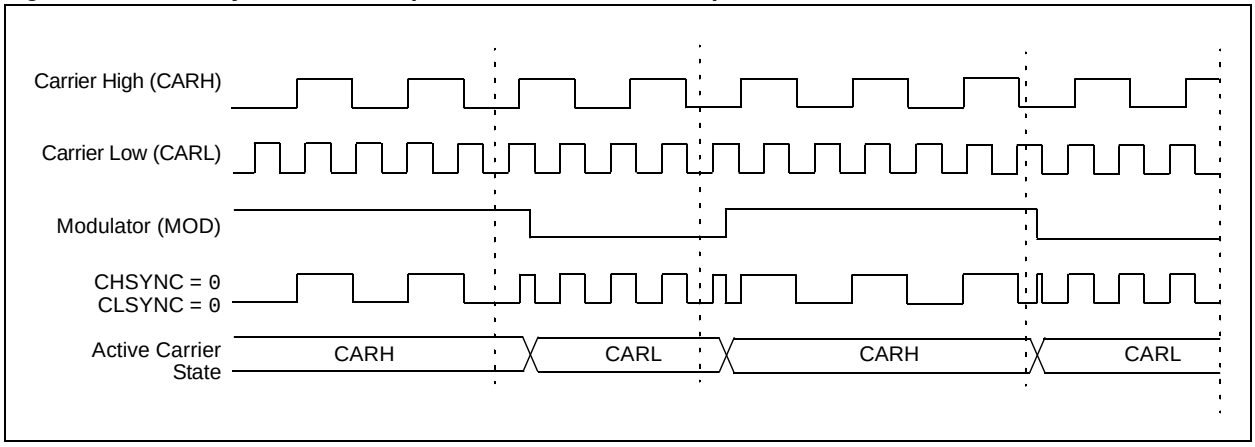


Figure 55-4: Carrier High Synchronization (CHSYNC = 1, CLSYNC = 0)

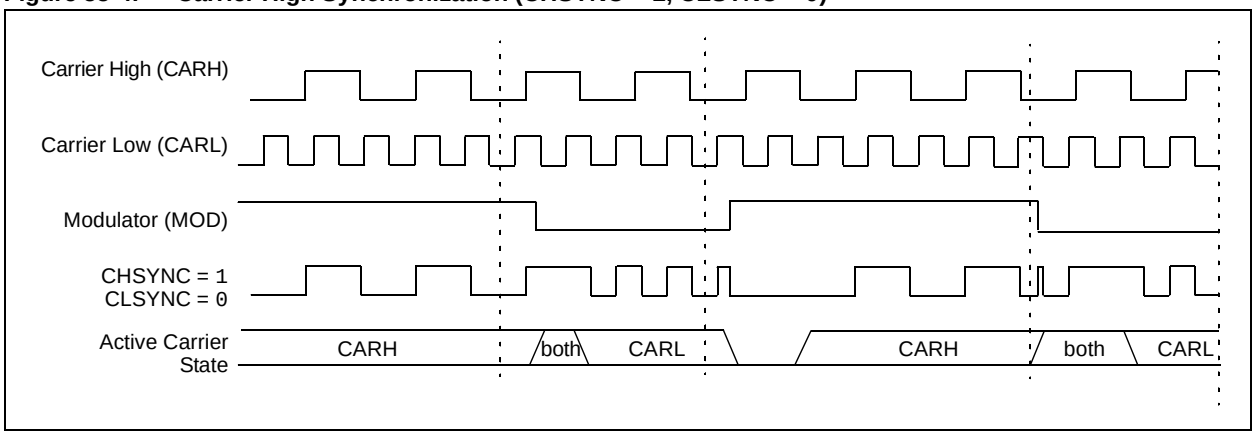


Figure 55-5: Carrier Low Synchronization (CHSYNC = 0, CLSYNC = 1)

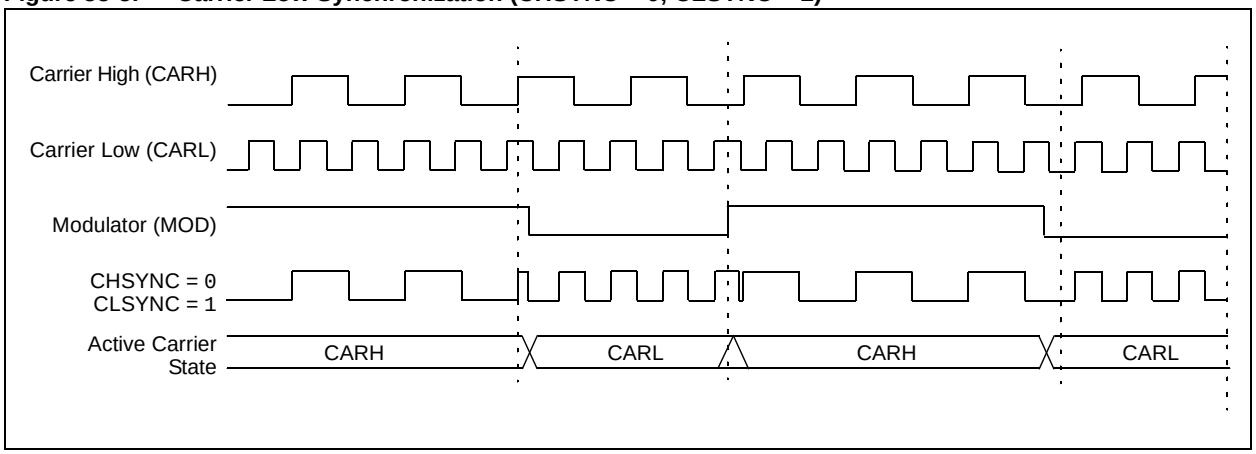
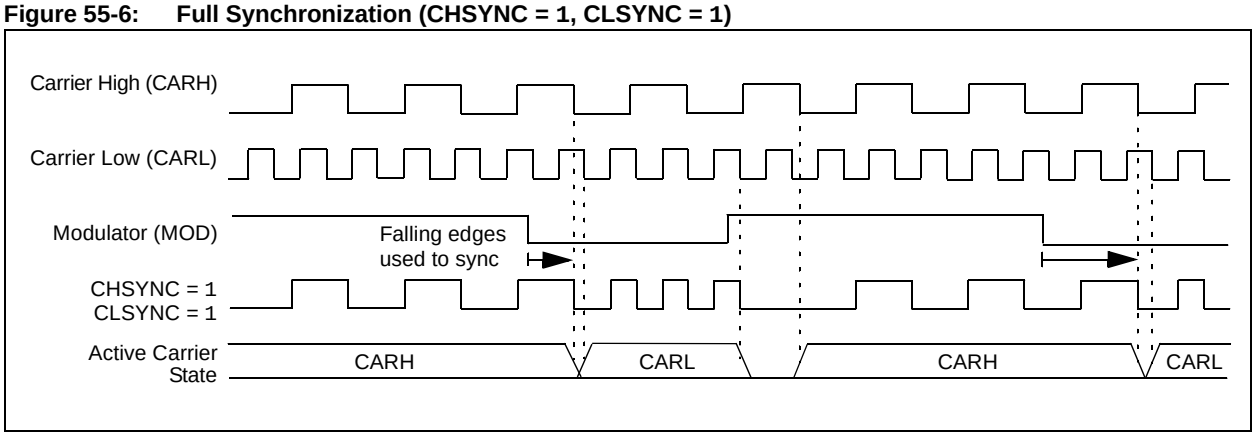


Figure 55-6: Full Synchronization (CHSYNC = 1, CLSYNC = 1)



55.6 CARRIER SOURCE POLARITY SELECT

The signal provided from any selected input source for the Carrier High and Carrier Low signals can be inverted. Inverting the signal for the Carrier High source is enabled by setting the CHPOL bit of the MDCAR register. Inverting the signal for the Carrier Low source is enabled by setting the CLPOL bit of the MDCAR register.

55.7 CARRIER SOURCE PIN DISABLE

Some peripherals assert control over their corresponding output pin when they are enabled. For example, when the OC/PWM module is enabled, the output of OC/PWM is connected to the OC/PWM pin.

This default connection to a pin can be disabled by setting the CHODIS bit in the MDCAR register for the Carrier High source, and the CLODIS bit in the MDCAR register for the Carrier Low source.

55.8 PROGRAMMABLE MODULATOR DATA

The MDBIT of the MDCON register can be selected as the source for the Modulator signal. This gives the user the ability to program the value used for modulation.

55.9 MODULATOR SOURCE PIN DISABLE

The Modulator source default connection to a pin can be disabled by setting the SODIS bit in the MDSRC register.

55.10 MODULATED OUTPUT POLARITY

The modulated output signal, provided on the MDOUT pin, can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON register.

55.11 SLEW RATE CONTROL

When modulated data streams of 20 MHz or greater are required, the slew rate limitation on the output port pin can be disabled. The slew rate limitation can be removed by clearing the MDSLR bit in the MDCON register.

55.12 OPERATION IN SLEEP MODE

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep if the Carrier and Modulator input sources are also still operable during Sleep.

55.13 EFFECTS OF A RESET

Upon any device Reset, the Data Signal Modulator module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

Register 55-1: MDCON: MODULATION CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
MDEN	MDFRZ	MSIDL	—	—	—	—	—
bit15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R-0	U-0	U-0	R/W-0
—	MDOE	MDSLR	MDOPOL	MDOUT	—	—	MDBIT(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **MDEN:** Modulator Module Enable bit
1 = Modulator module is enabled and mixing input signals
0 = Modulator module is disabled and has no output

bit 14 **MDFRZ:** MOD Freeze in Debug Mode bit
1 = When the emulator is in Debug mode, the module freezes operation
0 = When the emulator is in Debug mode, the module continues operation

bit 13 **MSIDL:** Modulator Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **MDOE:** Modulator Module Pin Output Enable bit
1 = Modulator pin output is enabled
0 = Modulator pin output is disabled

bit 5 **MDSLR:** MDOUT Pin Slew Rate Limiting bit
1 = MDOUT pin slew rate limiting is enabled
0 = MDOUT pin slew rate limiting is disabled

bit 4 **MDOPOL:** Modulator Output Polarity Select bit
1 = Modulator output signal is inverted
0 = Modulator output signal is not inverted

bit 3 **MDOUT:** Modulator Output bit
Displays the current output value of the Modulator module.(1)

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **MDBIT:** Manual Modulation Input bit(2)
1 = Carrier is modulated
0 = Carrier is not modulated

Note 1: The modulated output frequency can be greater and asynchronous from the clock that updates this register bit. The bit value may not be valid for higher speed Modulator or carrier signals.

2: The MDBIT must be selected as the modulation source (MDSRC<3:0> = 0000).

Register 55-2: MDSRC: Modulation Source Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit15							bit 8

R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
SODIS(1)	—	—	—	MS3(2)	MS2(2)	MS1(2)	MS0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **SODIS:** Modulation Source Output Disable bit(1)
1 = Output signal driving the peripheral output pin (selected by MS<3:0>) is disabled
0 = Output signal driving the peripheral output pin (selected by MS<3:0>) is enabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3-0 **MS<3:0>** Modulation Source Selection bits(2)
1111 = Unimplemented
1110 = Output Compare/PWM Module 7 output
1101 = Output Compare/PWM Module 6 output
1100 = Output Compare/PWM Module 5 output
1011 = Output Compare/PWM Module 4 output
1010 = Output Compare/PWM Module 3 output
1001 = Output Compare/PWM Module 2 output
1000 = Output Compare/PWM Module 1 output
0111 = UART4 TX output
0110 = UART3 TX output
0101 = UART2 TX output
0100 = UART1 TX output
0011 = SPI2 module output (SDO2)
0010 = SPI1 module output (SDO1)
0001 = Input on MDMIN pin
0000 = Manual modulation using MDBIT (MDCON<0>)

Note 1: This bit is only affected by a POR.
2: These bits are not affected by a POR.

Register 55-3: MDCAR: Modulation Carrier Control Register

R/W-x	R/W-x	R/W-x	U-0	R/W-x	R/W-x	R/W-x	R/W-x
CHODIS	CHPOL	CHSYNC	—	CH3(1)	CH2(1)	CH1(1)	CH0(1)
bit 15							bit 8

R/W-0	R/W-x	R/W-x	U-0	R/W-x	R/W-x	R/W-x	R/W-x
CLODIS	CLPOL	CLSYNC	—	CL3(1)	CL2(1)	CL1(1)	CL0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CHODIS:** Modulator High Carrier Output Disable bit
1 = Output signal driving the peripheral output pin (selected by CH<3:0>) is disabled
0 = Output signal driving the peripheral output pin (selected by CH<3:0>) is enabled

bit 14 **CHPOL:** Modulator High Carrier Polarity Select bit
1 = Selected high carrier signal is inverted
0 = Selected high carrier signal is not inverted

bit 13 **CHSYNC:** Modulator High Carrier Synchronization Enable bit
1 = Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
0 = Modulator output is not synchronized to the high time carrier signal(1)

bit 12 **Unimplemented:** Read as '0'

bit 11-8 **CH<3:0>** Modulator Data High Carrier Selection bits(1)
11xx = Reserved
1011 = Reserved
1010 = Output Compare/PWM Module 7 output
1001 = Output Compare/PWM Module 6 output
1000 = Output Compare/PWM Module 5 output
0111 = Output Compare/PWM Module 4 output
0110 = Output Compare/PWM Module 3 output
0101 = Output Compare/PWM Module 2 output
0100 = Output Compare/PWM Module 1 output
0011 = Reference clock (REFO) output
0010 = Input on MDCIN2 pin
0001 = Input on MDCIN1 pin
0000 = Vss

bit 7 **CLODIS:** Modulator Low Carrier Output Disable bit
1 = Output signal driving the peripheral output pin (selected by CL<3:0>) is disabled
0 = Output signal driving the peripheral output pin (selected by CL<3:0>) is enabled

bit 6 **CLPOL:** Modulator Low Carrier Polarity Select bit
1 = Selected low carrier signal is inverted
0 = Selected low carrier signal is not inverted

bit 5 **CLSYNC:** Modulator Low Carrier Synchronization Enable bit
1 = Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier
0 = Modulator output is not synchronized to the low time carrier signal(1)

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **CL<3:0>** Modulator Data High Carrier Selection bits(1)
Bit settings are identical to those for CH<3:0>.

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

Example 55-1: Data Signal Modulation with Software Controlled Bit

```
#include "p24Fxxxx.h"
main()
{
       MDCAR=0x00;
       MDCON =0x00;
       MDSRC=0x00;
       MDCONbits.MDEN=1;      //enable the data signal modulator module
       MDSRCbits.MDSRC=1;     //selecting modulating source as the MDBIT
                              //allows software to manually control the modulation
       MDCARbit.CH=3;         //select the carrier high signal as reference clock
       MDCARbits.CL=0;        //select the carrier low signal as Vss
       MDCONbits.MDOE=1;      //enable the output of the modulator
       while(1)               //infinite loop where the carrier signal is modulated
                              //with the manual software control of the MDBIT
{
              for(i=0;i<30;i++)
                             Nop();
              MDCONbits.MDBIT=1;
                             Nop();
              for(i=0;i<30;i++)
                             Nop();
              MDCONbits.MDBIT=0;
                             Nop();
}
}
```

55.14 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the DSM module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

55.15 REVISION HISTORY

Revision A (May 2011)

This is the initial released revision of this document.

NOTES:

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