

Section 52. Liquid Crystal Display (LCD)

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52.1 INTRODUCTION

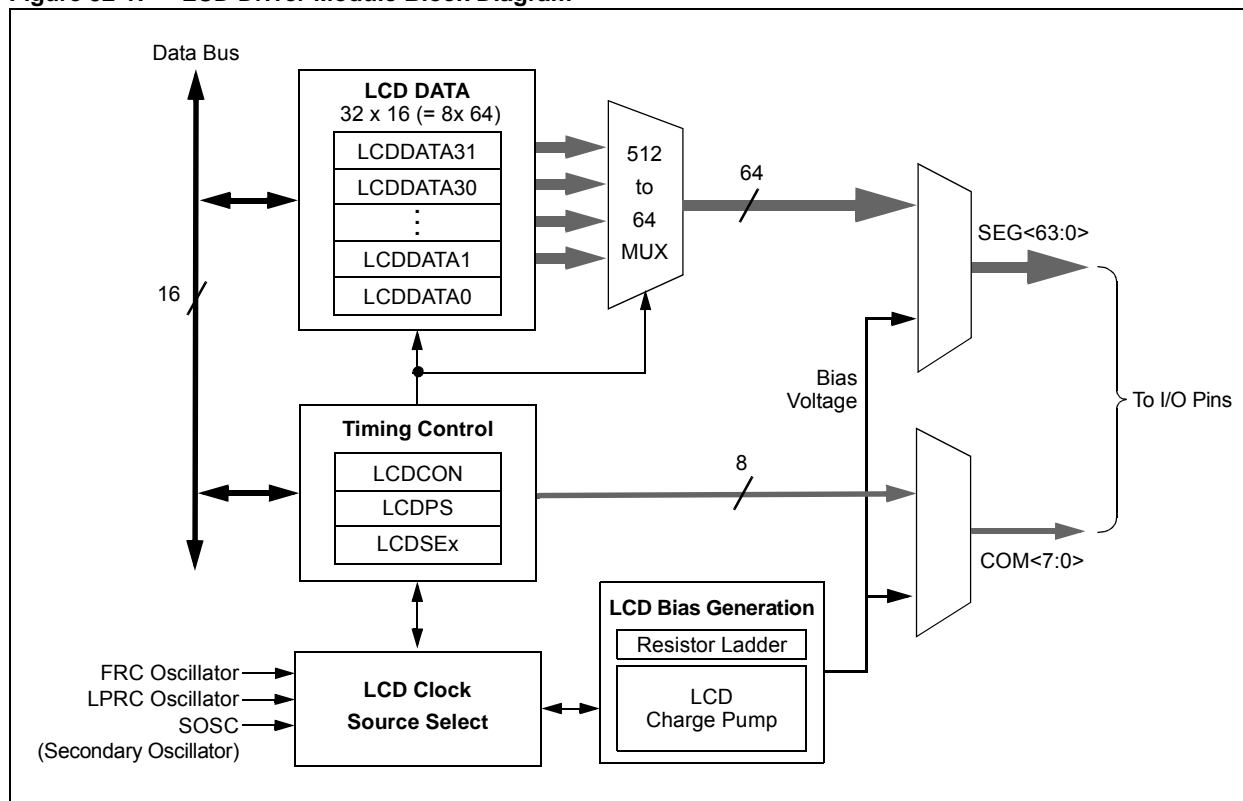
The Liquid Crystal Display (LCD) driver module generates the timing control to drive a static or multiplexed LCD panel. In the 100-pin devices (PIC24FJXXXGA3XX), the module drives panels of up to eight commons and up to 60 segments when 5 to 8 commons are used, and up to 64 segments when 1 to 4 commons are used. It also provides control of the LCD pixel data.

The LCD driver module supports:

- Direct driving of LCD panel
- Three LCD clock sources with selectable prescaler
- Up to eight commons:
 - Static (one common)
 - 1/2 Multiplex (two commons)
 - 1/3 Multiplex (three commons)
 - 1/8 Multiplex (eight commons)
- Up to 60 segments (in 100-pin devices when 1/5-1/8 Multiplex is selected), 64 (in 100-pin devices when up to 1/4 Multiplex is selected), 46 (in 80-pin devices when 1/5-1/8 Multiplex is selected), 50 (in 80-pin devices when up to 1/4 Multiplex is selected), 30 (in 64-pin devices when 1/5-1/8 Multiplex is selected) and 34 (in 64-pin devices when up to 1/4 Multiplex is selected)
- Static, 1/2 or 1/3 LCD Bias
- On-chip Bias generator with dedicated charge pump to support a range of fixed and variable Bias options
- Internal resistors for Bias voltage generation
- Software contrast control for LCD using the internal biasing

A simplified block diagram of the module is shown in Figure 52-1.

Figure 52-1: LCD Driver Module Block Diagram



52.2 LCD REGISTERS

The LCD driver module has 40 registers:

- LCD Control Register (LCDCON)
- LCD Phase Register (LCDPS)
- LCD Voltage Regulator Control Register (LCDREG)
- LCD Reference Ladder Control Register (LCDREF)
- Four LCD Segment Enable Registers (LCDSE3:LCDSE0)
- 32 LCD Data Registers (LCDDATA31:LCDDATA0)

The LCDCON register, shown in Register 52-1, controls the overall operation of the module. Once the module is configured, the LCDEN (LCDCON<15>) bit is used to enable or disable the LCD module. The LCD panel can also operate during Sleep by clearing the SLPEN (LCDCON<6>) bit.

The LCDPS register, shown in Register 52-2, configures the LCD clock source prescaler and the type of waveform: Type-A or Type-B. For details on these features, see **Section 52.4 “LCD Clock Source Selection”**, **Section Table 52-6: “Special Function Registers Associated with LCD Driver Module”** and **Section 52.10 “LCD Waveform Generation”**.

Register 52-1: LCDCON: LCD Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
LCDEN	—	LCDSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SLPEN	WERR	CS1	CS0	LMUX2	LMUX1	LMUX0
bit 7							bit 0

Legend:	C = Clearable bit
R = Readable bit	W = Writable bit
-n = Value at POR	‘1’ = Bit is set
	U = Unimplemented bit, read as ‘0’
	‘0’ = Bit is cleared
	x = Bit is unknown

- bit 15 **LCDEN:** LCD Driver Enable bit
1 = LCD driver module is enabled
0 = LCD driver module is disabled
- bit 14 **Unimplemented:** Read as ‘0’
- bit 13 **LCDSIDL:** Stop LCD Drive in CPU Idle mode control bit
1 = LCD driver halts in CPU Idle mode
0 = LCD driver continues to operate in CPU Idle mode
- bit 12-7 **Unimplemented:** Read as ‘0’
- bit 6 **SLPEN:** LCD Driver Enable in Sleep Mode bit
1 = LCD driver module is disabled in Sleep mode
0 = LCD driver module is enabled in Sleep mode
- bit 5 **WERR:** LCD Write Failed Error bit
1 = LCDDATAx register is written while WA (LCDPS<4>) = 0 (must be cleared in software)
0 = No LCD write error
- bit 4-3 **CS<1:0>:** Clock Source Select bits
00 = FRC (8 MHz)/8192
01 = SOSC oscillator (32.768 kHz)/32
1x = INTRC (31.25 kHz)/32

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Register 52-1: LCDCON: LCD Control Register (Continued)

bit 2-0 **LMUX<2:0>**: Commons Select bits

LMUX<2:0>	Multiplex	Bias
111	1/8 MUX (COM<7:0>)	1/3
110	1/7 MUX (COM<6:0>)	1/3
101	1/6 MUX (COM<5:0>)	1/3
100	1/5 MUX (COM<4:0>)	1/3
011	1/4 MUX (COM<3:0>)	1/3
010	1/3 MUX (COM<2:0>)	1/2 or 1/3
001	1/2 MUX (COM<1:0>)	1/2 or 1/3
000	Static (COM0)	Static

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Register 52-2: LCDPS: LCD Phase Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R-0	R-0	r-0	R/W-0	R/W-0	R/W-0
WFT	BIASMD	LCDA	WA	Reserved	LP2	LP1	LP0
bit 7							bit 0

Legend: r = Reserved bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **WFT:** Waveform Type Select bit
1 = Type-B waveform (phase changes on each frame boundary)
0 = Type-A waveform (phase changes within each common type)
- bit 6 **BIASMD:** Bias Mode Select bit
When LMUX<2:0> = 000 or 011-111:
0 = Static Bias mode/1/3 Bias mode (do not set this bit to '1')
When LMUX<2:0> = 001 or 010:
1 = 1/2 Bias mode
0 = 1/3 Bias mode
- bit 5 **LCDA:** LCD Active Status bit
1 = LCD driver module is active
0 = LCD driver module is inactive
- bit 4 **WA:** LCD Write Allow Status bit
1 = Write into the LCDDATAx registers is allowed
0 = Write into the LCDDATAx registers is not allowed
- bit 3 **Reserved:** Maintain as '0'
- bit 2-0 **LP<2:0>:** LCD Prescaler Select bits

LP<2:0>	Prescaler	Frame Frequency							
		Static	1/2 MUX	1/3 MUX	1/4 MUX	1/5 MUX	1/6 MUX	1/7 MUX	1/8 MUX
111	1:8	31	31	42	31	25	21	18	16
110	1:7	36	36	48	36	29	24	20	18
101	1:6	42	42	56	42	33	28	24	21
100	1:5	50	50	67	50	40	33	29	25
011	1:4	62	62	83	62	50	42	36	31
010	1:3	83	83	111	83	67	56	48	42
001	1:2	125	125	167	125	100	83	71	62
000	1:1	250	250	333	250	200	167	143	125

52.3 LCD SEGMENT PINS CONFIGURATION

The LCDSEx registers configure the functions of the port pins. Setting the segment enable bit for a particular segment configures that pin as an LCD driver. There are four LCD Segment Enable registers, as shown in Table 52-1. The prototype LCDSEx register is shown in Register 52-3.

Table 52-1: LCDSE Registers and Associated Segments

Register	Segments
LCDSE0	Seg 15:Seg 0
LCDSE1	Seg 31:Seg 16
LCDSE2	Seg 47:Seg 32
LCDSE3	Seg 63:Seg 48

Once the module is initialized for the LCD panel, the individual bits of the LCDDATAx registers are cleared or set to represent a clear or dark pixel, respectively.

Specific sets of LCDDATA registers are used with specific segments and common signals. Each bit represents a unique combination of a specific segment connected to a specific common.

Individual LCDDATA bits are named by the convention, “SxxCy”, with “xx” as the segment number and “y” as the common number. The relationship is summarized in Register 52-2. The prototype LCDDATAx register is shown in Register 52-4.

Note: Not all LCDSEx and LCDDATAx registers are implemented in the devices. Refer to the specific device data sheet for more details.

Register 52-3: LCDSEx: LCD SEGMENTx Enable Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n+15)	SE(n+14)	SE(n+13)	SE(n+12)	SE(n+11)	SE(n+10)	SE(n+9)	SE(n+8)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n+7)	SE(n+6)	SE(n+5)	SE(n+4)	SE(n+3)	SE(n+2)	SE(n+1)	SE(n)
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

‘0’ = Bit is cleared

x = Bit is unknown

bit 7-0

SE(n + 15):SE(n): Segment Enable bits

For LCDSE0: n = 0

For LCDSE1: n = 16

For LCDSE2: n = 32

For LCDSE3: n = 48

1 = Segment function of the pin is enabled; digital I/O is disabled

0 = Segment function of the pin is disabled

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Register 52-4: LCDDATAx: LCD DATAx Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+15)Cy	S(n+14)Cy	S(n+13)Cy	S(n+12)Cy	S(n+11)Cy	S(n+10)Cy	S(n+9)Cy	S(n+8)Cy
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
S(n+7)Cy	S(n+6)Cy	S(n+5)Cy	S(n+4)Cy	S(n+3)Cy	S(n+2)Cy	S(n+1)Cy	S(n)Cy
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0

S(n + 15)Cy:S(n)Cy: Pixel On bits

For registers, LCDDATA0 through LCDDATA3: n = (16x), y = 0

For registers, LCDDATA4 through LCDDATA7: n = (16(x - 4)), y = 1

For registers, LCDDATA8 through LCDDATA11: n = (16(x - 8)), y = 2

For registers, LCDDATA12 through LCDDATA15: n = (16(x - 12)), y = 3

For registers, LCDDATA16 through LCDDATA19: n = (16(x - 16)), y = 4

For registers, LCDDATA20 through LCDDATA23: n = (16(x - 20)), y = 5

For registers, LCDDATA24 through LCDDATA27: n = (16(x - 24)), y = 6

For registers, LCDDATA28 through LCDDATA31: n = (16(x - 28)), y = 7

1 = Pixel on

0 = Pixel off

Table 52-2: LCDDATA Registers and Bits for Segment and COM Combinations

COM Lines	Segments			
	0 to 15	16 to 31	32 to 47	48 to 64
0	LCDDATA0 S00C0:S15C0	LCDDATA1 S16C0:S31C0	LCDDATA2 S32C0:S47C0	LCDDATA3 S48C0:S63C0
1	LCDDATA4 S00C1:S15C1	LCDDATA5 S16C1:S31C1	LCDDATA6 S32C1:S47C1	LCDDATA7 S48C1:S63C1
2	LCDDATA8 S00C2:S15C2	LCDDATA9 S16C2:S31C2	LCDDATA10 S32C2:S47C2	LCDDATA11 S48C2:S63C2
3	LCDDATA12 S00C3:S15C3	LCDDATA13 S16C3:S31C3	LCDDATA14 S32C3:S47C3	LCDDATA15 S48C3:S63C3
4	LCDDATA16 S00C4:S15C4	LCDDATA17 S16C4:S31C4	LCDDATA18 S32C4:S47C4	LCDDATA19 S48C4:S59C4
5	LCDDATA20 S00C5:S15C5	LCDDATA21 S16C5:S31C5	LCDDATA22 S32C5:S47C5	LCDDATA23 S48C5:S69C5
6	LCDDATA24 S00C6:S15C6	LCDDATA25 S16C6:S31C6	LCDDATA26 S32C6:S47C6	LCDDATA27 S48C6:S59C6
7	LCDDATA28 S00C7:S15C7	LCDDATA29 S16C7:S31C7	LCDDATA30 S32C7:S47C7	LCDDATA31 S48C7:S59C7

52.4 LCD CLOCK SOURCE SELECTION

The LCD driver module has three possible clock sources:

- FRC/8192
- SOSC Clock/32
- LPRC/32

The first clock source is the 8 MHz Fast Internal RC (FRC) oscillator divided by 8,192. This divider ratio is chosen to provide about 1 kHz output. The divider is not programmable. Instead, the LCD prescaler bits, LCDPS<3:0>, are used to set the LCD frame clock rate.

The second clock source is the SOSC oscillator/32. This also outputs about 1 kHz when a 32.768 kHz crystal is used with the SOSC oscillator. To use the SOSC oscillator as a clock source, set the SOSCEN OSCCON<1> bit.

The third clock source is a 31.25 kHz internal LPRC oscillator/32 that provides approximately 1 kHz output.

The second and third clock sources may be used to continue running the LCD while the processor is in Sleep.

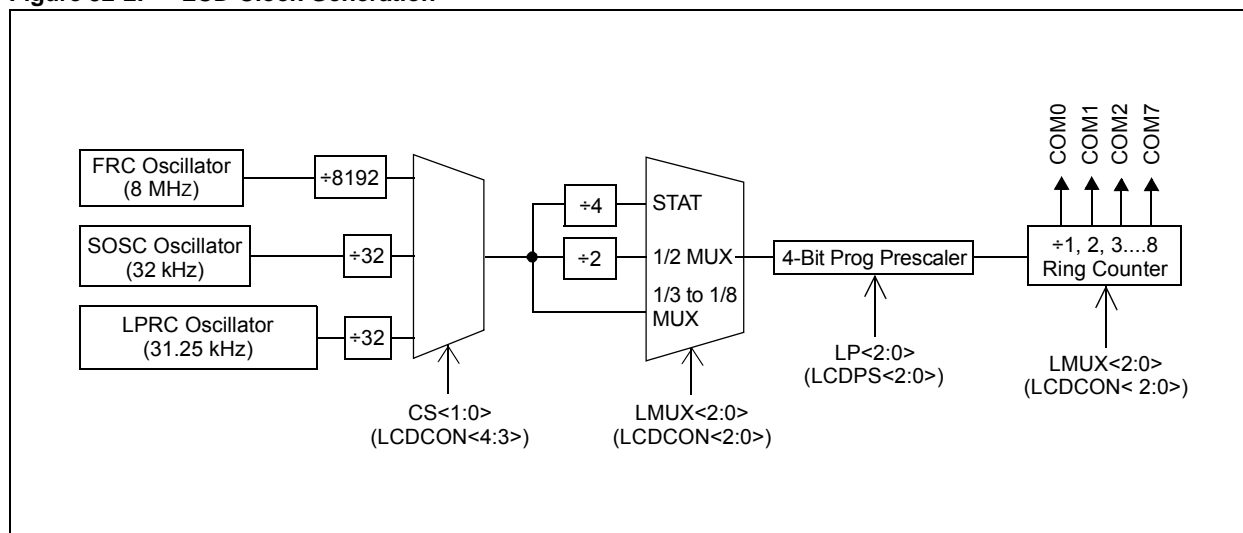
These clock sources are selected through the bits, CS<1:0> (LCDCON<4:3>).

52.4.1 LCD Prescaler

A 16-bit counter is available as a prescaler for the LCD clock. The prescaler is not directly readable or writable. Its value is set by the LP<2:0> bits (LCDPS<2:0>) that determine the prescaler assignment and prescale ratio.

Selectable prescale values are from 1:1 through 1:16, in increments of one.

Figure 52-2: LCD Clock Generation



52.5 LCD BIAS TYPES

The LCD module can be configured in one of three bias types:

- Static Bias (two voltage levels: V_{SS} and V_{DD})
- 1/2 Bias (three voltage levels: V_{SS} , $1/2 V_{DD}$ and V_{DD})
- 1/3 Bias (four voltage levels: V_{SS} , $1/3 V_{DD}$, $2/3 V_{DD}$ and V_{DD})

LCD bias voltages can be generated with an internal resistor ladder, internal bias generator or external resistor ladder.

52.5.1 Internal Resistor Biasing

This mode does not use external resistors, but rather internal resistor ladders that are configured to generate the bias voltage.

The internal reference ladder actually consists of three separate ladders. Disabling the internal reference ladder disconnects all of the ladders, allowing external voltages to be supplied.

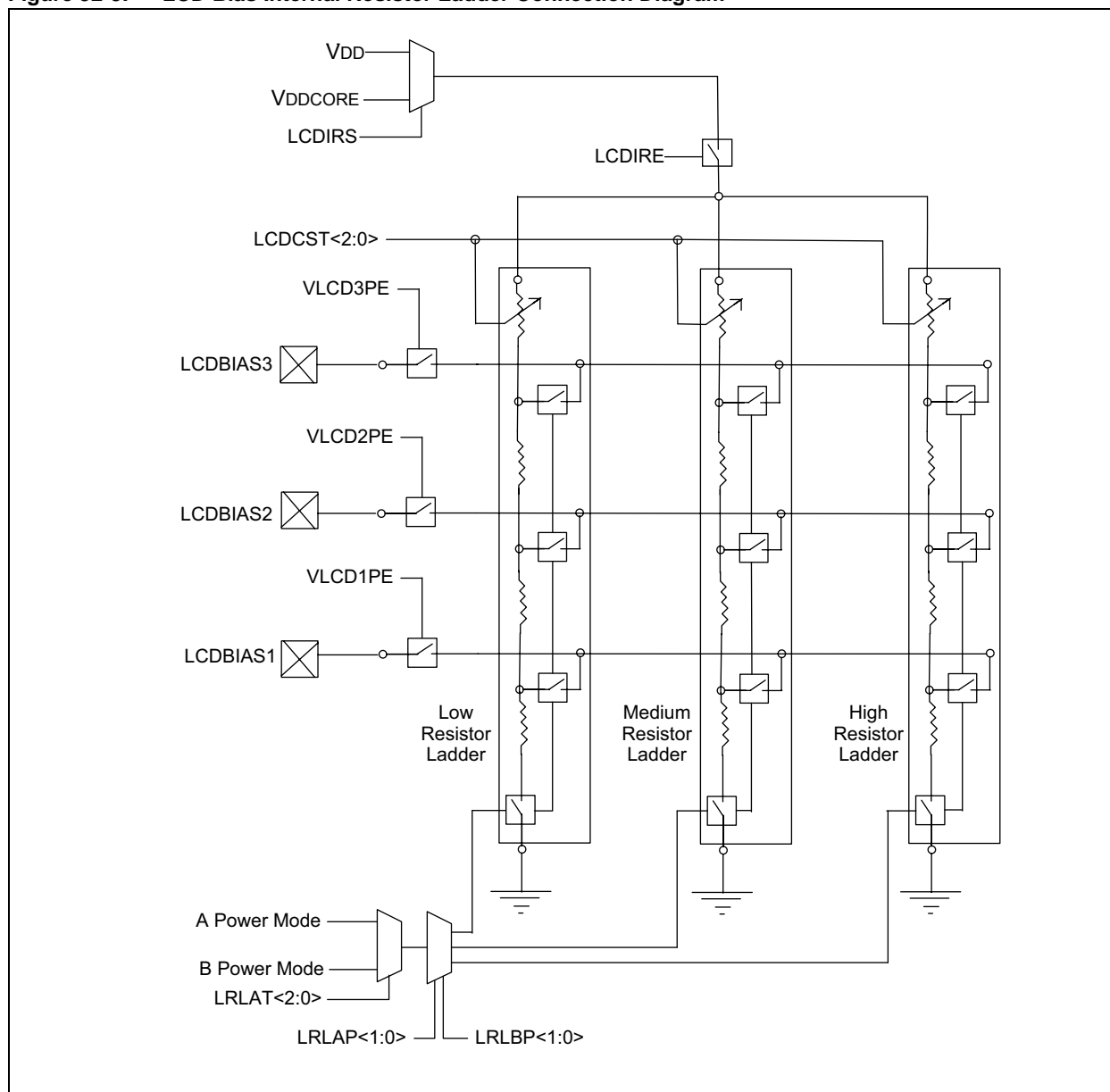
Depending on the total resistance of the resistor ladders, the biasing can be classified as low, medium or high power.

Table 52-3 shows the total resistance of each of the ladders. Figure 52-3 shows the internal resistor ladder connections. When the internal resistor ladder is selected, the bias voltage can either be from V_{DD} or from V_{DDCORE} , depending on the LCDIRS setting. It can also provide software contrast control (using $LCDCST<2:0>$).

Table 52-3: Internal Resistance Ladder Power Modes

Power Mode	Nominal Resistance of Entire Ladder	I_{DD}
Low	3 M Ω	1 μ A
Medium	300 k Ω	10 μ A
High	30 k Ω	100 μ A

Figure 52-3: LCD Bias Internal Resistor Ladder Connection Diagram



There are two power modes, designated as “Mode A” and “Mode B”. Mode A is set by the bits, LRLAP<1:0>, and Mode B by LRLBP<1:0>. The resistor ladder to use for Modes A and B are selected by the bits, LRLAP<1:0> and LRLBP<1:0>, respectively.

Each ladder has a matching contrast control ladder, tuned to the nominal resistance of the reference ladder. This contrast control resistor can be controlled by LCDST<2:0> (LCDREF<13:11>). Disabling the internal reference ladder results in all of the ladders being disconnected, allowing external voltages to be supplied.

To get additional current in High-Power mode, when LRLAP<1:0> (LCDREF<7:6>) = 11, both the medium and high-power resistor ladders are activated.

Whenever the LCD module is inactive LCDPS<5> = 0, the reference ladder will be turned off.

52.5.1.1 AUTOMATIC POWER MODE SWITCHING

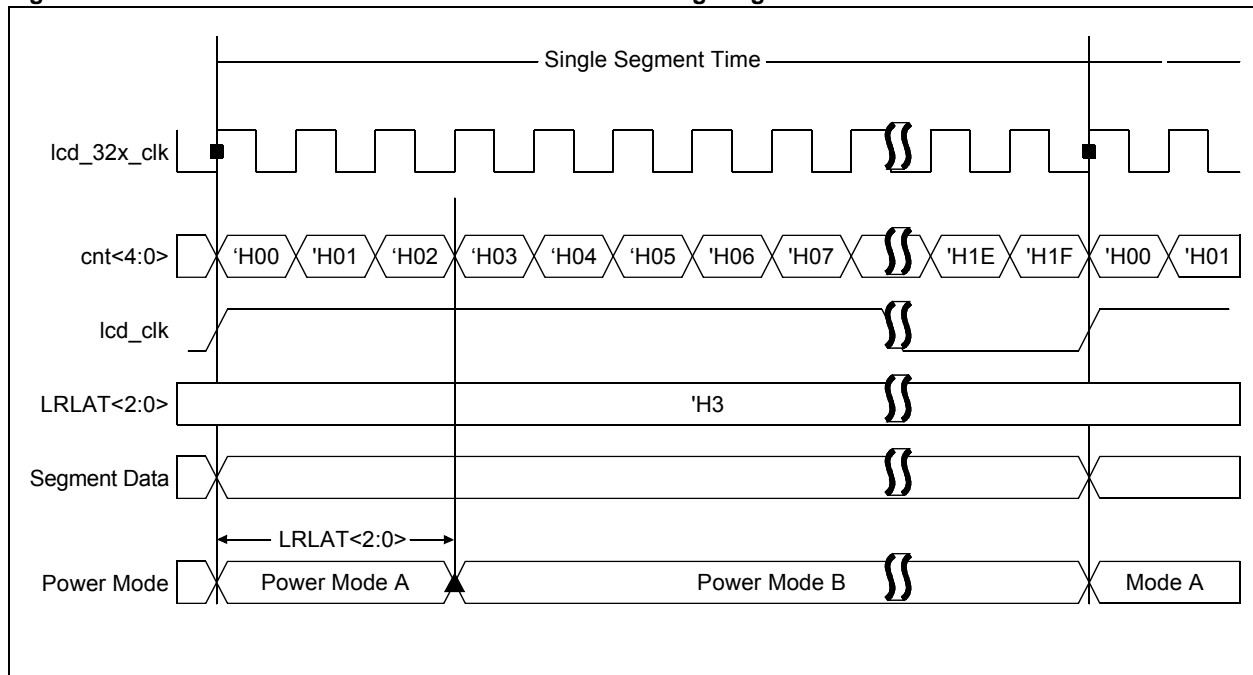
As an LCD segment is electrically only a capacitor, current is drawn only during the interval when the voltage is switching. To minimize total device current, the LCD reference ladder can be operated in a different power mode for the transition portion of the duration. This is controlled by the LCDREF register.

Mode A Power mode is active for a programmable time, beginning at the time when the LCD segment waveform is transitioning. The LRLAT<2:0> (LCDREF<2:0>) bits select how long, or if the Mode A is active. Mode B Power mode is active for the remaining time before the segments or commons change again.

As shown in Figure 52-4, there are 32 counts in a single segment time. Type-A can be chosen during the time when the waveform is in transition. Type-B can be used when the clock is stable or not in transition.

By using this feature of automatic power switching, using Type-A/Type-B, the power consumption can be optimized for a given contrast.

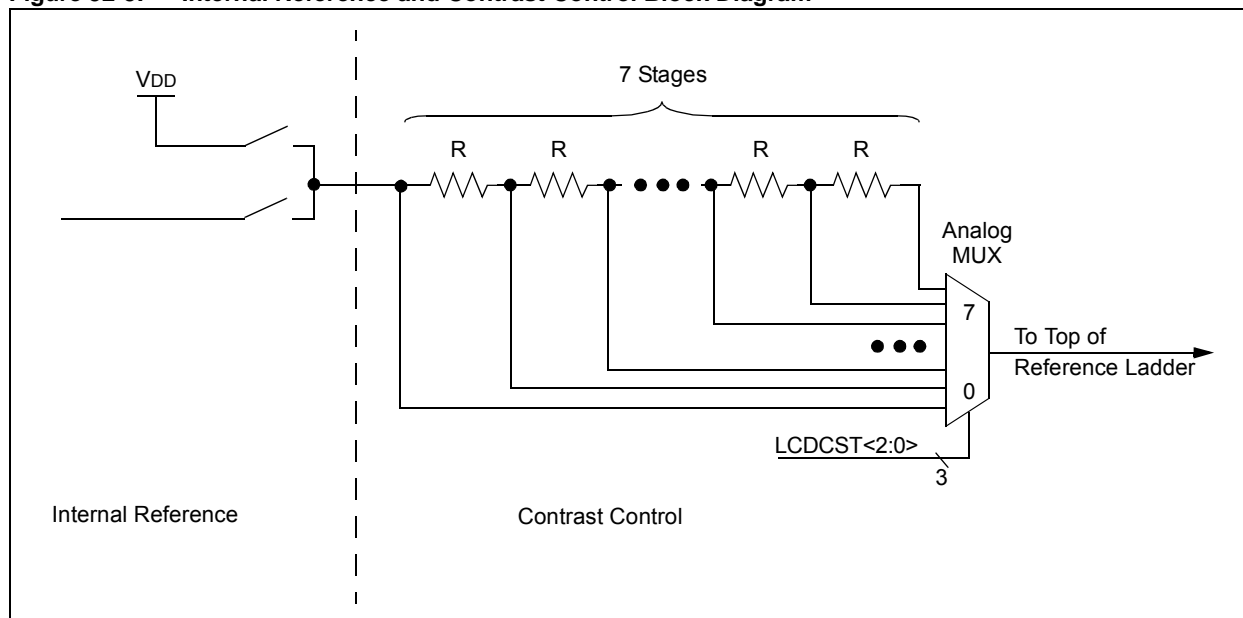
Figure 52-4: LCD Reference Ladder Power Mode Switching Diagram



52.5.1.2 CONTRAST CONTROL

The LCD contrast control circuit consists of a 7-tap resistor ladder, controlled by the LCDCST bits (see Figure 52-5)

Figure 52-5: Internal Reference and Contrast Control Block Diagram



52.5.1.3 INTERNAL REFERENCE

Under firmware control, an internal reference for the LCD bias voltages can be enabled. When enabled, the source of this voltage can be VDD.

When no internal reference is selected, the LCD contrast control circuit is disabled and the LCD bias must be provided externally. Whenever the LCD module is inactive (LCDA = 0), the internal reference will be turned off.

52.5.1.4 VLCDx PINS

The VLCD3, VLCD2 and VLCD1 pins provide the ability for an external LCD bias network to be used instead of the internal ladder. Use of the VLCDx pins does not prevent use of the internal ladder.

Each VLCD pin has an independent control in the LCDREF register, allowing access to any or all of the LCD bias signals.

This architecture allows for maximum flexibility in different applications. The VLCDx pins could be used to add capacitors to the internal reference ladder for increasing the drive capacity. For applications where the internal contrast control is insufficient, the firmware can choose to enable only the VLCD3 pin, allowing an external contrast control circuit to use the internal reference divider.

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Register 52-5: LCDREF: LCD Reference Ladder Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCDIRE	—	LCDCST2	LCDCST1	LCDCST0	VLCD3PE	VLCD2PE	VLCD1PE
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
LRLAP1	LRLAP0	LRLBP1	LRLBP0	—	LRLAT2	LRLAT1	LRLAT0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **LCDIRE:** LCD Internal Reference Enable bit
1 = Internal LCD reference is enabled and connected to the internal contrast control circuit
0 = Internal LCD reference is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13-11 **LCDCST<2:0>:** LCD Contrast Control bits
Selects the resistance of the LCD contrast control resistor ladder:
111 = Resistor ladder is at maximum resistance (minimum contrast)
110 = Resistor ladder is at 6/7th of maximum resistance
101 = Resistor ladder is at 5/7th of maximum resistance
100 = Resistor ladder is at 4/7th of maximum resistance
011 = Resistor ladder is at 3/7th of maximum resistance
010 = Resistor ladder is at 2/7th of maximum resistance
001 = Resistor ladder is at 1/7th of maximum resistance
000 = Minimum resistance (maximum contrast); resistor ladder is shorted
- bit 10 **VLCD3PE:** Bias 3 Pin Enable bit
1 = Bias 3 level is connected to the external pin, LCDBIAS3
0 = Bias 3 level is internal (internal resistor ladder)
- bit 9 **VLCD2PE:** Bias 2 Pin Enable bit
1 = Bias 2 level is connected to the external pin, LCDBIAS2
0 = Bias 2 level is internal (internal resistor ladder)
- bit 8 **VLCD1PE:** Bias 1 Pin Enable bit
1 = Bias 1 level is connected to the external pin, LCDBIAS1
0 = Bias 1 level is internal (internal resistor ladder)
- bit 7-6 **LRLAP<1:0>:** LCD Reference Ladder A Time Power Control bits
During Time Interval A:
11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected
- bit 5-4 **LRLBP<1:0>:** LCD Reference Ladder B Time Power Control bits
During Time Interval B:
11 = Internal LCD reference ladder is powered in High-Power mode
10 = Internal LCD reference ladder is powered in Medium Power mode
01 = Internal LCD reference ladder is powered in Low-Power mode
00 = Internal LCD reference ladder is powered down and unconnected
- bit 3 **Unimplemented:** Read as '0'

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bit 2-0

LRLAT<2:0>: LCD Reference Ladder A Time Interval Control bits

Sets the number of 32 clock counts when the A Time Interval Power mode is active.

For Type-A Waveforms (WFT = 0):

111 = Internal LCD reference ladder is in A Power mode for 7 clocks and B Power mode for 9 clocks
110 = Internal LCD reference ladder is in A Power mode for 6 clocks and B Power mode for 10 clocks
101 = Internal LCD reference ladder is in A Power mode for 5 clocks and B Power mode for 11 clocks
100 = Internal LCD reference ladder is in A Power mode for 4 clocks and B Power mode for 12 clocks
011 = Internal LCD reference ladder is in A Power mode for 3 clocks and B Power mode for 13 clocks
010 = Internal LCD reference ladder is in A Power mode for 2 clocks and B Power mode for 14 clocks
001 = Internal LCD reference ladder is in A Power mode for 1 clock and B Power mode for 15 clocks
000 = Internal LCD reference ladder is always in B Power mode

For Type-B Waveforms (WFT = 1):

111 = Internal LCD reference ladder is in A Power mode for 7 clocks and B Power mode for 25 clocks
110 = Internal LCD reference ladder is in A Power mode for 6 clocks and B Power mode for 26 clocks
101 = Internal LCD reference ladder is in A Power mode for 5 clocks and B Power mode for 27 clocks
100 = Internal LCD reference ladder is in A Power mode for 4 clocks and B Power mode for 28 clocks
011 = Internal LCD reference ladder is in A Power mode for 3 clocks and B Power mode for 29 clocks
010 = Internal LCD reference ladder is in A Power mode for 2 clocks and B Power mode for 30 clocks
001 = Internal LCD reference ladder is in A Power mode for 1 clock and B Power mode for 31 clocks
000 = Internal LCD reference ladder is always in B Power mode

52.5.2 LCD Bias Generation

The LCD driver module is capable of generating the required bias voltages for LCD operation with a minimum of external components. This includes the ability to generate the different voltage levels required by the different bias types that are required by the LCD. The driver module can also provide bias voltages, both above and below microcontroller VDD, through the use of an on-chip LCD voltage regulator.

52.5.2.1 LCD BIAS TYPES

PIC24FJXXXGA3XX family devices support three bias types based on the waveforms generated to control segments and commons:

- Static (two discrete levels)
- 1/2 Bias (three discrete levels)
- 1/3 Bias (four discrete levels)

The use of different waveforms in driving the LCD is discussed in more detail in **Section 52.10 “LCD Waveform Generation”**.

52.5.2.2 LCD VOLTAGE REGULATOR

The purpose of the LCD regulator is to provide proper bias voltage and good contrast for the LCD, regardless of VDD levels. This module contains a charge pump and internal voltage reference. The regulator can be configured by using external components to boost bias voltage above VDD. It can also operate a display at a constant voltage below VDD. The regulator can also be selectively disabled to allow bias voltages to be generated by an external resistor network.

The LCD regulator is controlled through the LCDREG register (Register 52-6). It is enabled or disabled using the CKSEL<1:0> bits, while the charge pump can be selectively enabled using the CPEN bit. When the regulator is enabled, the MODE13 bit is used to select the bias type. The peak LCD bias voltage, measured as a difference between the potentials of LCDBIAS3 and LCDBIAS0, is configured with the BIAS bits.

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Register 52-6: LCDREG: LCD Voltage Regulator Control Register

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
CPEN	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
—	—	BIAS2	BIAS1	BIAS0	MODE13	CKSEL1	CKSEL 0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CPEN:** LCD Charge Pump Enable bit
1 = Charge pump enabled; highest LCD bias voltage is 3.6V
0 = Charge pump disabled; highest LCD bias voltage is AVDD
- bit 14-6 **Unimplemented:** Read as '0'
- bit 5-3 **BIAS<2:0>:** Regulator Voltage Output Control bits
111 = 3.60V peak (offset on LCDBIAS0 of 0V)
110 = 3.47V peak (offset on LCDBIAS0 of 0.13V)
101 = 3.34V peak (offset on LCDBIAS0 of 0.26V)
100 = 3.21V peak (offset on LCDBIAS0 of 0.39V)
011 = 3.08V peak (offset on LCDBIAS0 of 0.52V)
010 = 2.95V peak (offset on LCDBIAS0 of 0.65V)
001 = 2.82V peak (offset on LCDBIAS0 of 0.78V)
000 = 2.69V peak (offset on LCDBIAS0 of 0.91V)
- bit 2 **MODE13:** 1/3 LCD Bias Enable bit
1 = Regulator output supports 1/3 LCD Bias mode
0 = Regulator output supports Static LCD Bias mode
- bit 1-0 **CKSEL<1:0>:** Regulator Clock Source Select bits
11 = 8 MHz FRC
10 = 31 kHz LPRC
01 = SOSC
00 = LCD regulator disabled

52.5.3 Bias Configurations

PIC24FJXXXGA3XX family devices have four distinct circuit configurations for LCD bias generation:

- M0: Regulator with Boost
- M1: Regulator without Boost
- M2: Resistor Ladder with Software Contrast
- M3: Resistor Ladder with Hardware Contrast

52.5.3.1 M0 (REGULATOR WITH BOOST)

In M0 operation, the LCD charge pump feature is enabled. This allows the regulator to generate voltages up to +3.6V to the LCD (as measured at LCDBIAS3).

M0 uses a flyback capacitor connected between VLCAP1 and VLCAP2, as well as filter capacitors on LCDBIAS0 through LCDBIAS3, to obtain the required voltage boost (Figure 52-6). The output voltage (VBIAS) is the difference of potential between LCDBIAS3 and LCDBIAS0. It is set by the BIAS<2:0> bits which adjust the offset between LCDBIAS0 and Vss. The flyback capacitor (CFLY) acts as a charge storage element for large LCD loads. This mode is useful in those cases where the voltage requirements of the LCD are higher than the microcontroller's VDD. It also permits software control of the display's contrast, by adjustment of bias voltage, by changing the value of the BIAS bits.

M0 supports Static and 1/3 Bias types. Generation of the voltage levels for 1/3 Bias is handled automatically, but must be configured in software.

M0 is enabled by selecting a valid regulator clock source (CKSEL<1:0> set to any value except '00') and setting the CPEN bit. If Static Bias type is required, the MODE13 bit must be cleared.

52.5.3.2 M1 (REGULATOR WITHOUT BOOST)

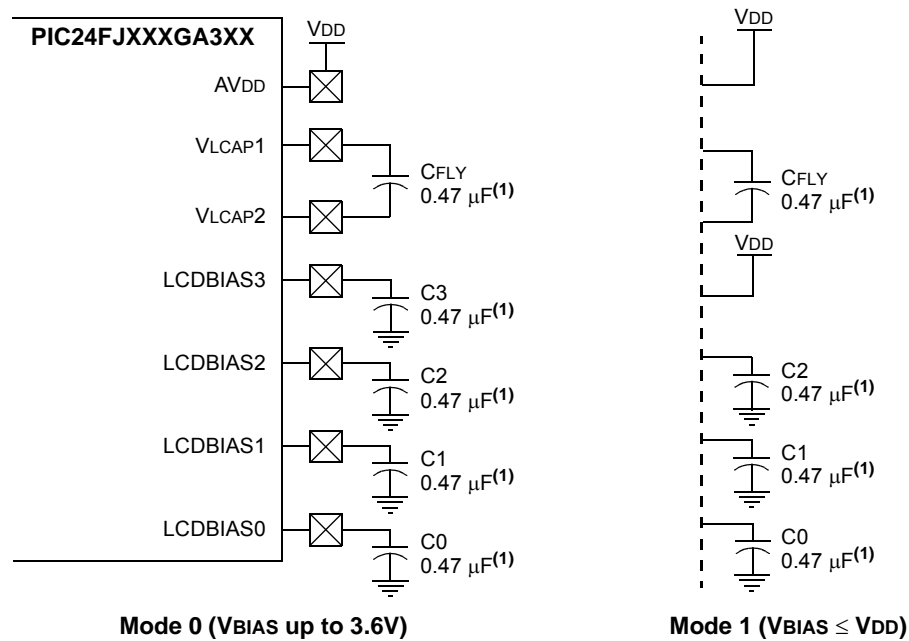
M1 operation is similar to M0, but does not use the LCD charge pump. It can provide VBIAS up to the voltage level supplied directly to LCDBIAS3. It can be used in cases where VDD for the application is expected to never drop below a level that can provide adequate contrast for the LCD. The connection of external components is very similar to M0, except that LCDBIAS3 must be tied directly to VDD (Figure 52-6).

Note: When the device is put to Sleep while operating in mode M0 or M1, make sure that the bias capacitors are fully discharged to get the lowest Sleep current.

The BIAS<2:0> bits can still be used to adjust contrast in software by changing VBIAS. As with M0, changing these bits changes the offset between LCDBIAS0 and Vss. In M1, this is reflected in the change between the LCDBIAS0 and the voltage tied to LCDBIAS3. Thus, if VDD should change, VBIAS will also change; where in M0, the level of VBIAS is constant.

Like M0, M1 supports Static and 1/3 Bias types. Generation of the voltage levels for 1/3 Bias is handled automatically but must be configured in software. M1 is enabled by selecting a valid regulator clock source (CKSEL<1:0> set to any value except '00') and clearing the CPEN bit. If 1/3 Bias type is required, the MODE13 bit should also be set.

Figure 52-6: LCD Regulator Connections for M0 and M1 Configurations



Note 1: These values are provided for design guidance only. They should be optimized for the application by the designer based on the actual LCD specifications.

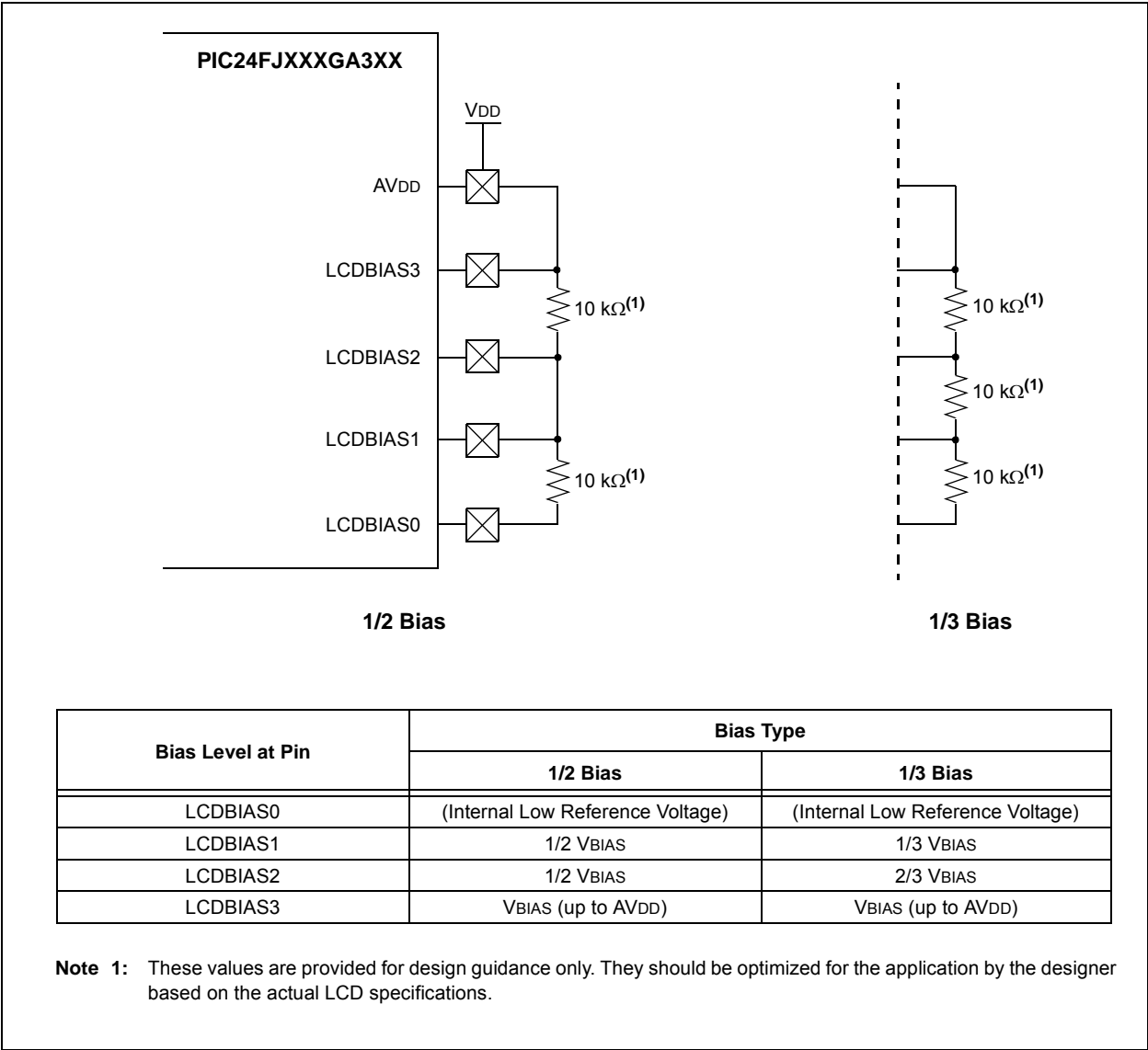
52.5.3.3 M2 (EXTERNAL RESISTOR LADDER WITH SOFTWARE CONTRAST)

M2 operation also uses the LCD regulator but disables the charge pump. The regulator’s internal voltage reference remains active as a way to regulate contrast. It is used in cases where the current requirements of the LCD exceed the capacity of the regulator’s charge pump.

In this configuration, the LCD bias voltage levels are created by an external resistor voltage divider, connected across LCDBIAS0 through LCDBIAS3, with the top of the divider tied to VDD (Figure 52-7). The potential at the bottom of the ladder is determined by the LCD regulator’s voltage reference, tied internally to LCDBIAS0. The bias type is determined by the voltages on the LCDBIAS pins, which are controlled by the configuration of the resistor ladder. Most applications using M2 will use a 1/3 or 1/2 Bias type. While Static Bias can also be used, it offers extremely limited contrast range and additional current consumption over other bias generation modes.

Like M1, the LCDBIAS bits can be used to control contrast, limited by the level of VDD supplied to the device. Also, since there is no capacitor required across VLCAP1 and VLCAP2, these pins are available as digital I/O ports, RG2 and RG3. M2 is selected by clearing the CKSEL<1:0> bits and setting the CPEN bit.

Figure 52-7: Resistor Ladder Connections for M2 Configuration



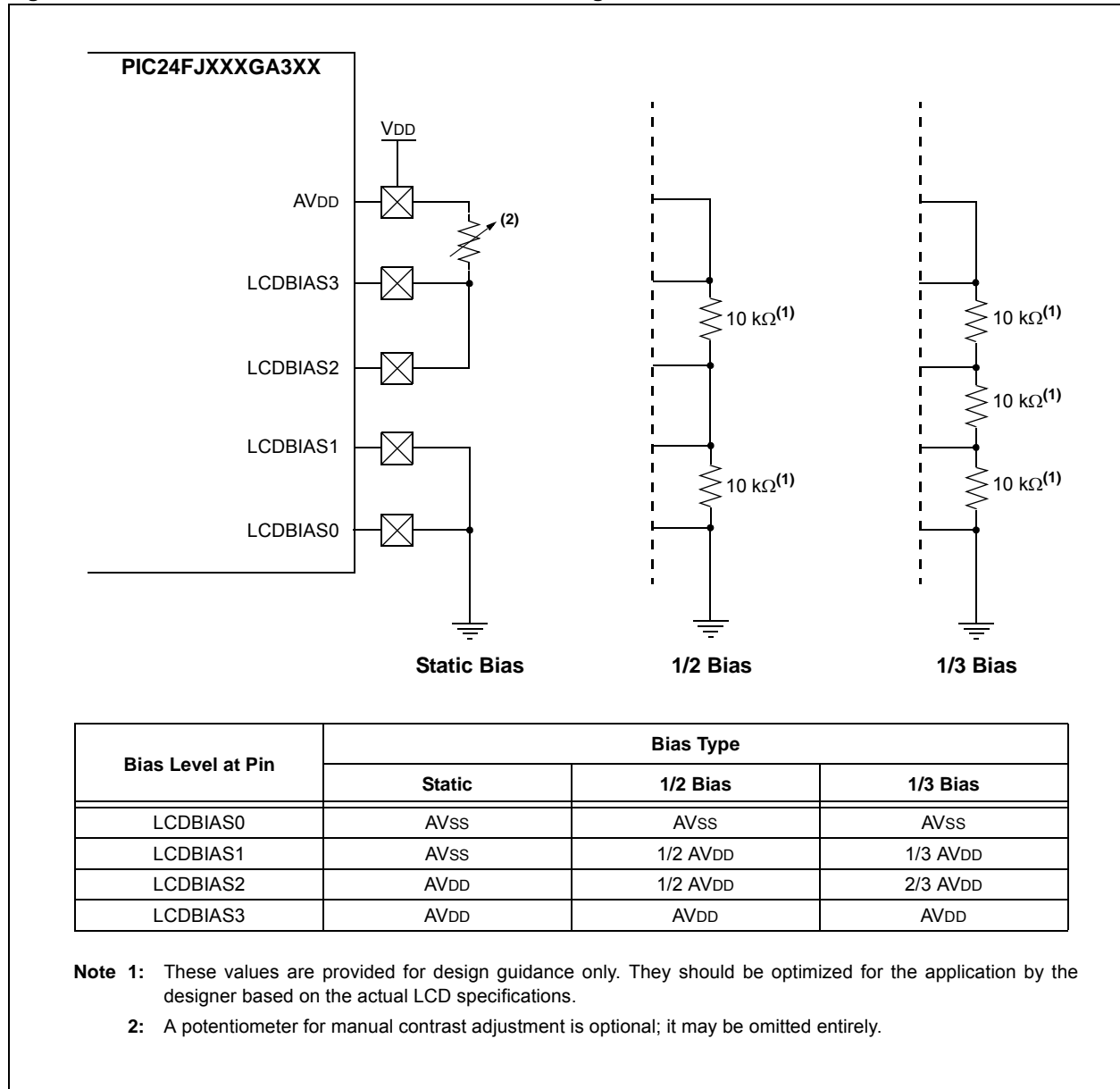
52.5.3.4 M3 (HARDWARE CONTRAST)

In M3, the LCD regulator is completely disabled. Like M2, LCD bias levels are tied to AVDD and are generated using an external divider. The difference is that the internal voltage reference is also disabled and the bottom of the ladder is tied to ground (VSS); see Figure 52-8. The value of the resistors, and the difference between VSS and VDD, determine the contrast range; no software adjustment is possible. This configuration is also used where the LCD module's current requirements exceed the capacity of the charge pump and software contrast control is not needed.

Depending on the bias type required, resistors are connected between some or all of the pins. A potentiometer can also be connected between LCDBIAS3 and VDD to allow for hardware controlled contrast adjustment.

M3 is selected by clearing the CKSEL<1:0> and CPEN bits.

Figure 52-8: Resistor Ladder Connections for M3 Configuration



52.5.4 Design Considerations For The LCD Charge Pump

When designing applications that use the LCD regulator with the charge pump enabled, users must always consider both the dynamic current and RMS (static) current requirements of the display, and what the charge pump can deliver. Both dynamic and static current can be determined by Equation 52-1:

Equation 52-1:

$$I = C \times \frac{dV}{dT}$$

For dynamic current, C is the value of the capacitors attached to LCDBIAS3 and LCDBIAS2. The variable, dV, is the voltage drop allowed on C2 and C3 during a voltage switch on the LCD display, and dT is the duration of the transient current after a clock pulse occurs.

For practical design purposes, these will be assumed to be 0.047 iF for C, 0.1V for dV and 1 is for dT. This yields a dynamic current of 4.7 mA for 1 is.

RMS current is determined by the value of C_{FLY} for C, the voltage across VLCAP1 and VLCAP2 for dV and the regulator clock period (TPER) for dT. Assuming a C_{FLY} value of 0.047 iF, a value of 1.02V across C_{FLY} and a TPER of 30, the maximum theoretical static current will be 1.8 mA. Since the charge pump must charge five capacitors, the maximum current becomes 360 iA.

For a real-world assumption of 50% efficiency, this yields a practical current of 180 iA. Users should compare the calculated current capacity against the requirements of the LCD. While dV and dT are relatively fixed by device design, the values of C_{FLY} and the capacitors on the LCDBIAS pins can be changed to increase or decrease current. As always, any changes should be evaluated in the actual circuit for their impact on the application.

52.6 LCD MULTIPLEX TYPES

The LCD driver module can be configured into four multiplex types:

- Static (only COM0 used)
- 1/2 Multiplex (COM0 and COM1 are used)
- 1/3 Multiplex (COM0, COM1 and COM2 are used)
- 1/4 Multiplex (COM0, COM1, COM2 and COM3 are used)
- 1/5 Multiplex (COM0, COM1, COM2, COM3 and COM4 are used)
- 1/6 Multiplex (COM0, COM1, COM2, COM3, COM4 and COM5 are used)
- 1/7 Multiplex (COM0, COM1, COM2, COM3, COM4, COM5 and COM6 are used)
- 1/8 Multiplex (COM0, COM1, COM2, COM3, COM4, COM5, COM6 and COM7 are used)

The LMUX<2:0> bits setting (LCDCON<2:0>) decides the function of the COM pins. (For details, see Table 52-4.)

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, the TRIS setting of that pin is overridden.

Note: On a Power-on Reset, the LMUX<2:0> bits are '000'.

Table 52-4: COM<7:0> Pin Function

LMUX<2:0>	COM7 Pin	COM6 Pin	COM5 Pin	COM4 Pin	COM3 Pin	COM2 Pin	COM1 Pin	COM0 Pin
111	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
110	I/O Pin	COM6	COM5	COM4	COM3	COM2	COM1	COM0
101	I/O Pin	I/O Pin	COM5	COM4	COM3	COM2	COM1	COM0
100	I/O Pin	I/O Pin	I/O Pin	COM4	COM3	COM2	COM1	COM0
011	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM3	COM2	COM1	COM0
010	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM2	COM1	COM0
001	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM1	COM0
000	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	I/O Pin	COM0

Note: Pins, COM<7:4>, can also be used as SEG pins when 1/4 Multiplex to Static Multiplex are used. These pins can be used as I/O pins only if the respective bits in the LCDSEx registers are set to '0'.

52.7 SEGMENT ENABLES

The LCDSEx registers are used to select the pin function for each segment pin. The selection allows each pin to operate as either an LCD segment driver or a digital only pin. To configure the pin as a segment pin, the corresponding bits in the LCDSEx registers must be set to '1'.

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSEx registers overrides any bit settings in the corresponding TRIS register.

Note: On a Power-on Reset, these pins are configured as digital I/O.

52.8 PIXEL CONTROL

The LCDDATAx registers contain bits that define the state of each pixel. Each bit defines one unique pixel. Table 52-2 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals.

Any LCD pixel location not being used for display can be used as general purpose RAM.

52.9 LCD FRAME FREQUENCY

The rate at which the COM and SEG outputs change is called the LCD frame frequency.

Table 52-5: Frame Frequency Formulas

Multiplex	Frame Frequency =
Static (000)	$\text{Clock Source}/(4 \times 1 \times (\text{LP}<3:0> + 1))$
1/2 (001)	$\text{Clock Source}/(2 \times 2 \times (\text{LP}<3:0> + 1))$
1/3 (010)	$\text{Clock Source}/(1 \times 3 \times (\text{LP}<3:0> + 1))$
1/4 (011)	$\text{Clock Source}/(1 \times 4 \times (\text{LP}<3:0> + 1))$
1/5 (100)	$\text{Clock Source}/(1 \times 5 \times (\text{LP}<3:0> + 1))$
1/6 (101)	$\text{Clock Source}/(1 \times 6 \times (\text{LP}<3:0> + 1))$
1/7 (110)	$\text{Clock Source}/(1 \times 7 \times (\text{LP}<3:0> + 1))$
1/8 (111)	$\text{Clock Source}/(1 \times 8 \times (\text{LP}<3:0> + 1))$

Note: Clock source is FRC/8192, SOSC/32 or LPRC/32.

52.10 LCD WAVEFORM GENERATION

LCD waveform generation is based on the philosophy that the net AC voltage across the dark pixel should be maximized and the net AC voltage across the clear pixel should be minimized. The net DC voltage across any pixel should be zero.

The COM signal represents the time slice for each common, while the SEG contains the pixel data.

The pixel signal (COM-SEG) will have no DC component and can take only one of the two rms values. The higher rms value will create a dark pixel and a lower rms value will create a clear pixel.

As the number of commons increases, the delta between the two rms values decreases. The delta represents the maximum contrast that the display can have.

The LCDs can be driven by two types of waveforms: Type-A and Type-B. In a Type-A waveform, the phase changes within each common type, whereas a Type-B waveform's phase changes on each frame boundary. Thus, Type-A waveforms maintain 0 V_{DC} over a single frame, whereas Type-B waveforms take two frames.

Note: If Sleep has to be executed with LCD Sleep enabled (SLPEN (LCDCON<6>) = 1), care must be taken to execute Sleep only when the V_{DC} on all the pixels is '0'.

Figure 52-9 through Figure 52-21 provide waveforms for Static, Half-Multiplex, One-Third Multiplex and Quarter Multiplex drives for Type-A and Type-B waveforms.

Figure 52-9: Type-A/Type-B Waveforms in Static Drive

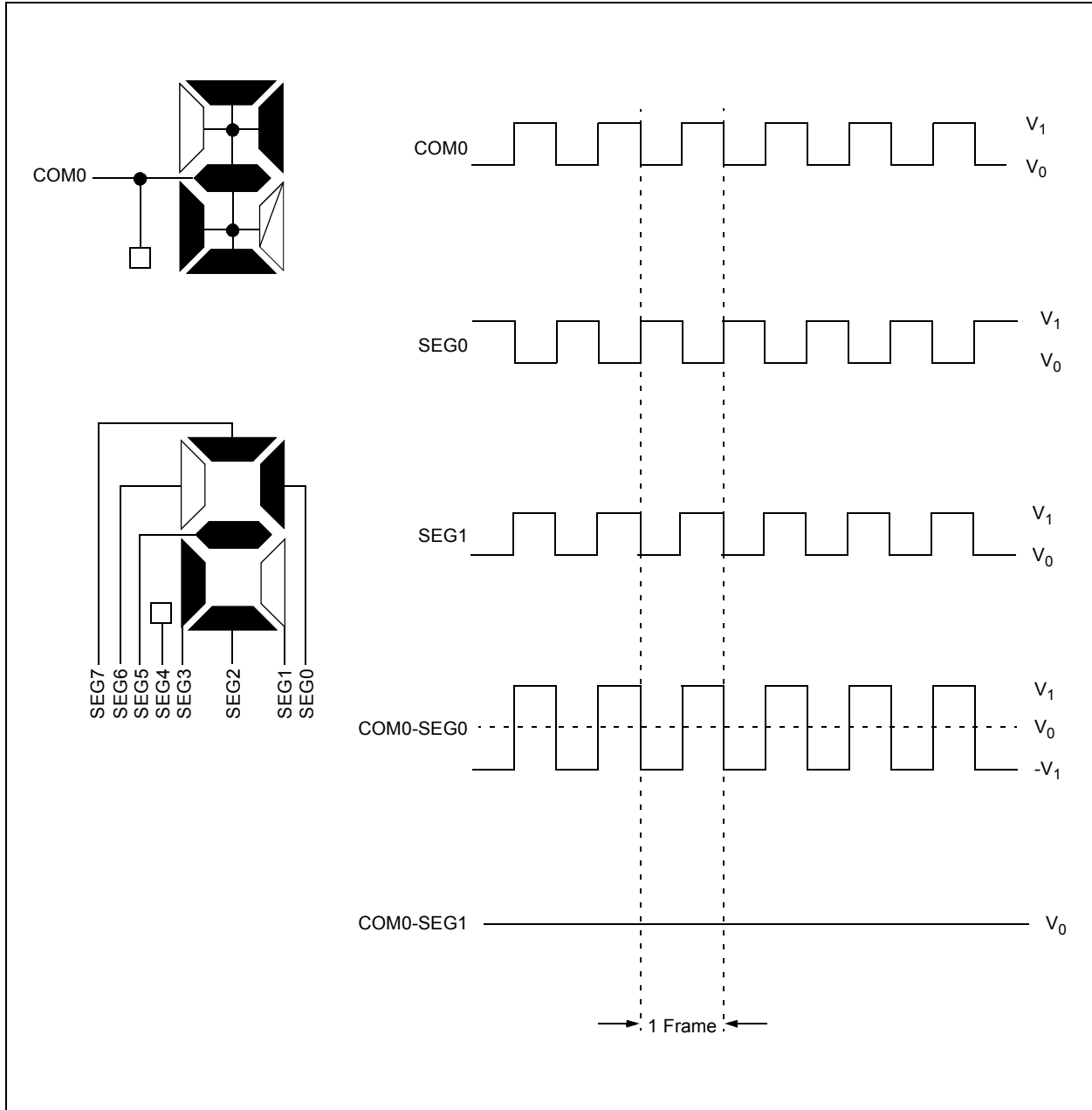


Figure 52-10: Type-A Waveforms in 1/2 MUX, 1/2 Bias Drive

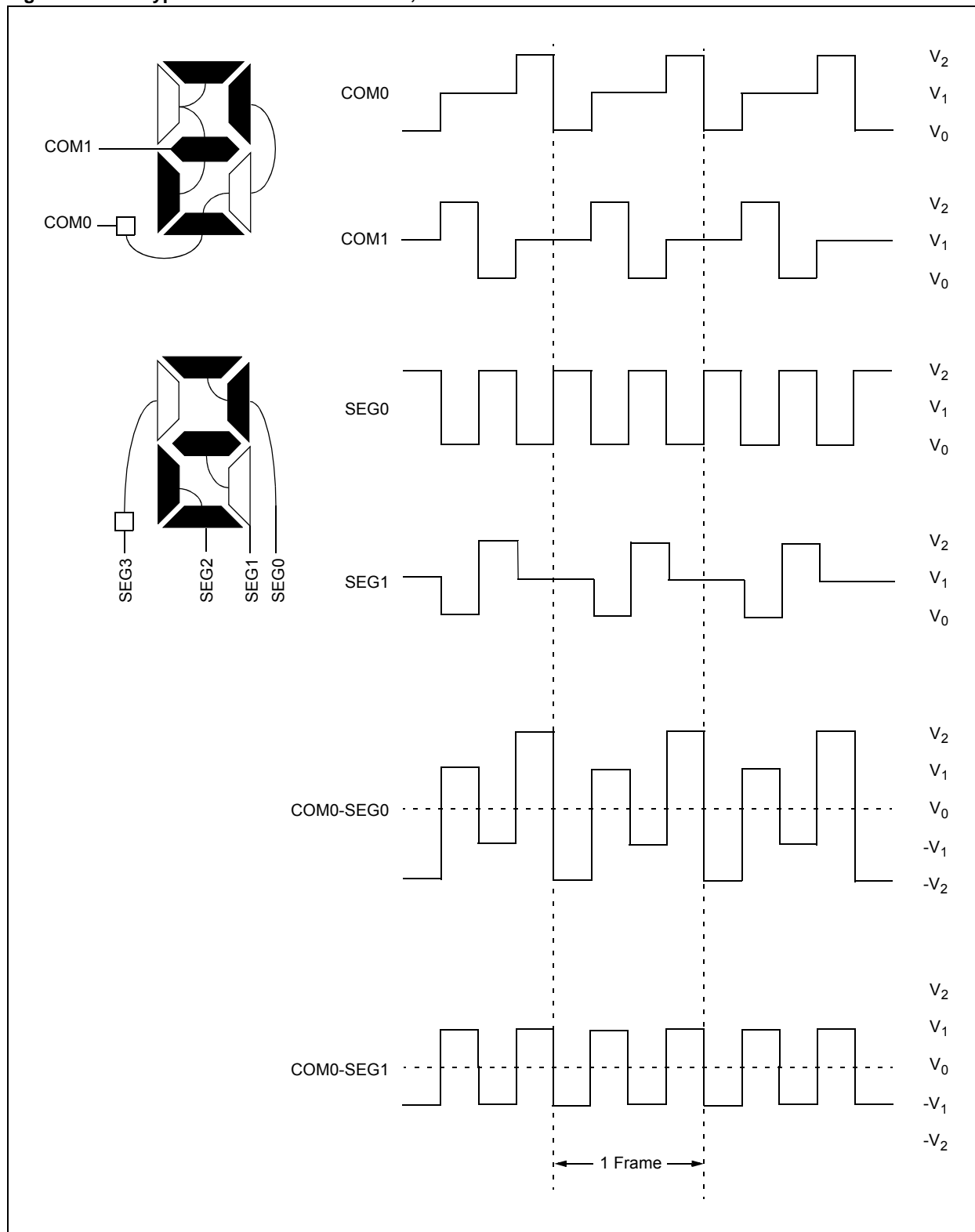


Figure 52-11: Type-B Waveforms in 1/2 MUX, 1/2 Bias Drive

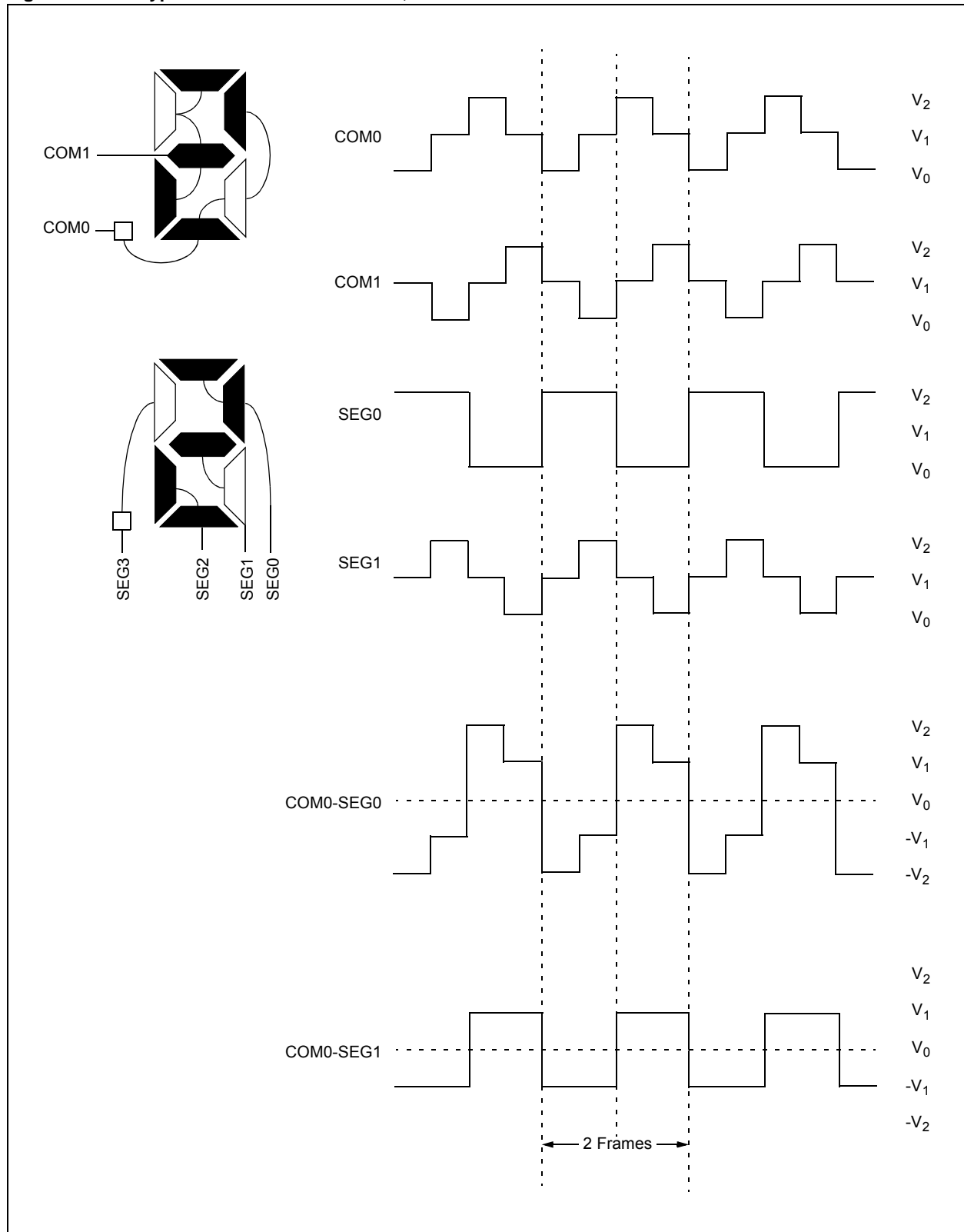


Figure 52-12: Type-A Waveforms in 1/2 MUX, 1/3 Bias Drive

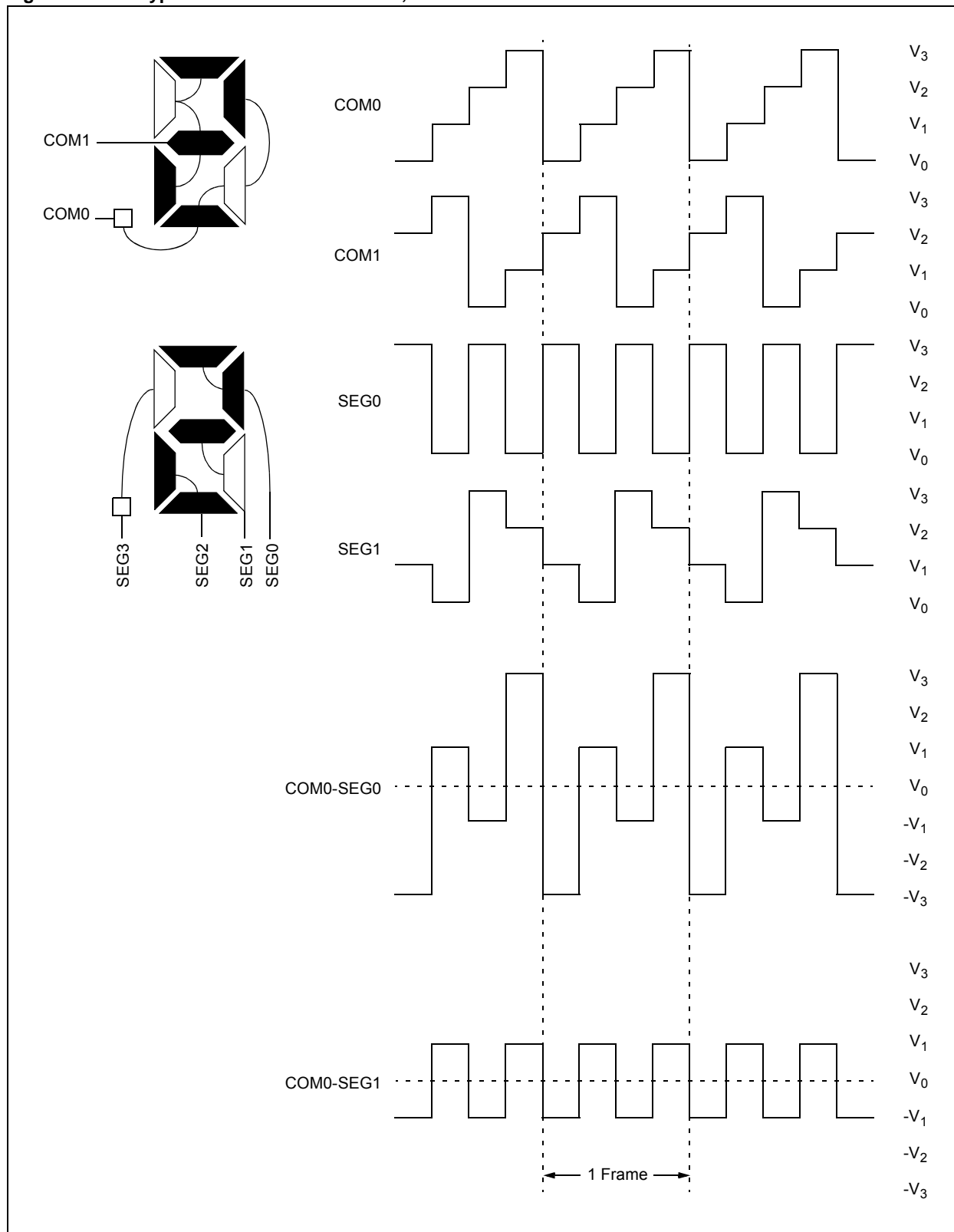


Figure 52-13: Type-B Waveforms in 1/2 MUX, 1/3 Bias Drive

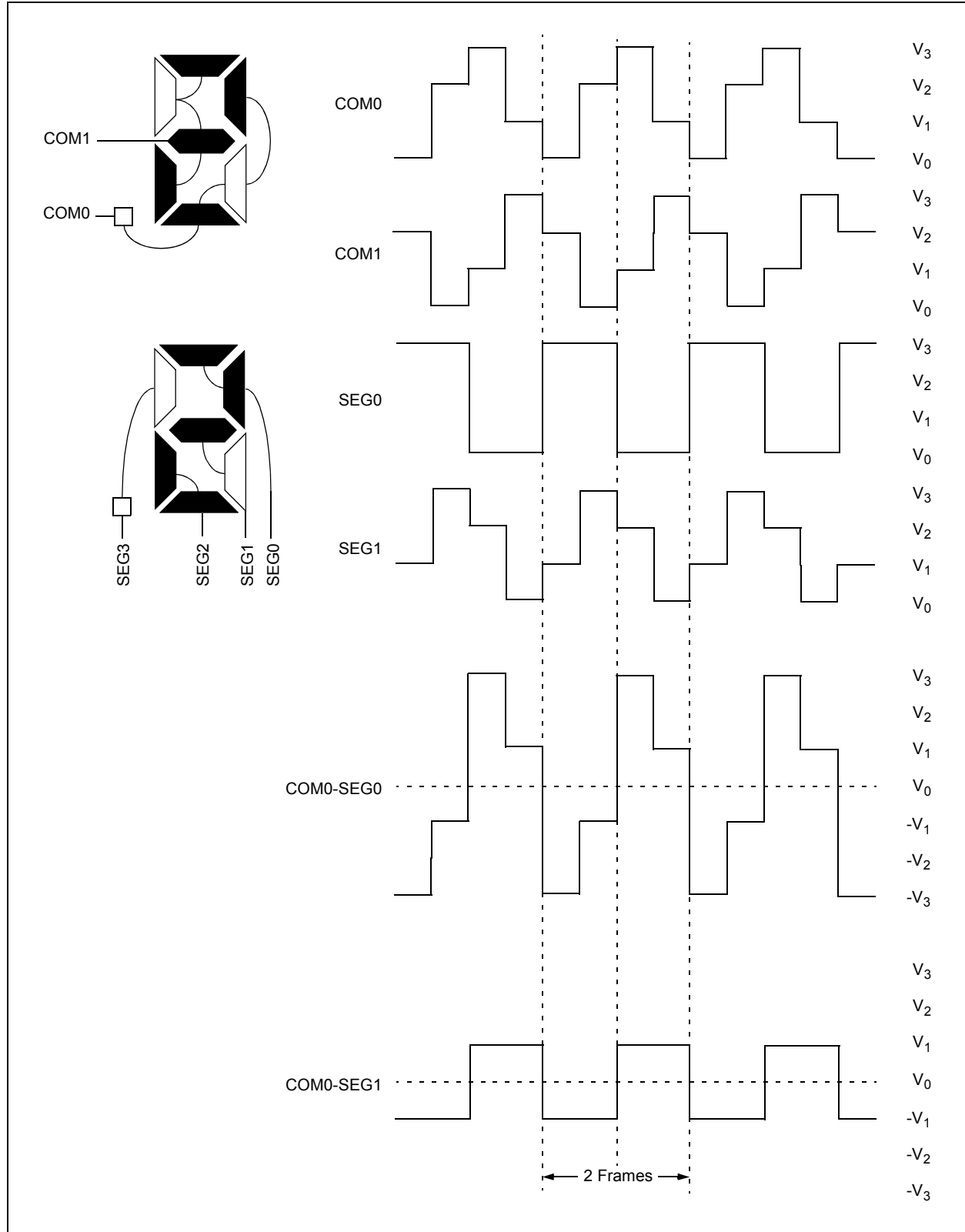


Figure 52-14: Type-A Waveforms in 1/3 MUX, 1/2 Bias Drive

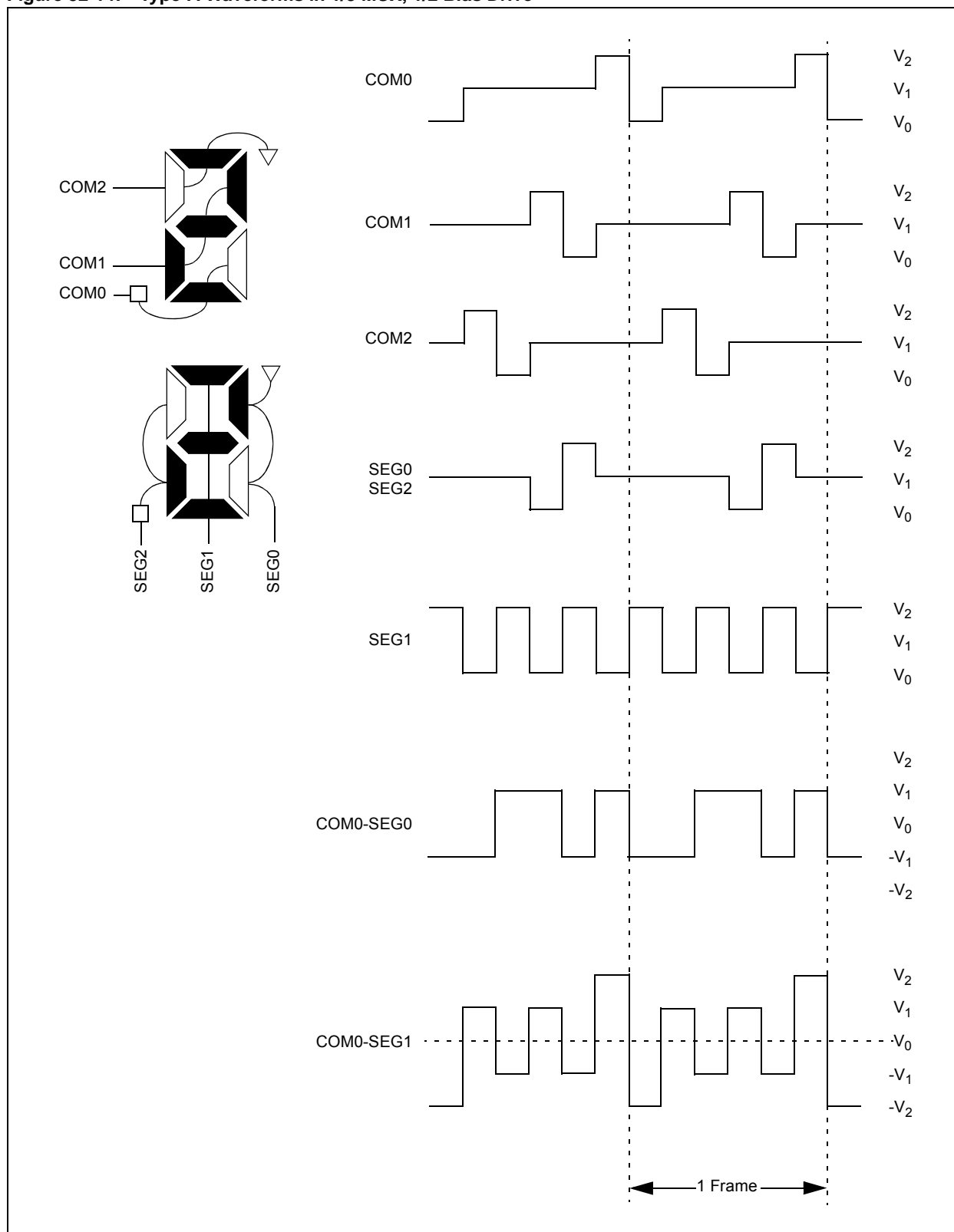


Figure 52-15: Type-B Waveforms in 1/3 MUX, 1/2 Bias Drive

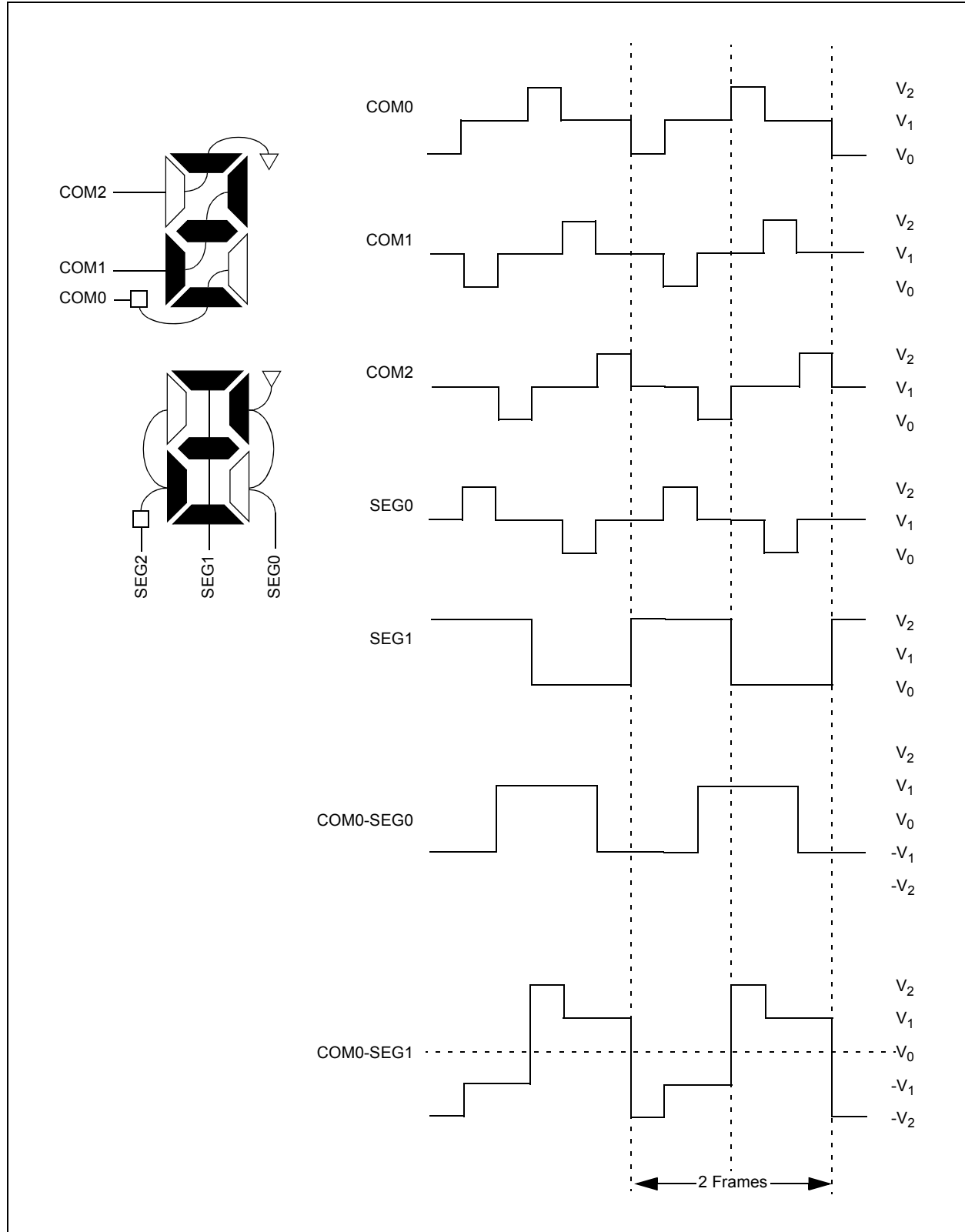


Figure 52-16: Type-A Waveforms in 1/3 MUX, 1/3 Bias Drive

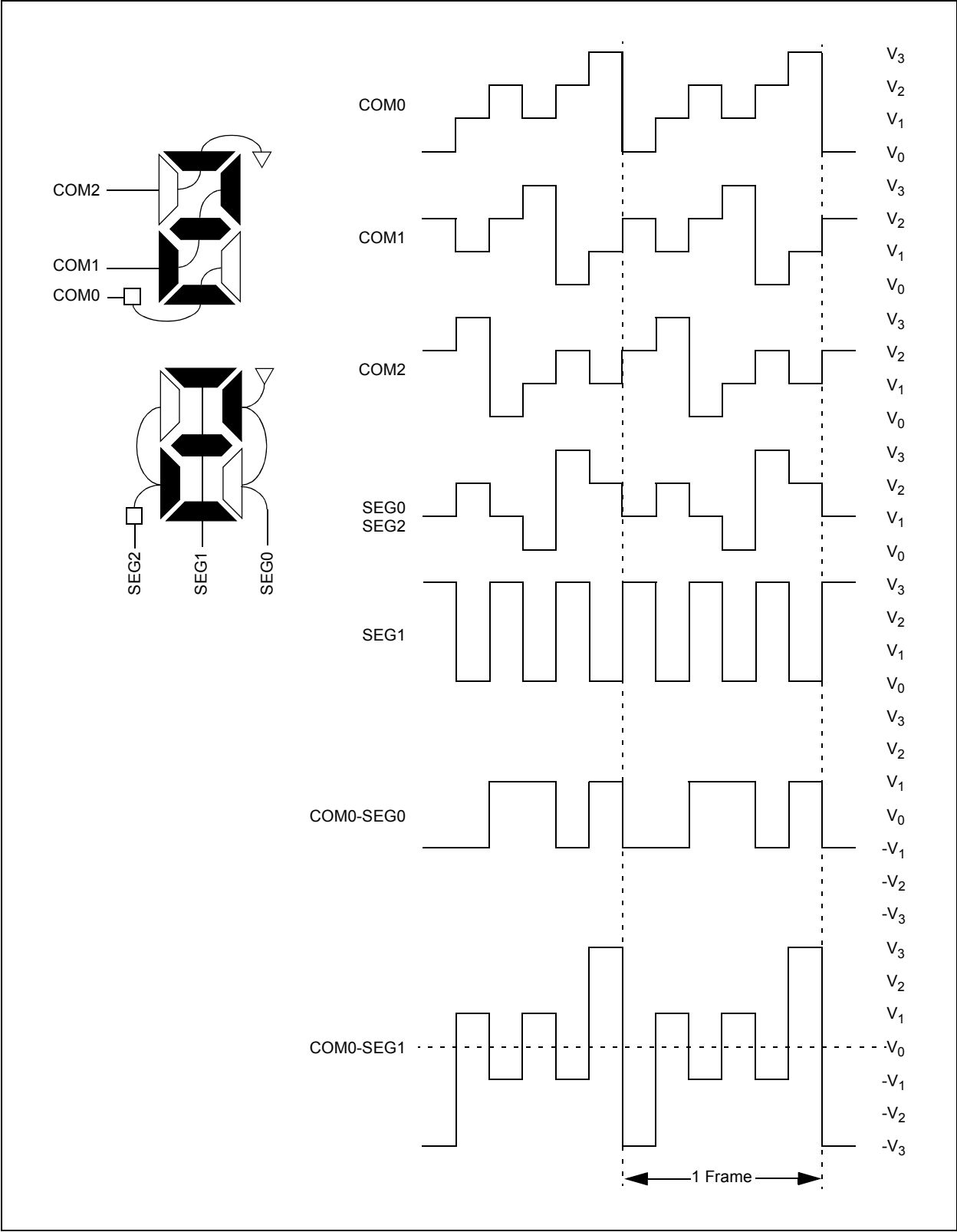


Figure 52-17: Type-B Waveforms in 1/3 MUX, 1/3 Bias Drive

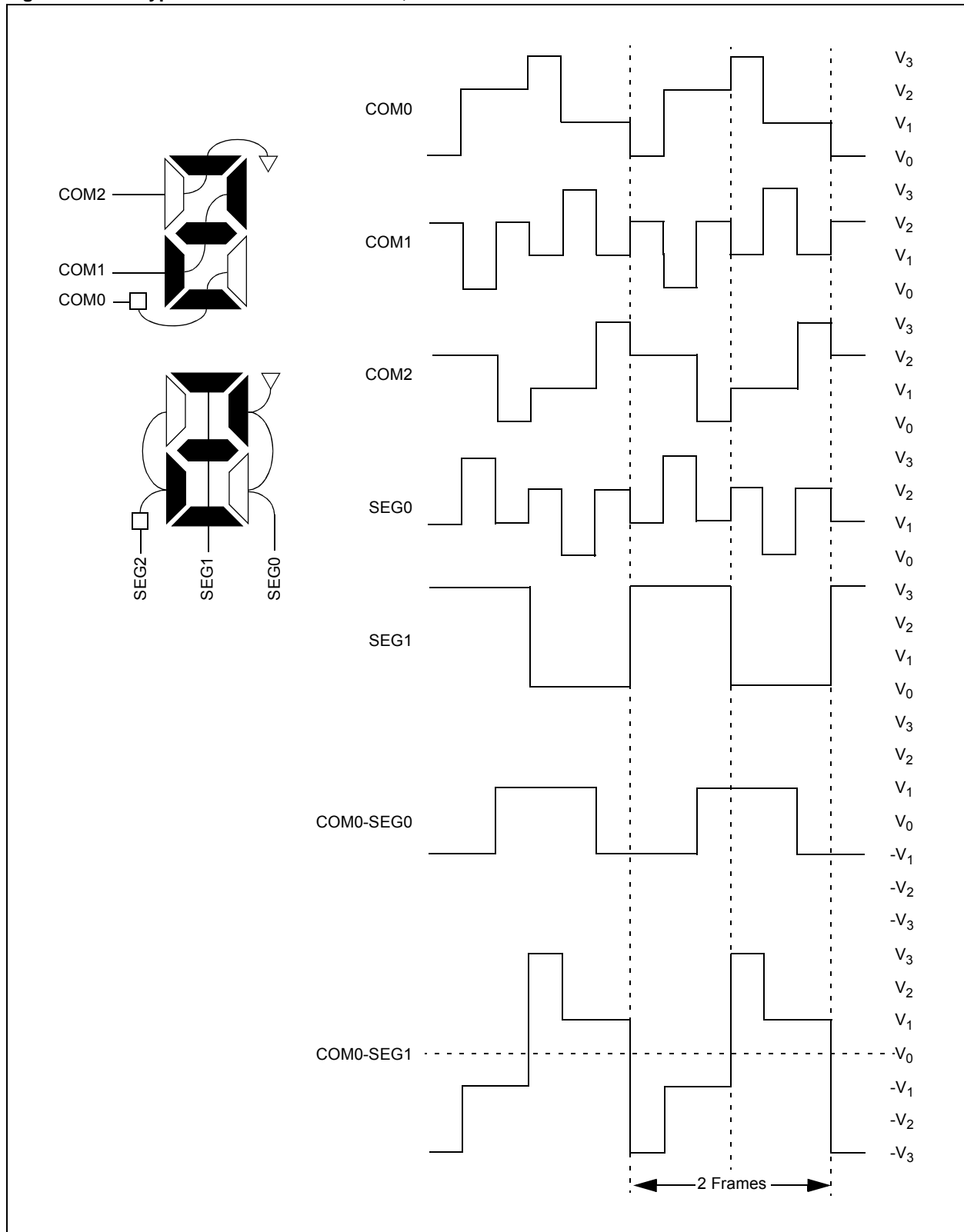


Figure 52-18: Type-A Waveforms in 1/4 MUX, 1/3 Bias Drive

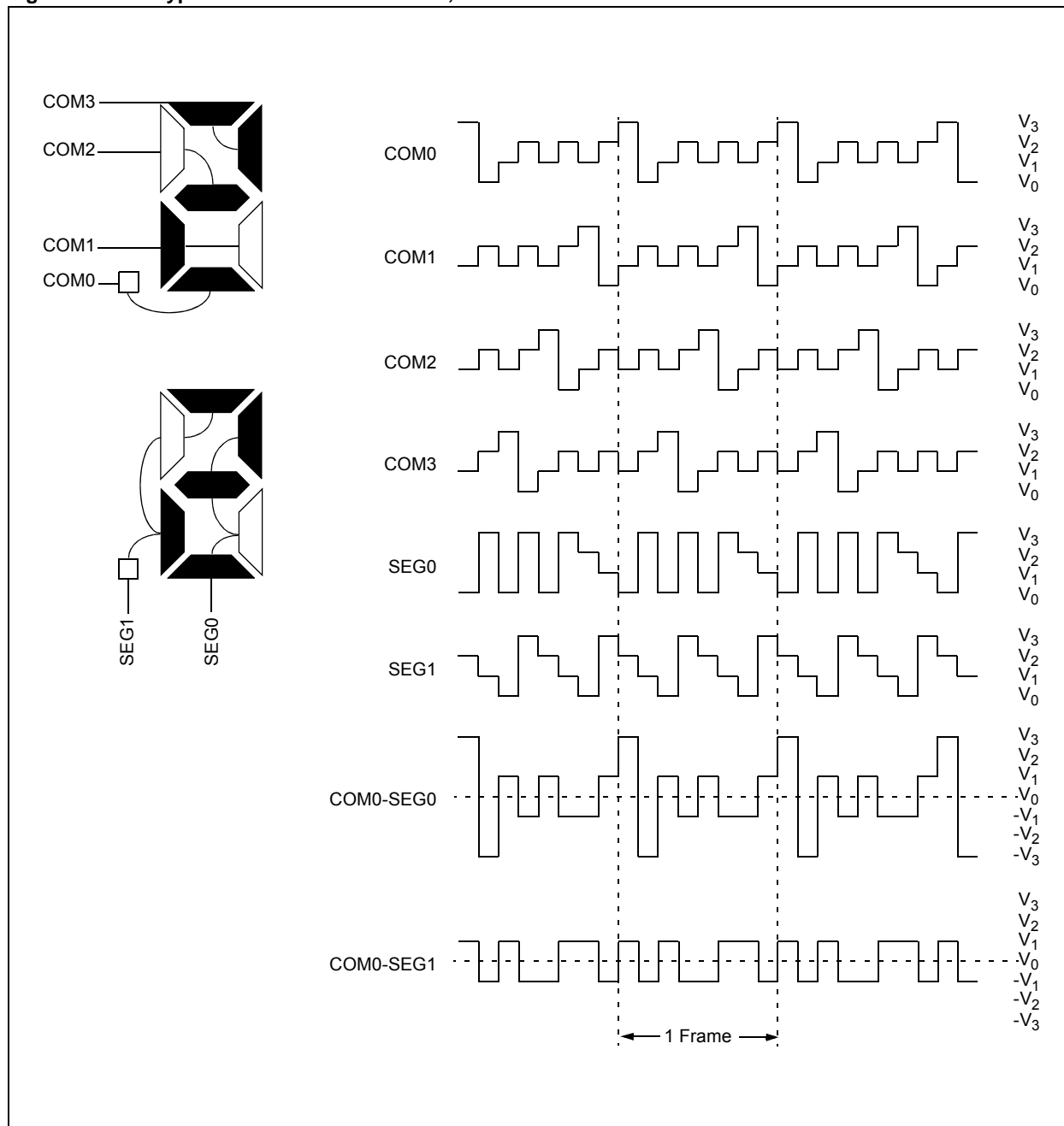


Figure 52-19: Type-B Waveforms in 1/4 MUX, 1/3 Bias Drive

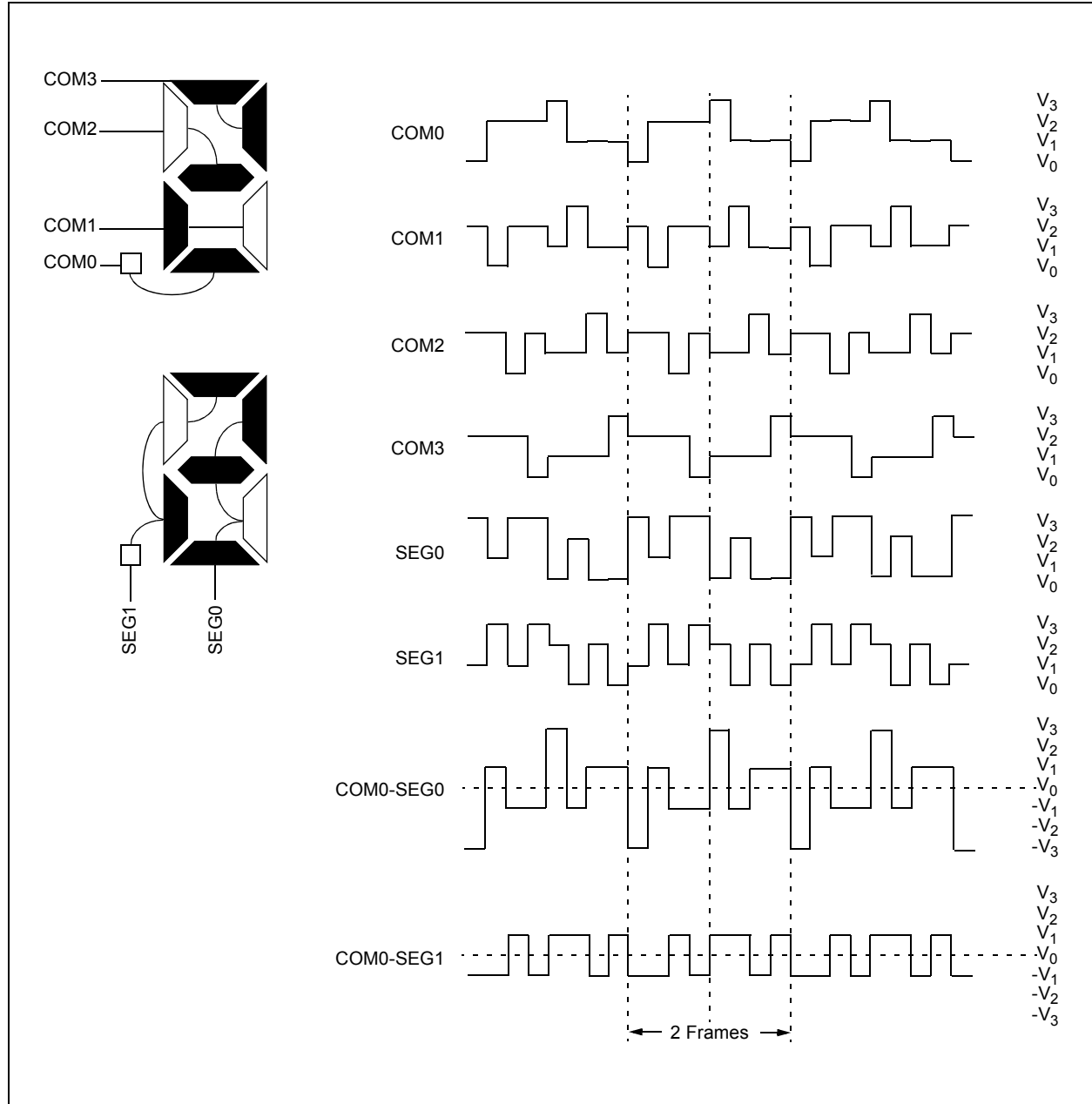


Figure 52-20: Type-A Waveforms in 1/8 MUX, 1/3 Bias Drive

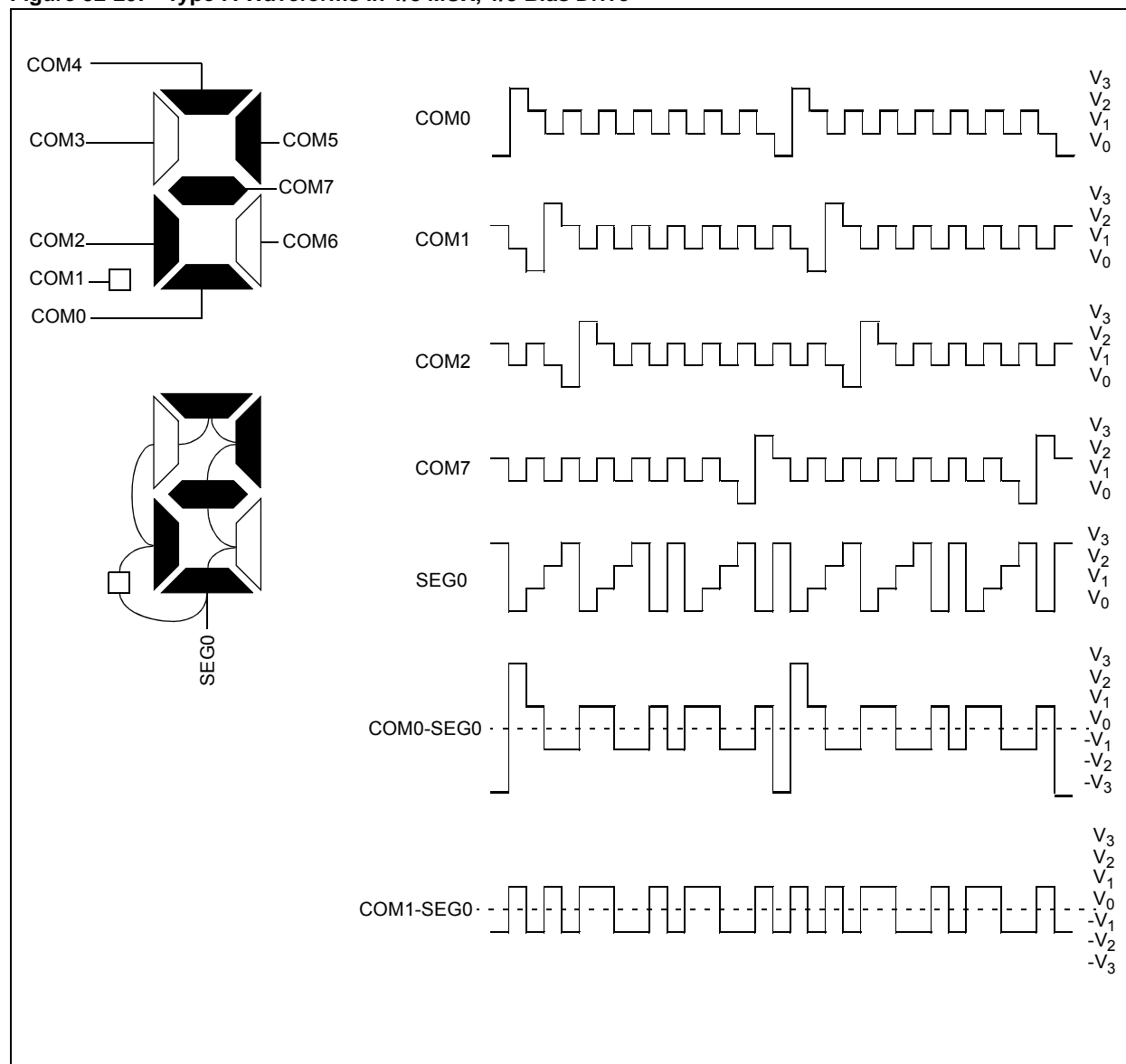
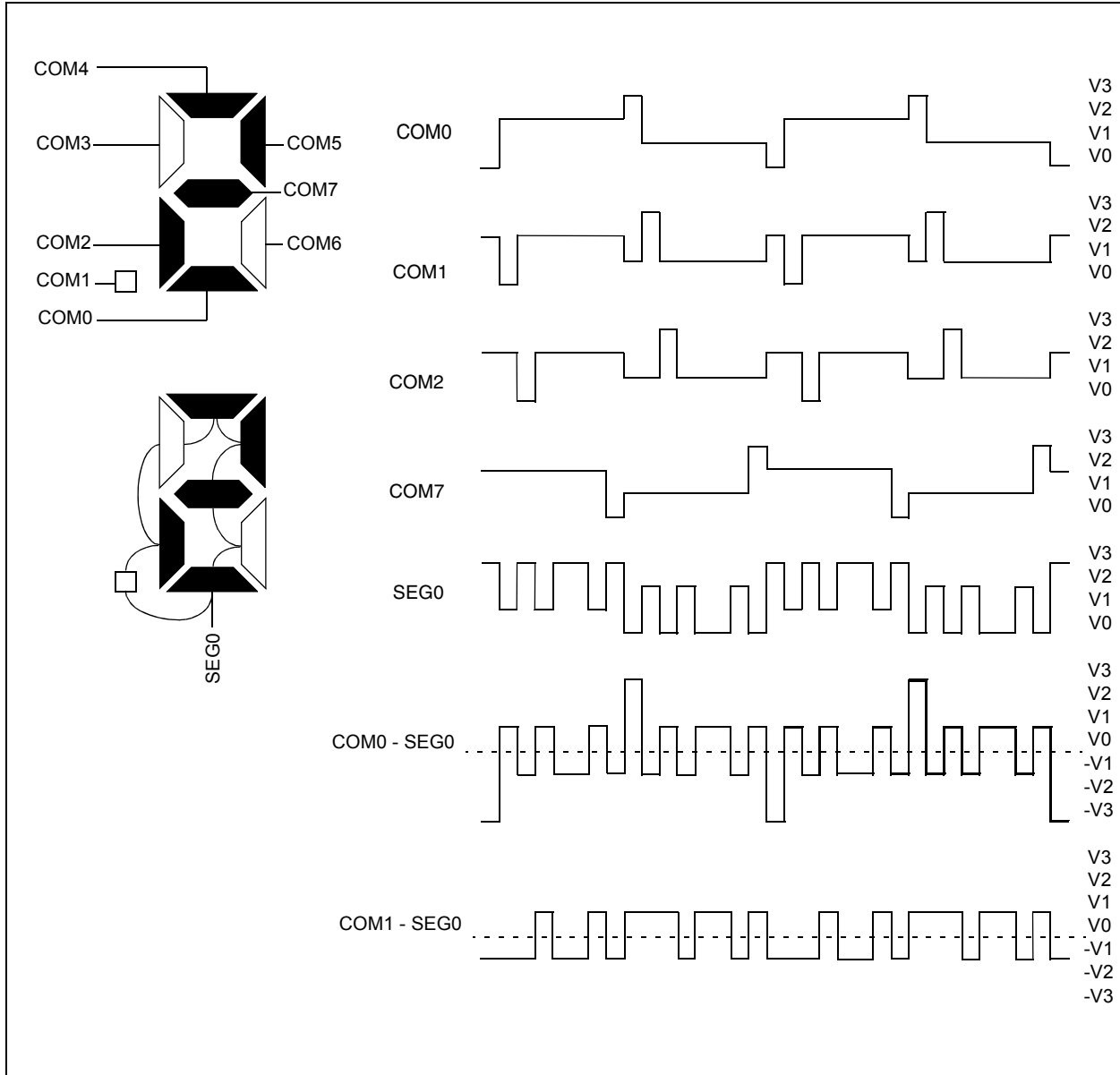


Figure 52-21: Type-B Waveforms in 1/8 MUX, 1/3 Bias Drive



52.11 LCD INTERRUPTS

The LCD timing generation provides an interrupt that defines the LCD frame timing. This interrupt can be used to coordinate the writing of the pixel data with the start of a new frame, which produces a visually crisp transition of the image.

This interrupt can also be used to synchronize external events to the LCD. For example, the interface to an external segment driver can be synchronized for segment data updates to the LCD frame.

A new frame is defined as beginning at the leading edge of the COM0 common signal. The interrupt will be set immediately after the LCD controller completes accessing all pixel data required for a frame. This will occur at a fixed interval before the frame boundary (TFINT), as shown in Figure 52-22.

The LCD controller will begin to access data for the next frame, within the interval from the interrupt to when the controller begins accessing data after the interrupt (TFWR). New data must be written within TFWR, as this is when the LCD controller will begin to access the data for the next frame.

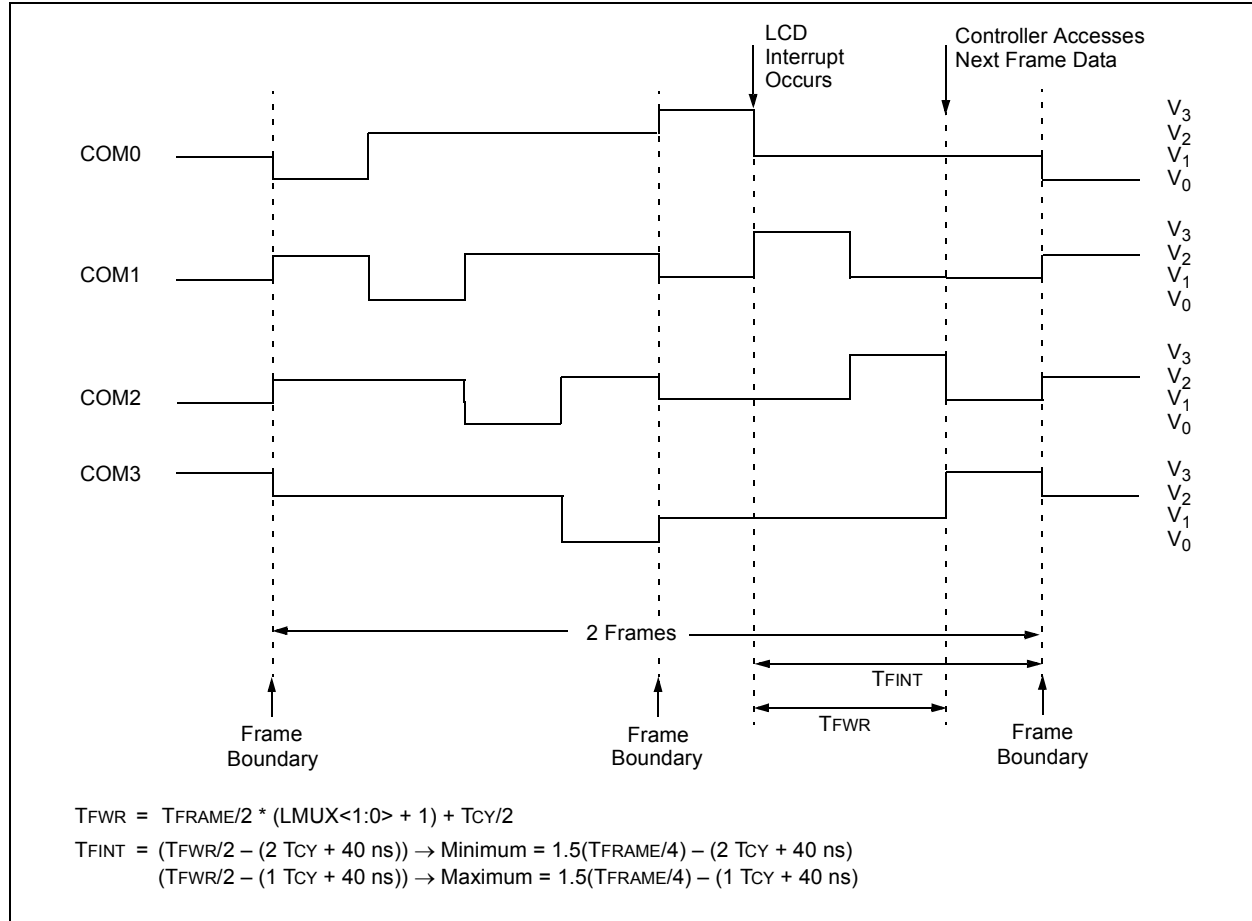
When the LCD driver is running with Type-B waveforms and the LMUX<1:0> bits are not equal to '00', there are some additional issues.

Since the DC voltage on the pixel takes two frames to maintain 0V, the pixel data must not change between subsequent frames. If the pixel data was allowed to change, the waveform for the odd frames would not necessarily be the complement of the waveform generated in the even frames, and a DC component would be introduced into the panel. Because of this, using Type-B waveforms requires synchronizing the LCD pixel updates to occur within a subframe after the frame interrupt.

To correctly sequence writing in Type-B, the interrupt only occurs on complete phase intervals. If the user attempts to write when the write is disabled, the WERR bit (LCDCON<5>) is set.

Note: The interrupt is not generated when the Type-A waveform is selected and when the Type-B with no multiplex (static) is selected.
--

Figure 52-22: Example Waveforms and Interrupt Timing in Quarter Duty Cycle Drive



52.12 CONFIGURING THE LCD MODULE

To configure the LCD module:

1. Select the frame clock prescale, using bits, LP<3:0> (LCDPS<3:0>).
2. Configure the appropriate pins to function as segment drivers using the LCDSEx registers.
3. If using the internal reference resistors for biasing, enable the internal reference ladder and:
 - define the Mode A and Mode B interval by using the LRLAT<2:0> bits (LCDREF<2:0>)
 - define the low, medium or high ladder for Mode A and Mode B by using the LRLAP<1:0> bits (LCDREF<7:6>) and the LRLBP<1:0> bits (LCDREF<5:4>), respectively
 - set the VLCDxPE bits and enable the LCDIRE bit (LCDREF<15>)
4. Configure the following LCD module functions using the LCDCON register:
 - Multiplex and Bias mode – LMUX<1:0> bits
 - Timing Source – CS<1:0> bits
 - Sleep mode – SLPEN bit
5. Write initial values to the pixel data registers, LCDDATA0 through LCDDATA31.
6. Clear the LCD Interrupt Flag, LCDIF, and if desired, enable the interrupt by setting bit, LCDIE.
7. Enable the LCD module by setting bit, LCDEN (LCDCON<15>)

52.13 OPERATION DURING SLEEP

The LCD module can operate during Sleep. The selection is controlled by the SLPEN bit (LCDCON<6>). Setting the SLPEN bit allows the LCD module to go to Sleep. Clearing the SLPEN bit allows the module to continue to operate during Sleep.

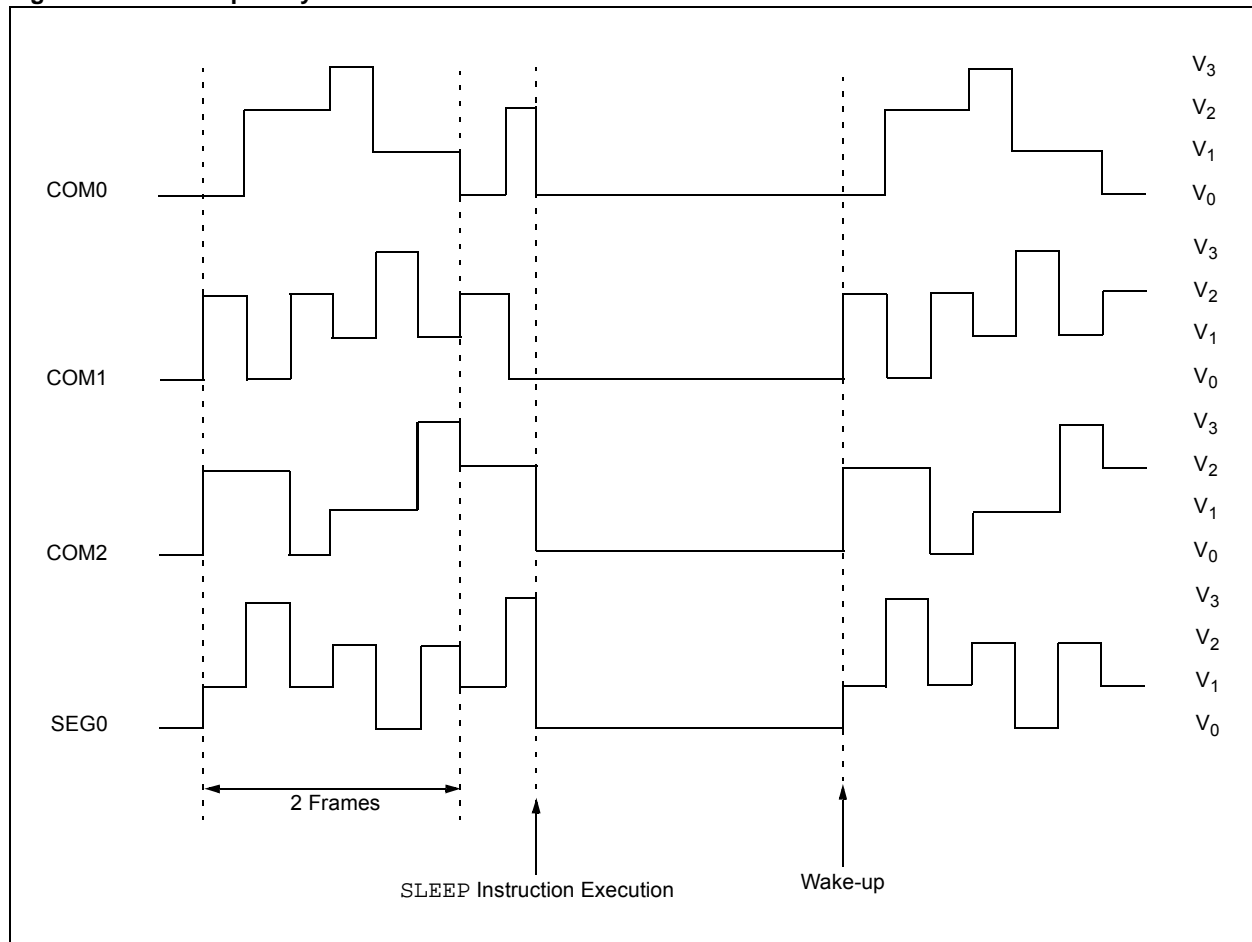
If a **SLEEP** instruction is executed and SLPEN = 1, the LCD module will cease all functions and go into a very low-current consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 52-23 shows this operation.

The LCD module current consumption will not decrease in this mode, but the overall consumption of the device will be lower due to shutdown of the core and other peripheral functions.

To ensure that no DC component is introduced on the panel, the **SLEEP** instruction should be executed immediately after a LCD frame boundary. The LCD interrupt can be used to determine the frame boundary. See **Section 52.11 "LCD Interrupts"** for the formulas to calculate the delay.

If a **SLEEP** instruction is executed and SLPEN = 0, the module will continue to display the current contents of the LCDDATA registers. The LCD data cannot be changed.

Figure 52-23: Sleep Entry/Exit when SLPEN = 1 or CS<1:0> = 00



52.14 REGISTERS

Table 52-6: Special Function Registers Associated with LCD Driver Module

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCON	LCDEN	—	LCDSIDL	—	—	—	—	—	—	SLPEN	WERR	CS1	CS0	LMUX2	LMUX1	LMUX0
LCDPS	—	—	—	—	—	—	—	—	WFT	BIASMD	LCDA	WA	r	LP2	LP1	LP0
LCDREF	LCDIRE	—	LCDCST2	LCDCST1	LCDCST0	VLCD3PE	VLCD2PE	VLCD1PE	LRLAP1	LRLAP0	LRLBP1	LRLBP0	—	LRLAT2	LRLAT1	LRLAT0
LCDREG	CPEN	—	—	—	—	—	—	—	—	—	BIAS2	BIAS1	BIAS0	MODE13	CKSEL1	CKSEL0
LCDSEx	LCD Segment Pin Enable Registers															
LCDDATAx	LCD Data Registers															
IFS6	—	—	—	—	—	—	—	—	—	—	—	LCDIF	—	—	—	—
IEC6	—	—	—	—	—	—	—	—	—	—	—	LCDIE	—	—	—	—
IPC25	—	—	—	—	—	—	—	—	—	—	—	—	—	LCDIP2	LCDIP1	LCDIP0

Legend: r = Reserved bit

52.15 REVISION HISTORY

Revision A (December 2010)

This is the initial released revision of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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