
Section 47. Motor Control PWM

HIGHLIGHTS

This section of the manual contains the following topics:

47.1	Introduction	47-2
47.2	Features of the MCPWM Module.....	47-2
47.3	Register Descriptions	47-3
47.4	Special Function Registers	47-5
47.5	MCPWM Module Architecture Overview.....	47-18
47.6	MCPWM Module Operating Modes	47-20
47.7	PWM Clock Control.....	47-21
47.8	Time Base Interrupts.....	47-24
47.9	PWM Output Modes.....	47-25
47.10	Duty Cycle Register Buffering.....	47-29
47.11	PWM Duty Cycle Resolution.....	47-31
47.12	PWM Dead-Time Control.....	47-33
47.13	PWM Fault Handling.....	47-37
47.14	Special Features of the MCPWM Module	47-40
47.15	Operation in Power-Saving Modes	47-45
47.16	Register Map.....	47-46
47.17	Related Application Notes.....	47-47
47.18	Revision History	47-48

47.1 INTRODUCTION

This section describes the Motor Control PWM (MCPWM) module in the PIC24F family of devices.

47.1.1 Purpose of the MCPWM Module

The MCPWM module is used to generate a periodic pulse waveform, which is useful in motor and power control applications. The MCPWM module acts as a timer to count up to a period count value. The time period and the duty cycle of the pulses are both programmable.

47.2 FEATURES OF THE MCPWM MODULE

The MCPWM module is used to generate multiple synchronized pulse-width modulated outputs. The following motor and power control applications are supported by the MCPWM module:

- Three-Phase AC Induction Motor (ACIM)
- Switched Reluctance Motor
- Brushless DC (BLDC) Motor
- Uninterruptible Power Supply (UPS)
- Independent Power Factor Correction (PFC) in a motor system
- Induction cooking systems
- DC motor control systems
- Single-phase inverter control
- Single-phase ACIM control

The distinctive features of the MCPWM module are summarized below:

- Up to six PWM outputs with four duty cycle generators
- Dedicated time base that supports $T_{CY}/2$ PWM edge resolution
- On-the-fly PWM frequency changes
- Hardware dead-time generators
- Output pin polarity programmed by device Configuration bits
- Multiple operating and output modes:
 - Single Event mode
 - Edge-Aligned mode
 - Center-Aligned mode
 - Center-Aligned mode with double updates
 - Complementary Output mode
 - Independent Output mode
- Manual override register for PWM output pins
- Duty cycle updates that can be configured to be immediate or synchronized to the PWM
- Up to two hardware Fault input pins with programmable function
- Special Event Trigger for synchronizing analog-to-digital conversions
- Output pins associated with the PWM can be individually enabled

Note: Depending on the PIC24F device variant, there are different versions of the MCPWM module. Refer to the specific device data sheet for further details.

47.3 REGISTER DESCRIPTIONS

The following registers are used to control the operation of the MCPWM module:

- **PxTCON: PWM Time Base Control Register**
This register is used for the selection of the Time Base mode, time base input clock prescaler and time base output postscaler, and for enabling the time base timer.
- **PxTMR: PWM Time Base Register**
The time base count value and the time base count direction status are obtained in this register.
- **PxTPER: PWM Time Base Period Register**
The PWM time base value is written into this register, which determines the PWM operating frequency.
- **PxSECMP: Special Event Compare Register**
This register provides the compare value at which the analog-to-digital conversions are to be synchronized with the PWM time base. Comparison can be either during up-count or down-count in Center-Aligned mode depending on the setting of the SEVTDIR bit in this register.
- **PWMxCON: PWM Control Register 1**
Selection of either Independent or Complementary mode for each PWM I/O pair is performed in this register.
- **PWMxCON2: PWM Control Register 2**
This register provides the following selections:
 - Selection of a PWM Special Event Trigger output postscaler value
 - Immediate updating of duty cycle registers
 - Selection of output override synchronization with the time base
 - Enabling updates from duty cycle and period buffer registers
- **PxDTCN1: Dead-Time Control Register 1**
The dead-time value and clock period prescaler for Dead Time Unit A and Dead Time Unit B can be selected using this register.
- **PxDTCN2: Dead-Time Control Register 2**
Dead-time insertions from Dead Time Unit A or Dead Time Unit B for each of the PWM outputs can be selected using this register.
- **PxFLTACON: Fault A Control Register(1)**
This register provides the following selections:
 - PWM output pin driven on an external Fault – active or inactive state
 - Fault mode – Cycle-by-Cycle mode or Latched mode
 - Pin pair to be controlled or not controlled by Fault Input A
- **PxFLTBCON: Fault B Control Register(1)**
This register provides the following selections:
 - PWM output pin driven on an external Fault – active or inactive state
 - Fault mode – Cycle-by-Cycle mode or Latched mode
 - Pin pair to be controlled or not controlled by Fault Input B
- **PxOVDCON: Override Control Register**
This register is used for enabling the output override feature and for PWM output pin control selection.
- **PxDC1: PWM Duty Cycle Register 1**
The 16-bit PWM duty cycle value for the PWM Output Pair 1 is written into this register.
- **PxDC2: PWM Duty Cycle Register 2**
The 16-bit PWM duty cycle value for the PWM Output Pair 2 is written into this register.

- **PxDC3: PWM Duty Cycle Register 3**

The 16-bit PWM duty cycle value for the PWM Output Pair 3 is written into this register.

- **PWMKEY: PWM Unlock Register**

This register enables the user to unlock the PWMxCON1, PxFLTACON and PxFLTBCON registers for write access.

- **FPOR: POR Device Configuration Register**

In addition to the Special Function Registers (SFRs) associated with the MCPWM module, three device Configuration bits can be used to set up the initial reset states and polarity of the PWM I/O pins. These Configuration bits are located in the FPOR register.

- **FOSCSEL: Oscillator Source Selection Register**

In addition to the Special Function Registers (SFRs) associated with the MCPWM module, one device Configuration bit in this register can be used to set up the write-protect feature of the PWM Configuration registers.

47.4 SPECIAL FUNCTION REGISTERS

Register 47-1: PxTCON: PWM Time Base Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
PTEN	—	PTSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTOPS3	PTOPS2	PTOPS1	PTOPS0	PTCKPS1	PTCKPS0	PTMOD1	PTMOD0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **PTEN:** PWM Time Base Timer Enable bit

1 = PWM time base is on

0 = PWM time base is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit

1 = PWM time base halts in CPU Idle mode

0 = PWM time base runs in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7-4 **PTOPS<3:0>:** PWM Time Base Output Postscale Select bits

1111 = 1:16 postscale

•

•

•

0001 = 1:2 postscale

0000 = 1:1 postscale

bit 3-2 **PTCKPS<1:0>:** PWM Time Base Input Clock Prescale Select bits

11 = PWM time base input clock period is 64 Tcy (1:64 prescale)

10 = PWM time base input clock period is 16 Tcy (1:16 prescale)

01 = PWM time base input clock period is 4 Tcy (1:4 prescale)

00 = PWM time base input clock period is Tcy (1:1 prescale)

bit 1-0 **PTMOD<1:0>:** PWM Time Base Mode Select bits

11 = PWM time base operates in a Continuous Up/Down mode with interrupts for double PWM updates

10 = PWM time base operates in a Continuous Up/Down Counting mode

01 = PWM time base operates in Single Event mode

00 = PWM time base operates in Free-Running mode

PIC24F Family Reference Manual

Register 47-2: PxTMR: PWM Time Base Register

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTDIR	PTMR14	PTMR13	PTMR12	PTMR11	PTMR10	PTMR9	PTMR8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTMR7	PTMR6	PTMR5	PTMR4	PTMR3	PTMR2	PTMR1	PTMR0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **PTDIR:** PWM Time Base Count Direction Status bit (read-only)

1 = PWM time base is counting down

0 = PWM time base is counting up

bit 14-0 **PTMR<14:0>:** PWM Time Base Register Count Value bits

Register 47-3: PxTPER: PWM Time Base Period Register

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PTPER14	PTPER13	PTPER12	PTPER11	PTPER10	PTPER9	PTPER8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTPER7	PTPER6	PTPER5	PTPER4	PTPER3	PTPER2	PTPER1	PTPER0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **PTPER<14:0>:** PWM Time Base Period Value bits

Register 47-4: PxSECMP: Special Event Compare Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTDIR	SEVTCMP14	SEVTCMP13	SEVTCMP12	SEVTCMP11	SEVTCMP10	SEVTCMP9	SEVTCMP8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP7	SEVTCMP6	SEVTCMP5	SEVTCMP4	SEVTCMP3	SEVTCMP2	SEVTCMP1	SEVTCMP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **SEVTDIR:** Special Event Trigger Time Base Direction bit⁽¹⁾

1 = A Special Event Trigger will occur when the PWM time base is counting down

0 = A Special Event Trigger will occur when the PWM time base is counting up

bit 14-0 **SEVTCMP<14:0>:** Special Event Compare Value bits⁽²⁾

Note 1: SEVTDIR is compared with PTDIR (PxTMR<15>) to generate the Special Event Trigger.

2: SEVTCMP<14:0> bits are compared with PxTMR<14:0> to generate the Special Event Trigger.

PIC24F Family Reference Manual

Register 47-5: PWMxCON1: PWM Control Register 1⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PMOD3	PMOD2	PMOD1
bit 15						bit 8	

U-0	R/W-x ⁽²⁾	R/W-x ⁽²⁾	R/W-x ⁽²⁾	U-0	R/W-x ⁽²⁾	R/W-x ⁽²⁾	R/W-x ⁽²⁾
—	PEN3H	PEN2H	PEN1H	—	PEN3L	PEN2L	PEN1L
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PMOD3:** PWM I/O Pair 3 Mode bit

1 = PWM I/O pin pair is in the Independent Output mode

0 = PWM I/O pin pair is in the Complementary Output mode

bit 9 **PMOD2:** PWM I/O Pair 2 Mode bit

1 = PWM I/O pin pair is in the Independent Output mode

0 = PWM I/O pin pair is in the Complementary Output mode

bit 8 **PMOD1:** PWM I/O Pair 1 Mode bit

1 = PWM I/O pin pair is in the Independent Output mode

0 = PWM I/O pin pair is in the Complementary Output mode

bit 7 **Unimplemented:** Read as '0'

bit 6 **PEN3H:** PWMxH3 I/O Enable bit⁽²⁾

1 = PWMxH3 pin is enabled for PWM output

0 = PWMxH3 pin is disabled; I/O pin becomes general purpose I/O

bit 5 **PEN2H:** PWMxH2 I/O Enable bit⁽²⁾

1 = PWMxH2 pin is enabled for PWM output

0 = PWMxH2 pin is disabled; I/O pin becomes general purpose I/O

bit 4 **PEN1H:** PWMxH1 I/O Enable bit⁽²⁾

1 = PWMxH1 pin is enabled for PWM output

0 = PWMxH1 pin is disabled; I/O pin becomes general purpose I/O

bit 3 **Unimplemented:** Read as '0'

bit 2 **PEN3L:** PWMxL3 I/O Enable bit⁽²⁾

1 = PWMxL3 pin is enabled for PWM output

0 = PWMxL3 pin is disabled; I/O pin becomes general purpose I/O

bit 1 **PEN2L:** PWMxL2 I/O Enable bit⁽²⁾

1 = PWMxL2 pin is enabled for PWM output

0 = PWMxL2 pin is disabled; I/O pin becomes general purpose I/O

bit 0 **PEN1L:** PWMxL1 I/O Enable bit⁽²⁾

1 = PWMxL1 pin is enabled for PWM output

0 = PWMxL1 pin is disabled; I/O pin becomes general purpose I/O

Note 1: In devices where the PWMLOCK bit is present in the FOSCSEL Configuration register, this register can be write-protected. If the PWMLOCK input signal is asserted (PWMLOCK = 1), the PWMxCON1 register is writable only after the proper sequence is written to the PWMKEY register. If the PWMLOCK input signal is deasserted (PWMLOCK = 0), the PWMxCON1 register is writable at all times. Refer to **Section 47.14.4 "Write-Protected Registers"** for further details about the unlock sequence.

2: The Reset condition of the PEN3H:PEN1H and PEN3L:PEN1L bits depend on the value of the PWMPIN device Configuration bit in the FPOR Configuration register. When PWMPIN is set to '0', Reset values are '1' and when PWMPIN is set to '1', Reset values are '0'.

Section 47. Motor Control PWM

Register 47-6: PWMxCON2: PWM Control Register 2

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SEVOPS3	SEVOPS2	SEVOPS1	SEVOPS0
bit 15				bit 8			

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IUE	OSYNC	UDIS
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SEVOPS<3:0>:** PWM Special Event Trigger Output Postscale Select bits

1111 = 1:16 postscale

•
•
•

0001 = 1:2 postscale

0000 = 1:1 postscale

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **IUE:** Immediate Update Enable bit

1 = Updates to the active PxDC3:PxDC1 registers are immediate

0 = Updates to the active PxDC3:PxDC1 registers are synchronized to the PWM time base

bit 1 **OSYNC:** Output Override Synchronization bit

1 = Output overrides via the PxOVDCON register are synchronized to the PWM time base

0 = Output overrides via the PxOVDCON register occur on the next Tcy boundary

bit 0 **UDIS:** PWM Update Disable bit

1 = Updates from duty cycle and period buffer registers are disabled

0 = Updates from duty cycle and period buffer registers are enabled

47

**Motor Control
PWM**

PIC24F Family Reference Manual

Register 47-7: PxDTCON1: Dead-Time Control Register 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTBPS1	DTBPS0	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTAPS1	DTAPS0	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **DTBPS<1:0>**: Dead Time Unit B Prescale Select bits

11 = Clock period for Dead Time Unit B is 8 T_{cy}

10 = Clock period for Dead Time Unit B is 4 T_{cy}

01 = Clock period for Dead Time Unit B is 2 T_{cy}

00 = Clock period for Dead Time Unit B is T_{cy}

bit 13-8 **DTB<5:0>**: Unsigned 6-Bit Dead-Time Value for Dead Time Unit B bits

bit 7-6 **DTAPS<1:0>**: Dead-Time Unit A Prescale Select bits

11 = Clock period for Dead Time Unit A is 8 T_{cy}

10 = Clock period for Dead Time Unit A is 4 T_{cy}

01 = Clock period for Dead Time Unit A is 2 T_{cy}

00 = Clock period for Dead Time Unit A is T_{cy}

bit 5-0 **DTA<5:0>**: Unsigned 6-Bit Dead-time Value for Dead Time Unit A bits

Section 47. Motor Control PWM

Register 47-8: PxDTCON2: Dead-Time Control Register 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **DTS3A:** Dead-Time Select for PWM I/O Pair 3 Signal Going Active bit

1 = Dead time provided from Unit B

0 = Dead time provided from Unit A

bit 4 **DTS3I:** Dead-Time Select for PWM I/O Pair 3 Signal Going Inactive bit

1 = Dead time provided from Unit B

0 = Dead time provided from Unit A

bit 3 **DTS2A:** Dead-Time Select for PWM I/O Pair 2 Signal Going Active bit

1 = Dead time provided from Unit B

0 = Dead time provided from Unit A

bit 2 **DTS2I:** Dead-Time Select for PWM I/O Pair 2 Signal Going Inactive bit

1 = Dead time provided from Unit B

0 = Dead time provided from Unit A

bit 1 **DTS1A:** Dead-Time Select for PWM I/O Pair 1 Signal Going Active bit

1 = Dead time provided from Unit B

0 = Dead time provided from Unit A

bit 0 **DTS1I:** Dead-Time Select for PWM I/O Pair 1 Signal Going Inactive bit

1 = Dead time provided from Unit B

0 = Dead time provided from Unit A

47

**Motor Control
PWM**

PIC24F Family Reference Manual

Register 47-9: PxFLTAcon: Fault A Control Register⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	R/W-x ⁽²⁾	R/W-x ⁽²⁾	R/W-x ⁽²⁾
FLTAM	—	—	—	—	FAEN3	FAEN2	FAEN1
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FAOV3H:FAOV1L:** Fault Input A PWM Override Value bits

1 = PWM output pin is driven active on an external Fault input event

0 = PWM output pin is driven inactive on an external Fault input event

bit 7 **FLTAM:** Fault A Mode bit

1 = Fault A input pin functions in Cycle-by-Cycle mode

0 = Fault A input pin latches all control pins to the programmed states in PxFLTACON<15:8>

bit 6-3 **Unimplemented:** Read as '0'

bit 2 **FAEN3:** Fault Input A Enable bit⁽²⁾

1 = PWMxH3/PWMxL3 pin pair is controlled by Fault Input A

0 = PWMxH3/PWMxL3 pin pair is not controlled by Fault Input A

bit 1 **FAEN2:** Fault Input A Enable bit⁽²⁾

1 = PWMxH2/PWMxL2 pin pair is controlled by Fault Input A

0 = PWMxH2/PWMxL2 pin pair is not controlled by Fault Input A

bit 0 **FAEN1:** Fault Input A Enable bit⁽²⁾

1 = PWMxH1/PWMxL1 pin pair is controlled by Fault Input A

0 = PWMxH1/PWMxL1 pin pair is not controlled by Fault Input A

Note 1: In devices where the PWMLOCK bit is present in the FOSCSEL Configuration register, this register can be write-protected. If the PWMLOCK input signal is asserted (PWMLOCK = 1), the PxFLTACON register is writable only after the proper sequence is written to the PWMKEY register. If the PWMLOCK input signal is deasserted (PWMLOCK = 0), the PxFLTACON register is writable at all times. Refer to **Section 47.14.4 “Write-Protected Registers”** for further details about the unlock sequence.

2: In devices where the PWMLOCK bit is present in the FOSCSEL Configuration register, the Reset value for this bit is '1' when PWMLOCK is set to '1'. In all other configurations, the Reset value for this bit is '0'. Refer to the specific device data sheet for further details.

Register 47-10: PxFLTBCON: Fault B Control Register⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	R/W-x ⁽²⁾	R/W-x ⁽²⁾	R/W-x ⁽²⁾
FLTBM	—	—	—	—	FBEN3	FBEN2	FBEN1
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FBOV3H:FBOV1L:** Fault Input B PWM Override Value bits

1 = PWM output pin is driven active on an external Fault input event

0 = PWM output pin is driven inactive on an external Fault input event

bit 7 **FLTBM:** Fault B Mode bit

1 = Fault B input pin functions in Cycle-by-Cycle mode

0 = Fault B input pin latches all control pins to the programmed states in PxFLTBCON<15:8>

bit 6-3 **Unimplemented:** Read as '0'

bit 2 **FBEN3:** Fault Input B Enable bit⁽²⁾

1 = PWMxH3/PWMxL3 pin pair is controlled by Fault Input B

0 = PWMxH3/PWMxL3 pin pair is not controlled by Fault Input B

bit 1 **FBEN2:** Fault Input B Enable bit⁽²⁾

1 = PWMxH2/PWMxL2 pin pair is controlled by Fault Input B

0 = PWMxH2/PWMxL2 pin pair is not controlled by Fault Input B

bit 0 **FBEN1:** Fault Input B Enable bit⁽²⁾

1 = PWMxH1/PWMxL1 pin pair is controlled by Fault Input B

0 = PWMxH1/PWMxL1 pin pair is not controlled by Fault Input B

Note 1: In devices where the PWMLOCK bit is present in the FOSCSEL Configuration register, this register can be write-protected. If the PWMLOCK input signal is asserted (PWMLOCK = 1), the PxFLTBCON register is writable only after the proper sequence is written to the PWMKEY register. If the PWMLOCK input signal is deasserted (PWMLOCK = 0), the PxFLTBCON register is writable at all times. Refer to **Section 47.14.4 “Write-Protected Registers”** for further details about the unlock sequence.

2: In devices where the PWMLOCK bit is present in the FOSCSEL Configuration register, the Reset value for this bits is '1'. Refer to the specific device data sheet for further details.

PIC24F Family Reference Manual

Register 47-11: PxOVDCON: Override Control Register

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **POVD3H:POVD1L:** PWM Output Override bits

1 = Output on PWMxH3:PWMxH1/PWMxL3:PWMxL1 I/O pin pair is controlled by the PWM generator

0 = Output on PWMxH3:PWMxH1/PWMxL3:PWMxL1 I/O pin pair is driven, controlled by the value in the corresponding POUT3H:POUT1H/POUT3L:POUT1L bit

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **POUT3H:POUT1L:** PWM Manual Output bits

1 = PWMxH3:PWMxH1/PWMxL3:PWMxL1 I/O pin pair is driven active when the corresponding POVD3H:POVD1H/POVD3L:POVD1L bit is cleared

0 = PWMxH3:PWMxH1/PWMxL3:PWMxL1 I/O pin pair is driven inactive when the corresponding POVD3H:POVD1H/POVD3L:POVD1L bit is cleared

Register 47-12: PxDC1: PWM Duty Cycle Register 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxDC115	PxDC114	PxDC113	PxDC112	PxDC111	PxDC110	PxDC19	PxDC18
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxDC17	PxDC16	PxDC15	PxDC14	PxDC13	PxDC12	PxDC11	PxDC10
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PxDC1<15:0>:** PWM Duty Cycle 1 Value bits

Section 47. Motor Control PWM

Register 47-13: PxDC2: PWM Duty Cycle Register 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxDC215	PxDC214	PxDC213	PxDC212	PxDC211	PxDC210	PxDC209	PxDC208
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxDC207	PxDC206	PxDC205	PxDC204	PxDC203	PxDC202	PxDC201	PxDC200
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PxDC2<15:0>**: PWM Duty Cycle 2 Value bits

Register 47-14: PxDC3: PWM Duty Cycle Register 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxDC315	PxDC314	PxDC313	PxDC312	PxDC311	PxDC310	PxDC309	PxDC308
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxDC307	PxDC306	PxDC305	PxDC304	PxDC303	PxDC302	PxDC301	PxDC300
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PxDC3<15:0>**: PWM Duty Cycle 3 Value bits

47

**Motor Control
PWM**

PIC24F Family Reference Manual

Register 47-15: PWMKEY: PWM Unlock Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMLOCK15	PWMLOCK14	PWMLOCK13	PWMLOCK12	PWMLOCK11	PWMLOCK10	PWMLOCK9	PWMLOCK8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMLOCK7	PWMLOCK6	PWMLOCK5	PWMLOCK4	PWMLOCK3	PWMLOCK2	PWMLOCK1	PWMLOCK0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PWMLOCK<15:0>**: PWM Unlock bits

If the PWMLOCK input signal is asserted (PWMLOCK = 1), the PWMxCON1, PxFLTAON and PxFLTBCON registers are writable only after the proper sequence is written to the PWMKEY register. If the PWMLOCK input signal is deasserted (PWMLOCK = 0), the PWMxCON1, PxFLTAON and PxFLTBCON registers are writable at all times. Refer to **Section 47.14.4 "Write-Protected Registers"** for further details about the unlock sequence.

Section 47. Motor Control PWM

Register 47-16: FPOR: POR Device Configuration Register

R-x	R-x	R-x	R-x	U-0	U-0	U-0	U-0
PWMPIN	HPOL	LPOL	ALTI2C	—	—	—	—
bit 7							bit0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

P = Programmable configuration bit

- bit 7 **PWMPIN:** Motor Control PWM Module Pin Mode bit
1 = PWM module pins controlled by the PORT register at device Reset (tri-stated)
0 = PWM module pins controlled by the PWM module at device Reset (configured as output pins)
- bit 6 **HPOL:** Motor Control PWM High-Side Polarity bit
1 = PWM module high-side output pins have active-high output polarity
0 = PWM module high-side output pins have active-low output polarity
- bit 5 **LPOL:** Motor Control PWM Low-Side Polarity bit
1 = PWM module low-side output pins have active-high output polarity
0 = PWM module low-side output pins have active-low output polarity
- bit 4 **ALTI2C:** Not used by the PWM module. Refer to the specific device data sheet for more information.
- bit 3-0 **Unimplemented:** Read as '0'

Register 47-17: FOSCSEL: Oscillator Source Selection Register

R-x	R-x	U-0	U-0	U-0	R-x	R-x	R-x
IESO	PWMLOCK	—	—	—	FNOSC2	FNOSC1	FNOSC0
bit 7							bit 0

Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **IESO:** Not used by the PWM module. Refer to the specific device data sheet for more information.
- bit 6 **PWMLOCK:** Motor Control PWM Unlock bit
1 = PWM module registers, PWMxCON1, PxFLTAON and PxFLTBCON, are write-protected
0 = PWM module registers are not write-protected
- bit 5-3 **Unimplemented:** Read as '0'
- bit 2-0 **FNOSC<2:0>:** Not used by the PWM module. Refer to the specific device data sheet for more information.

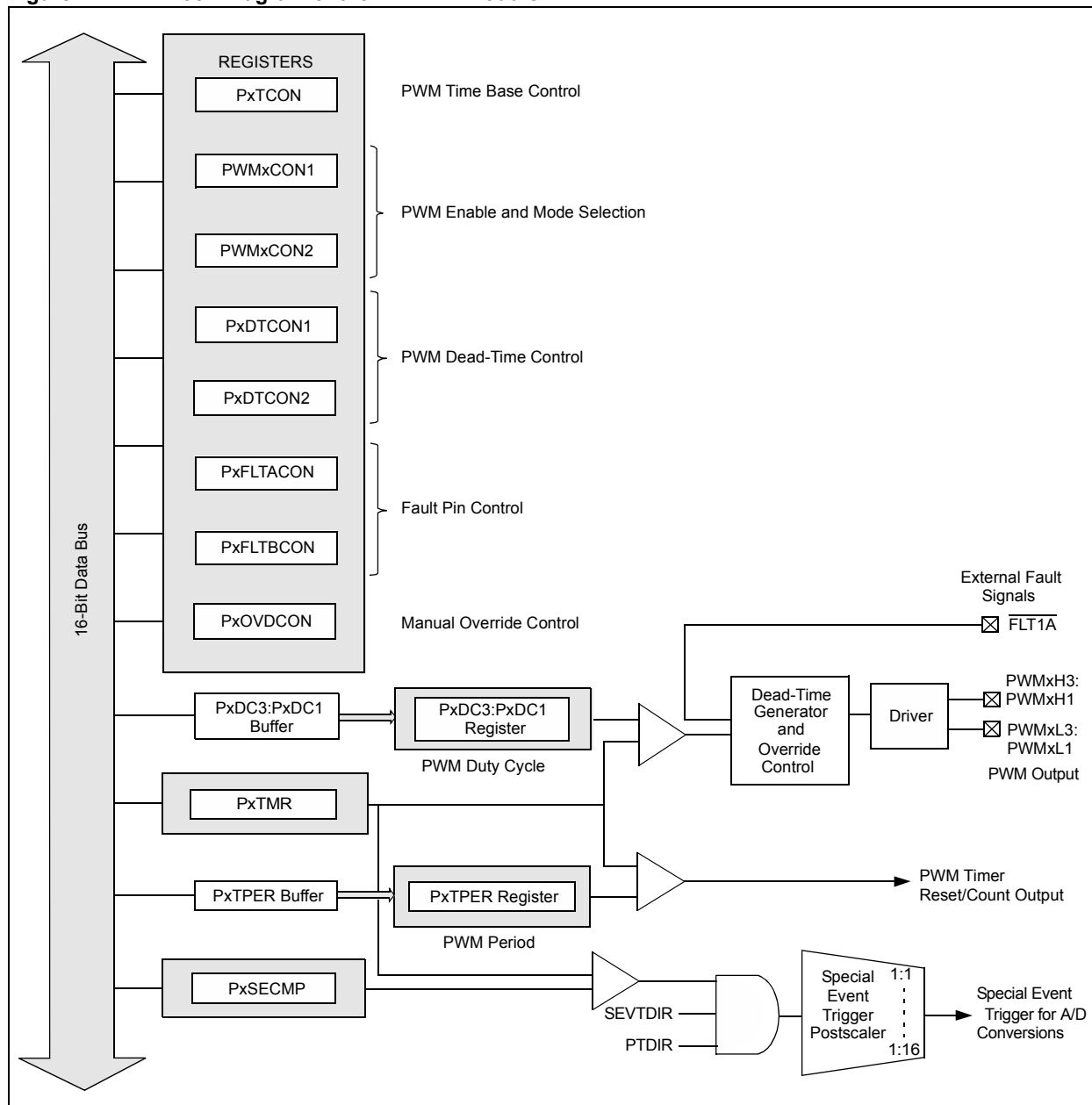
47

Motor Control
PWM

47.5 MCPWM MODULE ARCHITECTURE OVERVIEW

Figure 47-1 provides a block diagram of the MCPWM module for PIC24F devices.

Figure 47-1: Block Diagram of the MCPWM Module



47.5.1 Duty Cycle

The MCPWM module has up to three PWM generators. There are four Special Function Registers, PWM Duty Cycle (PxDC3:PxDC1), associated with the module to specify the duty cycle values for the PWM generators. The duty cycle gives the time for which the PWM pulses are active in a given PWM time period.

47.5.2 Dead-Time Generation

Dead-time generation is automatically enabled when any of the PWM I/O pin pairs are operating in the Complementary Output mode. As the power devices cannot switch instantaneously, some amount of time must be provided between the turn-off event of one PWM output in a complementary pair and the turn-on event of the other transistor.

There are two programmable dead-time values. To increase user application flexibility, these dead times can be used in either of the two methods described below:

- The PWM output signals can be optimized for different turn-off times in the high-side and low-side transistors. The first dead time is inserted between the turn-off event of the lower transistor of the complementary pair and the turn-on event of the upper transistor. The second dead time is inserted between the turn-off event of the upper transistor and the turn-on event of the lower transistor.
- The two dead times can be assigned to individual PWM I/O pairs. This operating mode allows the PWM module to drive different transistor/load combinations with each complementary PWM I/O pair.

There are up to two dead-time generation units (A and B) that can be configured in the Dead-Time Control (PxDTCON1 and PxDTCON2) registers.

47.5.3 Output Override Control

The PWM module output override feature allows the user application to manually drive the PWM I/O pins to specified logic states independent of the duty cycle comparison units. The PWM override bits are useful when controlling various types of electrically commutated motors.

The output override feature can be controlled using the PWM Output Override (POVD4H:POVD1L) bits in the Override Control (PxOVDCON<15:8>) register.

47.5.4 Special Event Trigger

The PWM module has a Special Event Trigger that allows analog-to-digital conversions to be synchronized to the PWM time base. The analog-to-digital sampling and conversion time may be programmed to occur at any point within the PWM period. The Special Event Compare (PxSECMP) register specifies the special event compare value for generating the Special Event Trigger to start analog-to-digital conversion.

Note: Detailed descriptions of the PWM timer, PWM time base period, output override feature and Special Event Trigger are provided in subsequent sections.

47.6 MCPWM MODULE OPERATING MODES

The MCPWM module can be configured for one of four modes of operation using the PWM Time Base Mode Select (PTMOD) control bits in the PWM Time Base Control (PxTCON<1:0>) register. The four operating modes are described in the following four sections.

47.6.1 Free-Running Mode (PTMOD<1:0> = 0b00)

In this mode, the PWM Time Base (PxTMR) register will count upward until the value in the PWM Time Base Period (PxTPER) register is matched. The PxTMR register is reset on the following input clock edge. The timer will continue counting upward and resetting as long as the PWM Time Base Timer Enable (PTEN) bit in the PWM Time Base Control (PxTCON<15>) register remains set.

47.6.2 Single Event Mode (PTMOD<1:0> = 0b01)

The PWM timer (PxTMR) will begin counting upward when the PTEN bit is set. When the PxTMR value matches the PxTPER register value, the PxTMR register is reset on the following input clock edge and the PTEN bit is cleared by the hardware to halt the timer.

47.6.3 Continuous Up/Down Count Mode (PTMOD<1:0> = 0b10)

In this mode, the PWM timer (PxTMR) will count upward until the value in the PxTPER register is matched. The timer will start counting downward on the following clock edge and continue counting down until it reaches zero. The PWM Time Base Count Direction Status (PTDIR) bit in the PWM Time Base (PxTMR<15>) register indicates the counting direction. This bit is set when the timer starts counting downward.

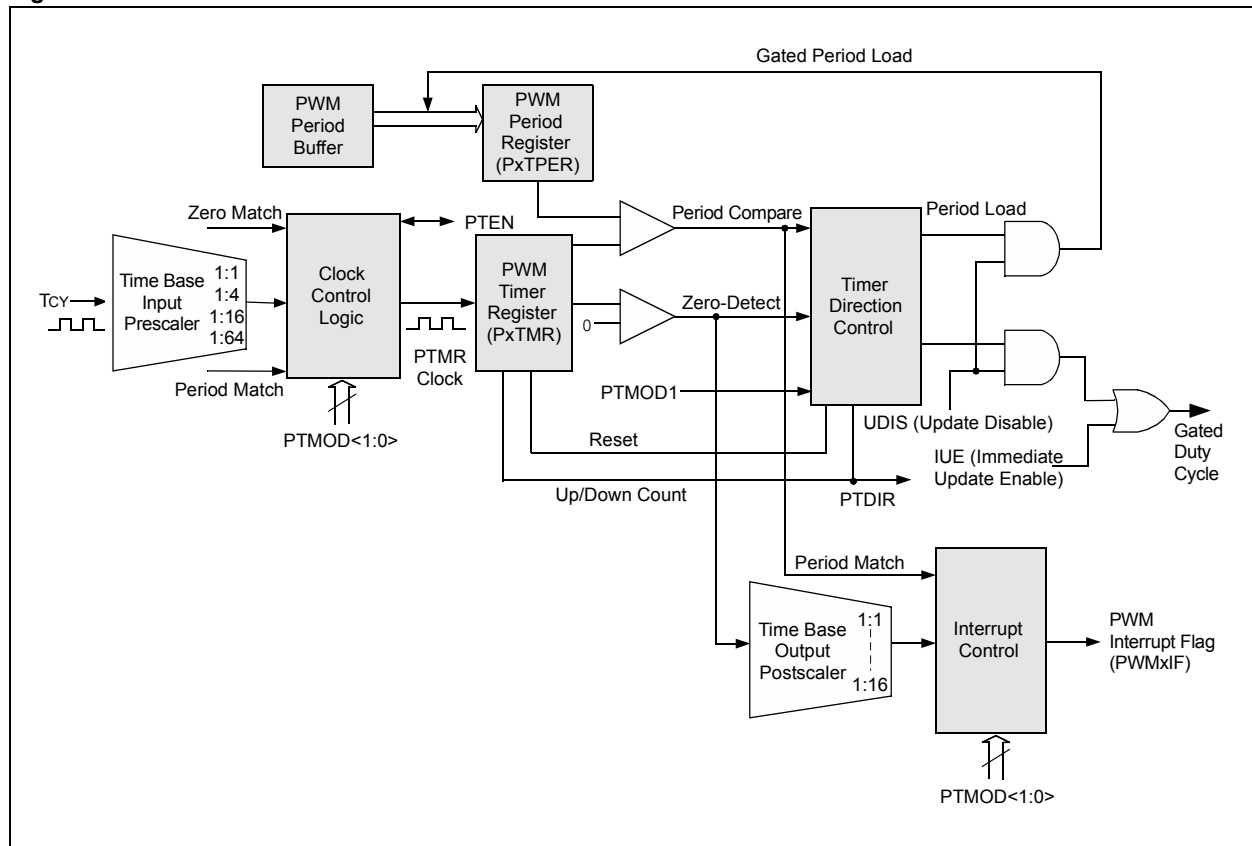
47.6.4 Continuous Up/Down Count Mode with Interrupts for Double Update of Duty Cycle (PTMOD<1:0> = 0b11)

This mode is similar to the Continuous Up/Down Count mode, with the exception that an interrupt event is generated twice per time base: once when the PxTMR register is equal to zero and a second time when a period match occurs.

47.7 PWM CLOCK CONTROL

The time base for the PWM pulses is provided by the 15-bit timer with prescale and postscale options, as shown in Figure 47-2.

Figure 47-2: PWM Clock Control



47.7.1 Time Base Input Prescaler

The input clock (T_{cy}) derived from the oscillator source can be prescaled to four possible options: 1:1, 1:4, 1:16 and 1:64. These options can be selected by using the PWM Time Base Input Clock Prescale Select (PTCKPS) bits of the PWM Time Base Control (PxTCON<3:2>) register. The prescaled clock is the input to the PWM clock control logic block.

47.7.2 Clock Control Logic and Time Base

This block determines the nature of the PWM timer output, depending on the time period match, zero match and PWM Time Base Mode Select (PTMOD) bits in the PWM Time Base Control (PxTCON<1:0>) register. The time base input prescaler counter is cleared when any of the following occurs:

- A write to the PxTMR register
- A write to the PxTCON register
- A device Reset

The PWM Time Base (PxTMR) register is not cleared when PxTCON is written.

The time base value of the PWM Time Base Register Count Value (PTMR) bit in the PWM Time Base (PxTMR<14:0>) register is compared with the contents of the PWM Time Base Period (PxTPER) register. If a match occurs, a period match signal is generated.

If the time base value of the PTMR bits of the PxTMR register is zero, a zero-detect signal is generated.

47.7.3 Timer Direction Control

The timer direction control block determines the count direction. The PWM Time Base Count Direction Status (PTDIR) bit in the PWM Time Base (PxTMR<15>) register is a read-only bit that gives the present direction of the count. If the PTDIR bit is cleared, PxTMR is counting upward, and if it is set, PxTMR is counting downward. The time base is enabled or disabled by setting or clearing the PWM Time Base Timer Enable (PTEN) bit in the PWM Time Base Control (PxTMR<15>) register. The PxTMR register is not cleared when the PTEN bit is cleared in software.

47.7.4 Time Base Output Postscaler

The time base output postscaler is used to optionally select one of several possible options (1:1 to 1:16, scaling inclusive) to postscale the timer output. The interrupt control logic decides when to set the PWM Interrupt Flag, PWMxIF, for generating a PWM interrupt, depending on the postscale value. The postscaler is useful when the PWM duty cycles need not be updated every PWM cycle.

The time base output postscaler counter is cleared when any of the following occurs:

- A write to the PxTMR register
- A write to the PxTCON register
- A device Reset

The PxTMR register is not cleared when the PxTCON register is written.

47.7.5 PWM Time Period

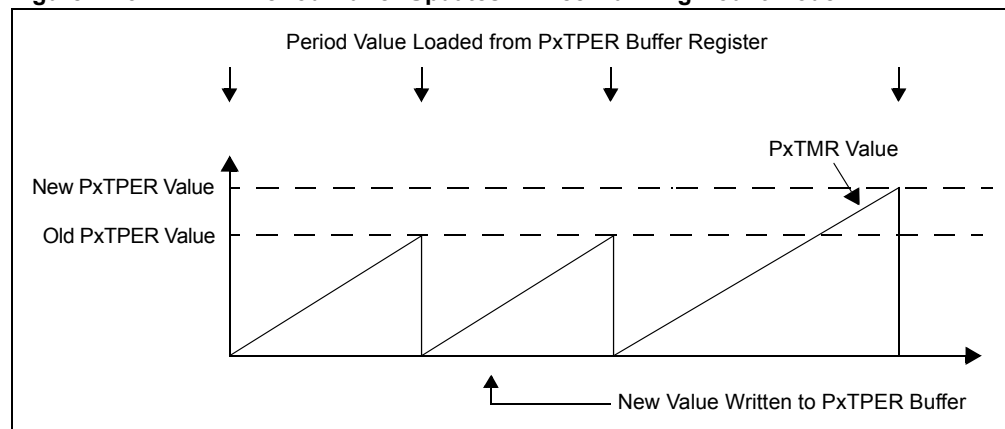
The PxTPER register determines the counting period for the PxTMR register. The user application must write a 15-bit value into the PWM Time Base Period Value (PxTPER) bits of the PWM Time Base (PxTMR<14:0>) register. When the value of PxTMR<14:0> matches the value of PxTPER<14:0>, the time base will either reset to zero or reverse the count direction on the next clock input edge. The action taken depends on the operating mode of the time base.

The time base period is double-buffered to allow run-time changes of the time period of the PWM signal without any glitches. The PxTPER register serves as a buffer to the actual register, which is not accessible by the user application. The PxTPER register contents are loaded into the actual Time Base Period register at the following times:

- Free-Running and Single Event modes: when the PxTMR register is reset to zero after a match with the PxTPER register.
- Up/Down Counting modes: when the PxTMR register is zero.

The value held in the PxTPER register is automatically loaded into the PWM Time Base Period (PxTPER) register when the PWM time base is disabled (PTEN = 0). Figure 47-3 and Figure 47-4 indicate the times when the contents of the PxTPER register are loaded into the Time Base Period register.

Figure 47-3: PWM Period Buffer Updates in Free-Running Count Mode



Equation 47-1 and Equation 47-2 show the formulas to determine the PWM period.

**Equation 47-1: PWM Period Calculation for Free-Running Count Mode
(PTMOD = 00 or 01)**

$$PITPER = \frac{FCY}{FPWM \times (PITMR \text{ Prescaler})} - 1$$

Example:

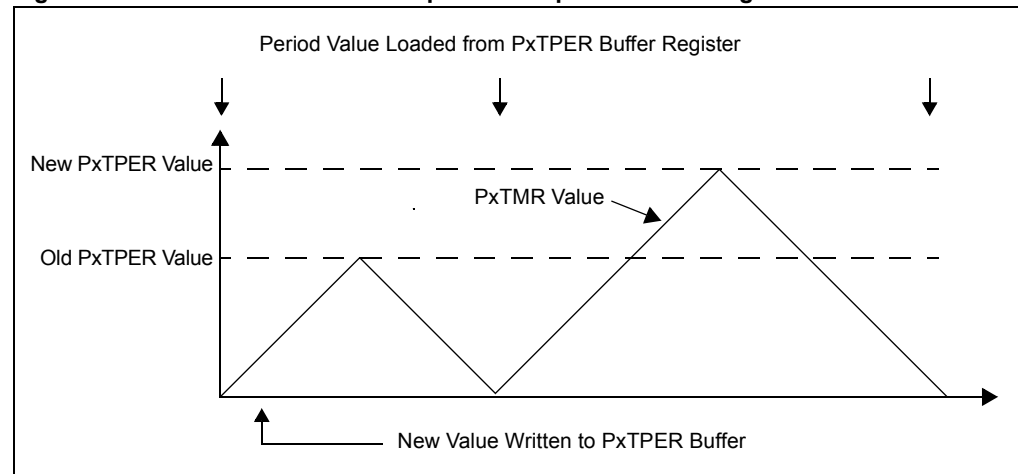
$FCY = 16 \text{ MHz}$

$FPWM = 20,000 \text{ Hz}$

$PITMR \text{ Prescaler} = 1:1$

$$\begin{aligned} PITPER &= \frac{16,000,000}{20,000 \times 1} - 1 \\ &= 800 - 1 \\ &= 799 \end{aligned}$$

Figure 47-4: PWM Period Buffer Updates in Up/Down Counting Modes



**Equation 47-2: PWM Period Calculation in Up/Down Counting Modes
(PTMOD = 10 or 11)**

$$PITPER = \frac{FCY}{FPWM \times (PITMR \text{ Prescaler}) \times 2} - 1$$

Example:

$FCY = 16 \text{ MHz}$

$FPWM = 20,000 \text{ Hz}$

$PITMR \text{ Prescaler} = 1:1$

$$\begin{aligned} PITPER &= \frac{16,000,000}{20,000 \times 1 \times 2} - 1 \\ &= 400 - 1 \\ &= 399 \end{aligned}$$

47.8 TIME BASE INTERRUPTS

The generation of PWM interrupts depends on the mode of operation selected by the PWM Time Base Mode Select (PTMOD) bits of the PWM Time Base Control (PxTCON<1:0>) register and the time base output postscaler selected using the PWM Time Base Output Postscale Select (PTOPS) bits of the PxTCON register (PxTCON<7:4>).

The interrupt generation for each of the operating modes is described in the following four sections.

47.8.1 Free-Running Mode

An interrupt event is generated when the PWM Time Base (PxTMR) register is reset to zero due to a match with the PWM Time Base Period (PxTPER) register. The postscaler selection bits can be used in Free-Running mode to reduce the frequency of the interrupt events.

47.8.2 Single Event Mode

An interrupt event is generated when the PxTMR register is reset to zero due to a match with the PxTPER register. The PWM Time Base Timer Enable (PTEN) bit of the PxTCON register (PxTCON<15>) is also cleared to inhibit further PxTMR increments. The postscaler selection bits have no effect in Single Event mode.

47.8.3 Up/Down Counting Mode

An interrupt event is generated each time the value of the PxTMR register is equal to zero and the PWM time base begins to count upward. The postscale selection can be used to reduce the frequency of interrupt events in Up/Down Counting mode.

47.8.4 Up/Down Counting Mode with Double Update of Duty Cycle

An interrupt event is generated each time the PxTMR register is equal to zero and each time a period match occurs. The postscale selection has no effect in Up/Down Counting mode with Double Update of Duty Cycle. This mode allows the control loop bandwidth to be doubled because the PWM duty cycles can be updated twice per period. Every rising and falling edge of the PWM signal can be controlled using the Double Update mode.

On generation of a PWM interrupt, the PWM Interrupt Flag, PWMIF, is set in the corresponding IFS register.

47.9 PWM OUTPUT MODES

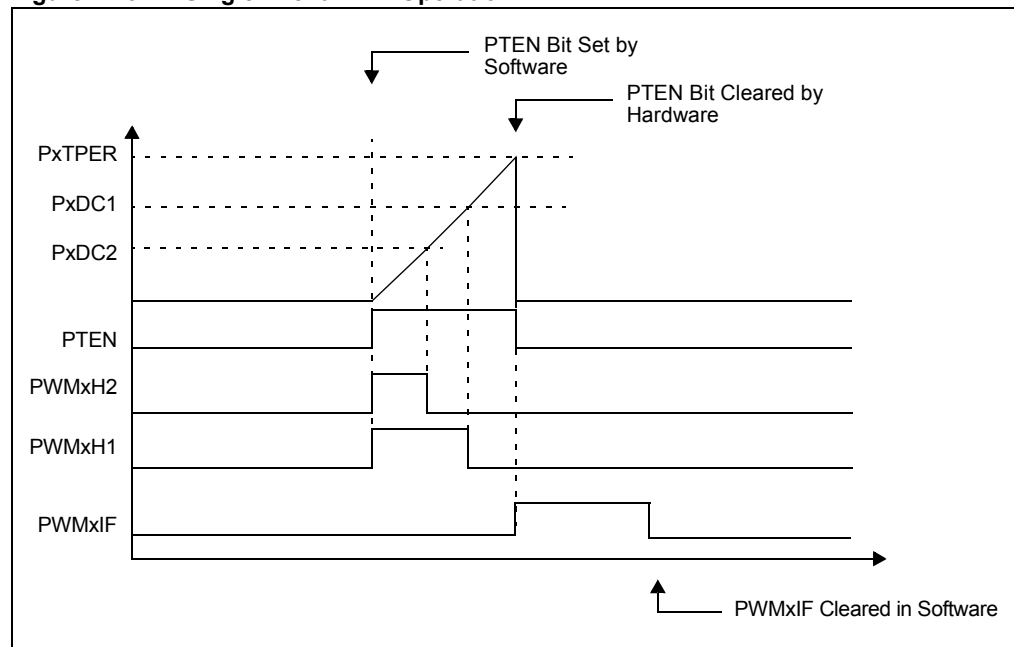
This section describes the PWM output modes.

47.9.1 Single Event PWM Operation

The PWM module produces single pulse outputs when the PWM time base is configured for the Single Event mode ($PTMOD<1:0> = 01$). This mode of operation is useful for driving certain types of electronically commutated motors, such as high-speed switched reluctance motor operation. Only edge-aligned outputs can be produced in Single Event mode.

In Single Event mode, the PWM I/O pin(s) are driven to the active state when the PTEN (PxTCON<15>) bit is set. When a match with a duty cycle register occurs, the PWM I/O pin is driven to the inactive state. When a match with the PxTPER register occurs, the PxTMR register is cleared, all active PWM I/O pins are driven to the inactive state, the PTEN bit is cleared and an interrupt is generated. Operation of the PWM module stops until the PTEN bit is set again in software.

Figure 47-5: Single Event PWM Operation



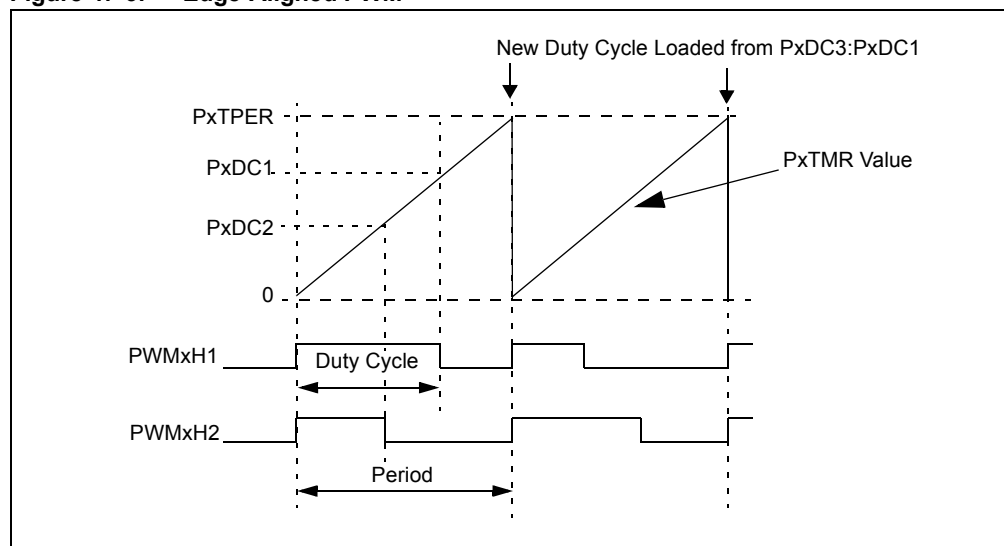
47.9.2 Edge-Aligned PWM

The PWM module produces edge-aligned PWM signals when the PWM time base is operating in Free-Running mode. The output signal for a given PWM channel has a period specified by the value loaded in PxTPER and a duty cycle specified by the appropriate PxDC3:PxDC1 register (see Figure 47-6). Assuming a non-zero duty cycle and no immediate updates enabled ($IUE = 0$), the outputs of all enabled PWM generators will be driven active at the beginning of the PWM period ($PxTMR = 0$). Each PWM output will be driven inactive when the value of PxTMR matches the duty cycle value of the PWM generator.

If the value in the PxDC3:PxDC1 register is zero, the output on the corresponding PWM pin is inactive for the entire PWM period. In addition, the output on the PWM pin is active for the entire PWM period if the value in the PxDC3:PxDC1 register is greater than the value held in the PxTPER register.

If immediate updates are enabled ($IUE = 1$), the new duty cycle value will be loaded when the new value is written to any active PxDC3:PxDC1 register.

Figure 47-6: Edge-Aligned PWM



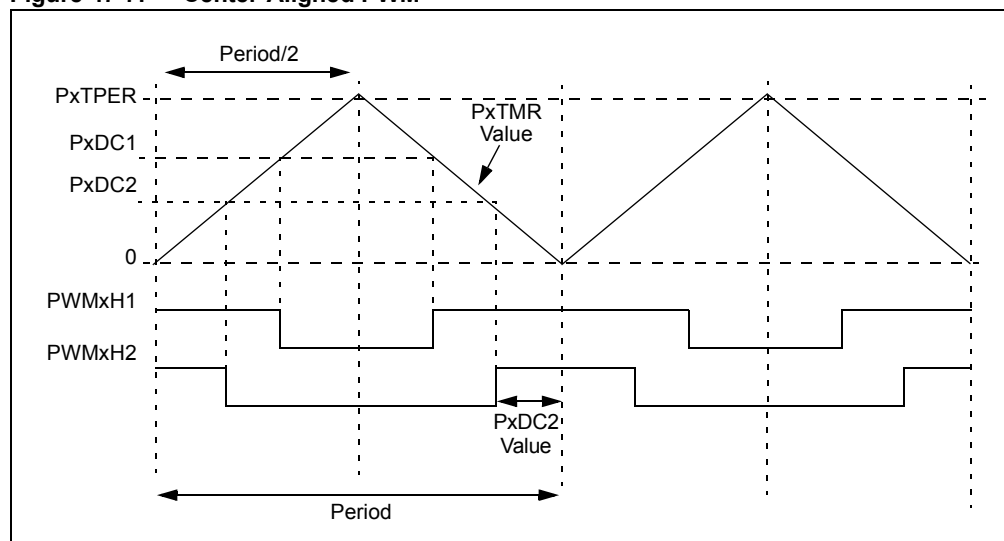
47.9.3 Center-Aligned PWM

The PWM module produces center-aligned PWM signals when the PWM time base is configured in one of the two Up/Down Counting modes ($PTMOD<1:0> = 1x$).

The PWM compare output is driven to the active state when the value of the duty cycle register matches the value of PTMR and the PWM time base is counting downward ($PTDIR = 1$). The PWM compare output is driven to the inactive state when the PWM time base is counting upward ($PTDIR = 0$) and the value in the PxTMR register matches the duty cycle value.

If the value in a particular duty cycle register is zero, the output on the corresponding PWM pin is inactive for the entire PWM period. In addition, the output on the PWM pin is active for the entire PWM period if the value in the duty cycle register is greater than the value in the PxTPER register.

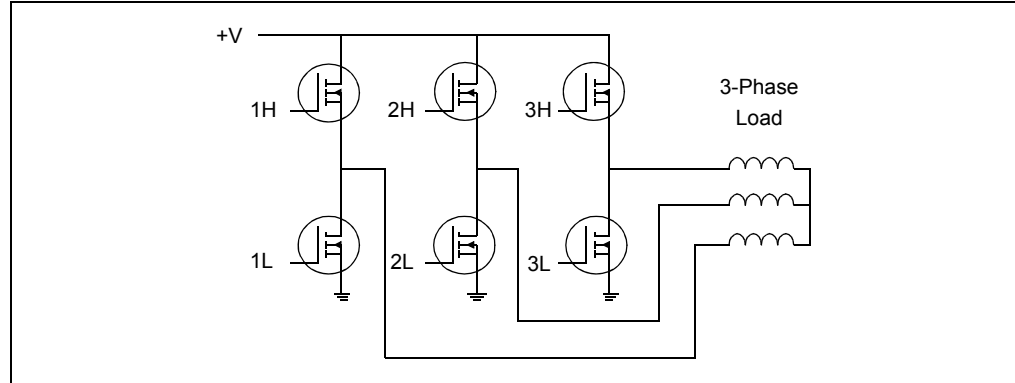
Figure 47-7: Center-Aligned PWM



47.9.4 Complementary PWM Output Mode

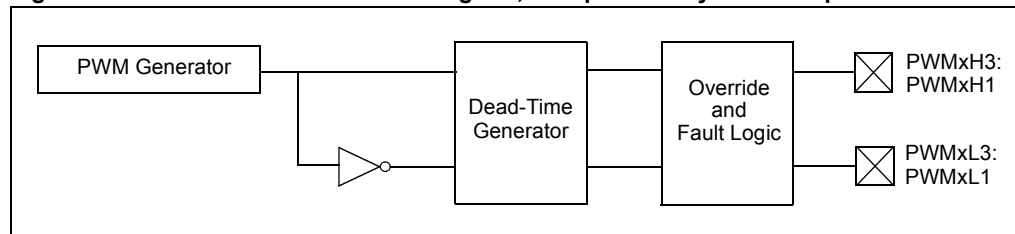
Complementary PWM Output mode is used to drive inverter loads similar to the one shown in Figure 47-8. This inverter topology is typical for ACIM and BLDC applications. In Complementary PWM Output mode, a pair of PWM outputs cannot be active simultaneously. Each PWM channel and output pin pair are internally configured as shown in Figure 47-9. A dead time can be optionally inserted during device switching, making both outputs inactive for a short period. (Refer to **Section 47.14 “Special Features of the MCPWM Module”**.)

Figure 47-8: Typical Load for Complementary PWM Outputs



Complementary PWM Output mode is selected for each PWM I/O pin pair by clearing the appropriate PWM I/O Pair Mode (PMOD) bits in PWM Control Register 1 (PWMxCON1<11:8>). The PWM I/O pins are set to Complementary PWM Output mode by default on a device Reset.

Figure 47-9: PWM Channel Block Diagram, Complementary PWM Output Mode



47.9.5 Independent PWM Output Mode

Independent PWM Output mode is useful for driving loads such as the one shown in Figure 47-10. A particular PWM output pair is in Independent PWM Output mode when the corresponding PWM I/O Pair Mode (PMOD) bits in PWM Control Register 1 (PWMxCON1<11:8>) is set. The dead-time generators are disabled in Independent PWM Output mode and there are no restrictions on the state of the pins for a given output pin pair.

Figure 47-10: Asymmetric Inverter Load Using Independent PWM Output Mode

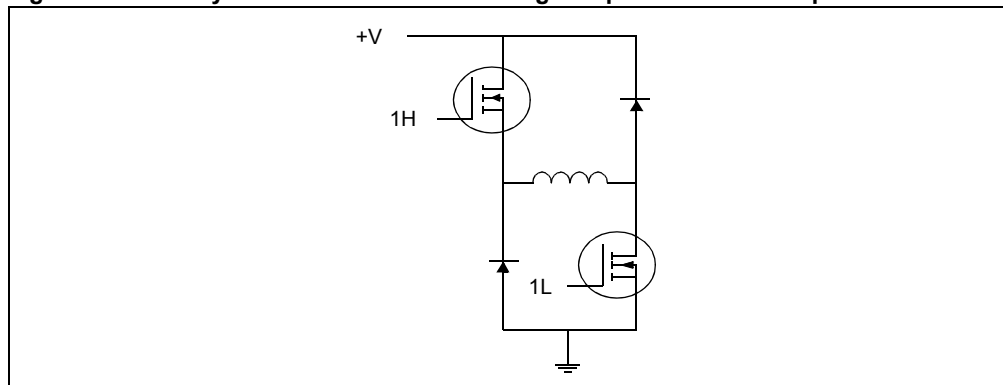
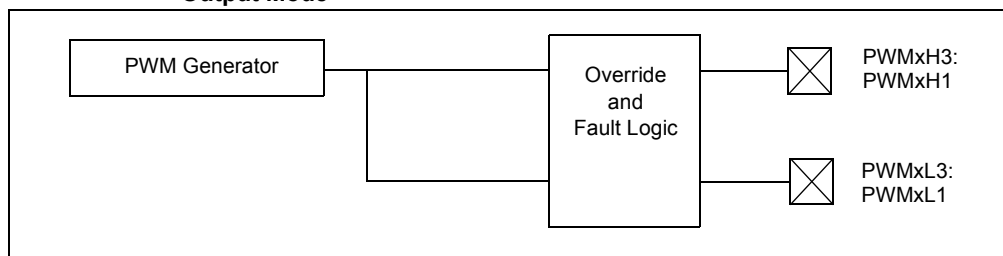


Figure 47-11: PWM Block Diagram for One Output Pin Pair, Independent PWM Output Mode



47.10 DUTY CYCLE REGISTER BUFFERING

The four PWM Duty Cycle registers, PxDC3:PxDC1, are buffered to allow glitchless updates of the PWM outputs. For each generator, there is a PxDC3:PxDC1 register (buffer register) that is accessible by the user application and a non-memory mapped Duty Cycle register that holds the actual compare value. The PWM duty cycle is updated with the value in the PxDC3:PxDC1 register at specific times in the PWM period to avoid glitches in the PWM output signal.

When the PWM time base is operating in Free-Running or Single Event mode (PTMOD<1:0> = 0x), the PWM duty cycle is updated whenever a match with the PxTPER register occurs and PxTMR is reset to '0'.

Note: Any write to the PxDC3:PxDC1 registers immediately updates the duty cycle when the PWM time base is disabled (PTEN = 0). This allows a duty cycle change to take effect before PWM signal generation is enabled.

When the PWM time base is operating in Up/Down Counting mode (PTMOD<1:0> = 10), duty cycles are updated when the value of the PxTMR register is zero and the PWM time base begins to count upward. Figure 47-12 indicates the times when the duty cycle updates occur for Up/Down Counting mode.

When the PWM time base is in Up/Down Counting mode with double updates (PTMOD<1:0> = 11), duty cycles are updated when the value of the PxTMR register is zero and when the value of the PxTMR register matches the value in the PxTPER register. Figure 47-12 and Figure 47-13 indicate the times when the duty cycle updates occur for this mode of the PWM time base.

Figure 47-12: Duty Cycle Update Times in Up/Down Counting Mode

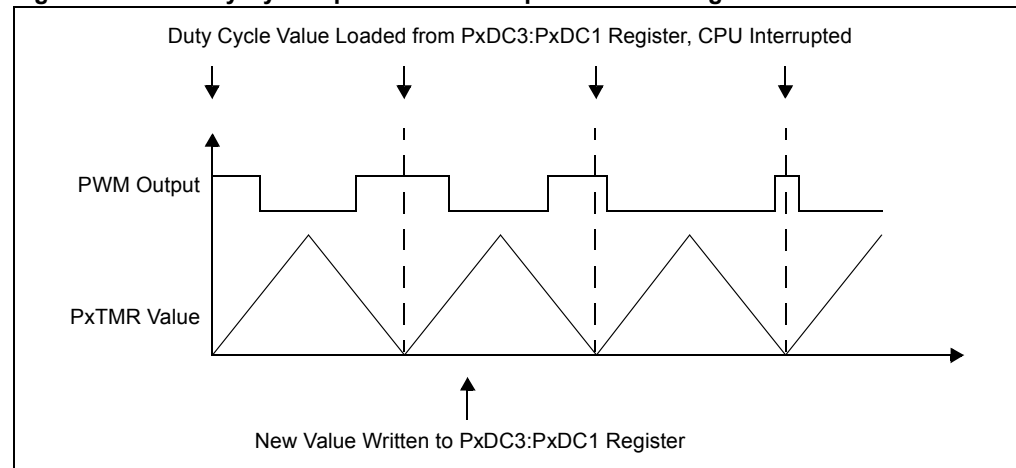
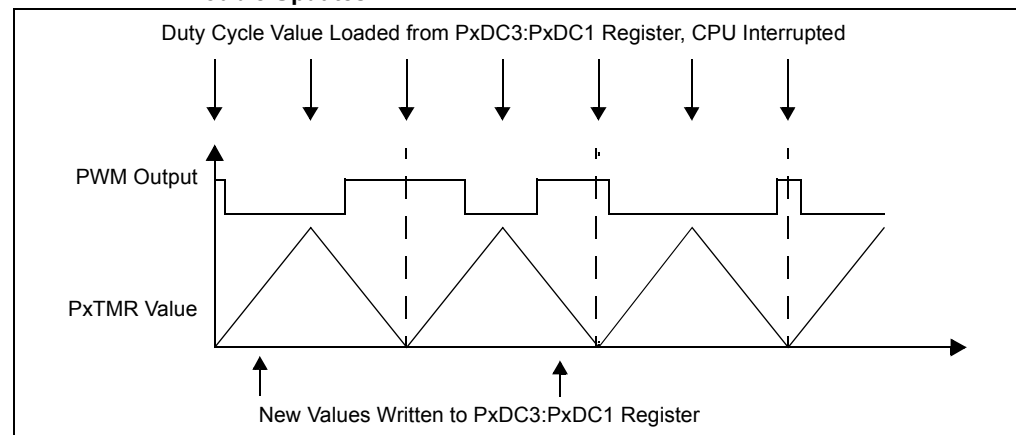


Figure 47-13: Duty Cycle Update Times in Up/Down Counting Mode with Double Updates



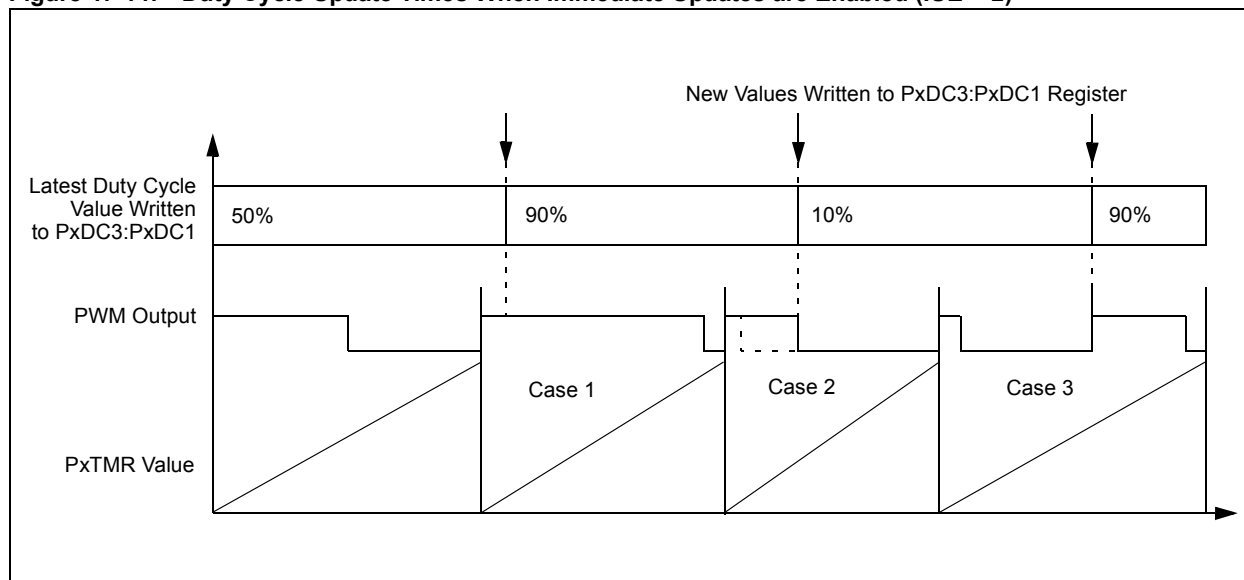
47.10.1 Immediate Update of PWM Duty Cycle

The Immediate Update Enable (IUE) bit in PWM Control Register 2 (PWMxCON2<2>) provides an option for updating the duty cycle values immediately after a write to the duty cycle registers. This feature eliminates waiting for the end of the time base period to update the duty cycle values. If the IUE bit is set, an immediate update of the duty cycle is enabled. If the bit is cleared, immediate update of the duty cycle is disabled. The following three cases are possible when immediate update is enabled:

- **Case 1:** If the PWM output is active at the time the new duty cycle is written, and the new duty cycle is greater than the current time base value, the PWM pulse width is lengthened.
- **Case 2:** If the PWM output is active at the time the new duty cycle is written, and the new duty cycle is less than the current time base value, the PWM pulse width is shortened.
- **Case 3:** If the PWM output is inactive at the time the new duty cycle is written, and the new duty cycle is greater than the current time base value, the PWM output becomes active immediately and remains active for the newly written duty cycle value.

Figure 47-14 shows the above mentioned cases.

Figure 47-14: Duty Cycle Update Times When Immediate Updates are Enabled (IUE = 1)



47.11 PWM DUTY CYCLE RESOLUTION

In the MCPWM module, the effective resolution for the generated PWM pulses is a function of the PWM frequency (or period) and the device operating frequency.

The maximum resolution (in bits) for a selected device oscillator and PWM frequency can be determined using the following formula:

Equation 47-3: PWM Resolution

$$PWMResolution = \log_2\left(\frac{2FCY}{FPWM}\right)$$

In Equation 47-3, FPWM is the PWM switching frequency and FCY is the device operating frequency.

Table 47-1 shows the PWM resolutions and frequencies for a selection of execution speeds and PxTPER values. The PWM frequencies in Table 47-1 are for Edge-Aligned (Free-Running PxTMR) PWM mode. For Center-Aligned modes (Up/Down PxTMR mode), the PWM frequencies are half the values in Table 47-1, as indicated in Table 47-2.

Table 47-1: Example of PWM Frequencies and Resolutions, 1:1 Prescaler, Edge-Aligned PWM

Tcy (Fcy)	PxTPER Value	PxDC3:PxDC1 Value for 100%	PWM Resolution	PWM Frequency (FPWM)
62.5 ns (16 MHz)	0x7FFE	0xFFFF	16 bits	488 kHz
62.5 ns (16 MHz)	0x3FE	0x7FE	11 bits	15.62 kHz
100 ns (10 MHz)	0x7FFE	0xFFFF	16 bits	305 Hz
100 ns (10 MHz)	0x1FE	0x3FE	10 bits	19.53 kHz
125 ns (8 MHz)	0x7FFE	0xFFFF	16 bits	244 Hz
125 ns (8 MHz)	0xFE	0x1FE	9 bits	31.25 kHz
250 ns (4 MHz)	0x7FFE	0xFFFF	16 bits	122 Hz
250 ns (4 MHz)	0x7E	0xFE	8 bits	31.25 kHz

Table 47-2: Example of PWM Frequencies and Resolutions, 1:1 Prescaler, Center-Aligned PWM

Tcy (Fcy)	PxTPER Value	PxDC3:PxDC1 Value for 100%	PWM Resolution	PWM Frequency
62.5 ns (16 MHz)	0x7FFE	0xFFFF	16 bits	244 Hz
62.5 ns (16 MHz)	0x3FFE	0x7FFE	15 bits	976 Hz
100 ns (10 MHz)	0x7FFE	0xFFFF	16 bits	152 Hz
100 ns (10 MHz)	0x1FFE	0x3FFE	14 bits	610 Hz
125 ns (8 MHz)	0x7FFE	0xFFFF	16 bits	122 Hz
125 ns (8 MHz)	0xFFE	0x1F FE	13 bits	976 Hz
250 ns (4 MHz)	0x7FFE	0xFFFF	16 bits	61 Hz
250 ns (4 MHz)	0x7FE	0xFFE	12 bits	976 Hz

Note: 100% duty cycle cannot be accomplished when PTPER = 0x7FFF. Maximum duty cycle in this scenario is 100 percent minus one-half Tcy.

The MCPWM module can produce PWM signal edges with $T_{CY}/2$ resolution. PXTMR increments every T_{CY} with a 1:1 prescaler. To achieve $T_{CY}/2$ edge resolution, PxDC3:PxDC1<15:1> are compared to PXTMR<14:0> to determine a duty cycle match. The value in PxDC3:PxDC1<0> determines whether the PWM signal edge will occur at the T_{CY} or the $T_{CY}/2$ boundary. When a 1:4, 1:16 or 1:64 prescaler is used with the PWM time base, PxDC3:PxDC1<0> is compared to the Most Significant bit (MSb) of the prescaler counter clock to determine when the PWM edge should occur.

PXTMR and PxDC3:PxDC1 resolutions are depicted in Figure 47-15. In this example, PXTMR resolution is T_{CY} and PxDC3:PxDC1 resolution is $T_{CY}/2$ for 1:1 prescaler selection.

Figure 47-15: PXTMR and PxDC3:PxDC1 Resolution Timing Diagram, Free-Running Mode and 1:1 Prescaler Selection

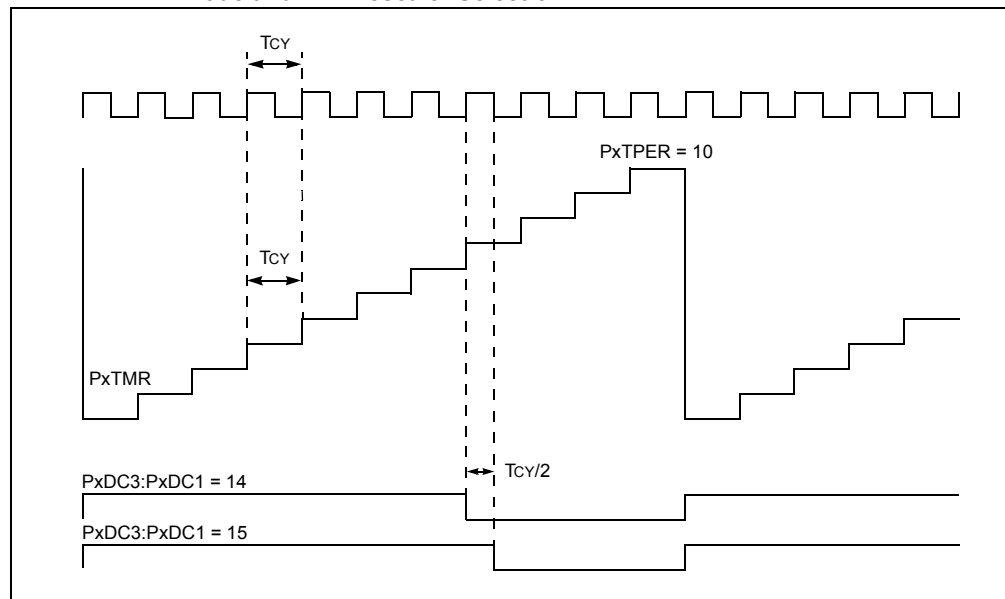
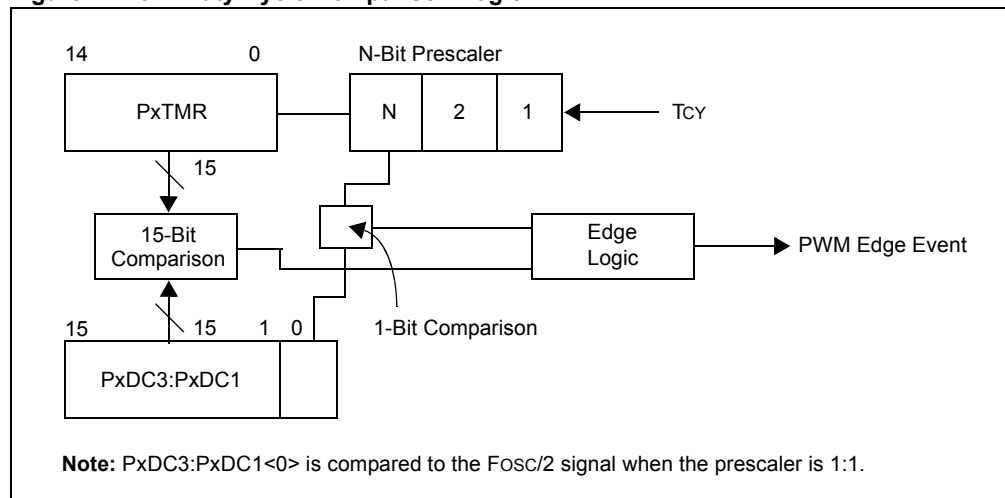


Figure 47-16: Duty Cycle Comparison Logic



47.12 PWM DEAD-TIME CONTROL

Each complementary output pair for the PWM module has a 6-bit down counter that is used to produce the dead-time insertion. As shown in Figure 47-17, each dead-time unit has a rising and falling edge detector connected to the duty cycle comparison output.

One of the two possible dead times is loaded into the timer on the detected PWM edge event. Depending on whether the edge is rising or falling, one of the transitions on the complementary outputs is delayed until the timer counts down to zero. Figure 47-18 shows a timing diagram indicating the dead-time insertion for one pair of PWM outputs. The use of two different dead times for the rising and falling edge events has been exaggerated in the figure for clarity.

Figure 47-17: Dead-Time Unit Block Diagram for One Output Pin Pair

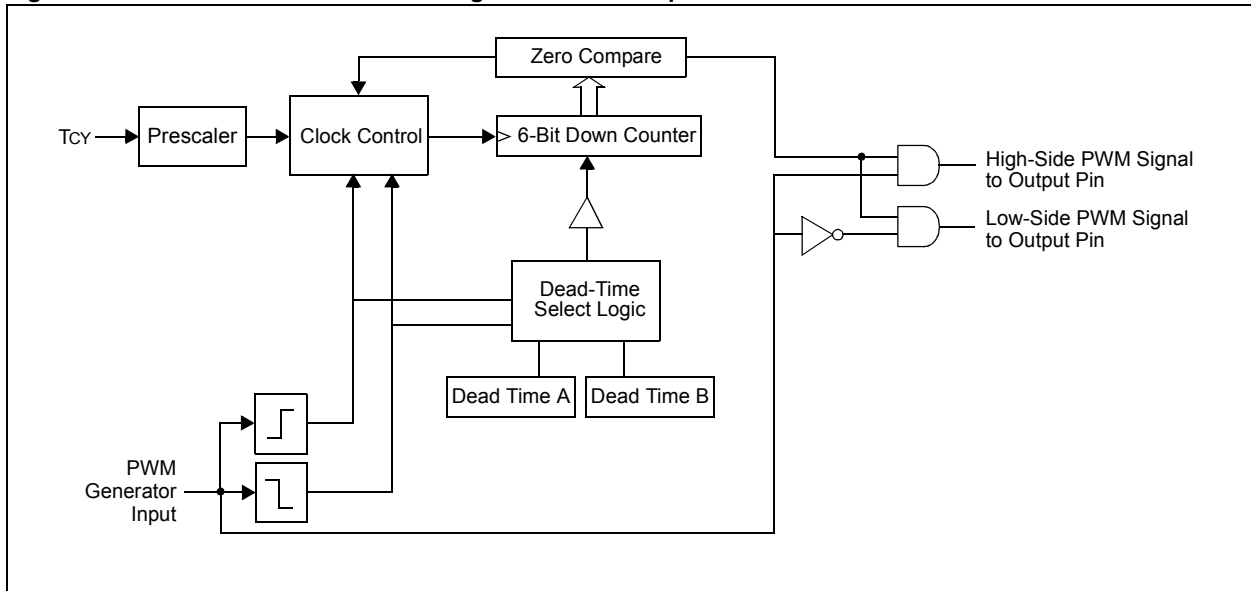
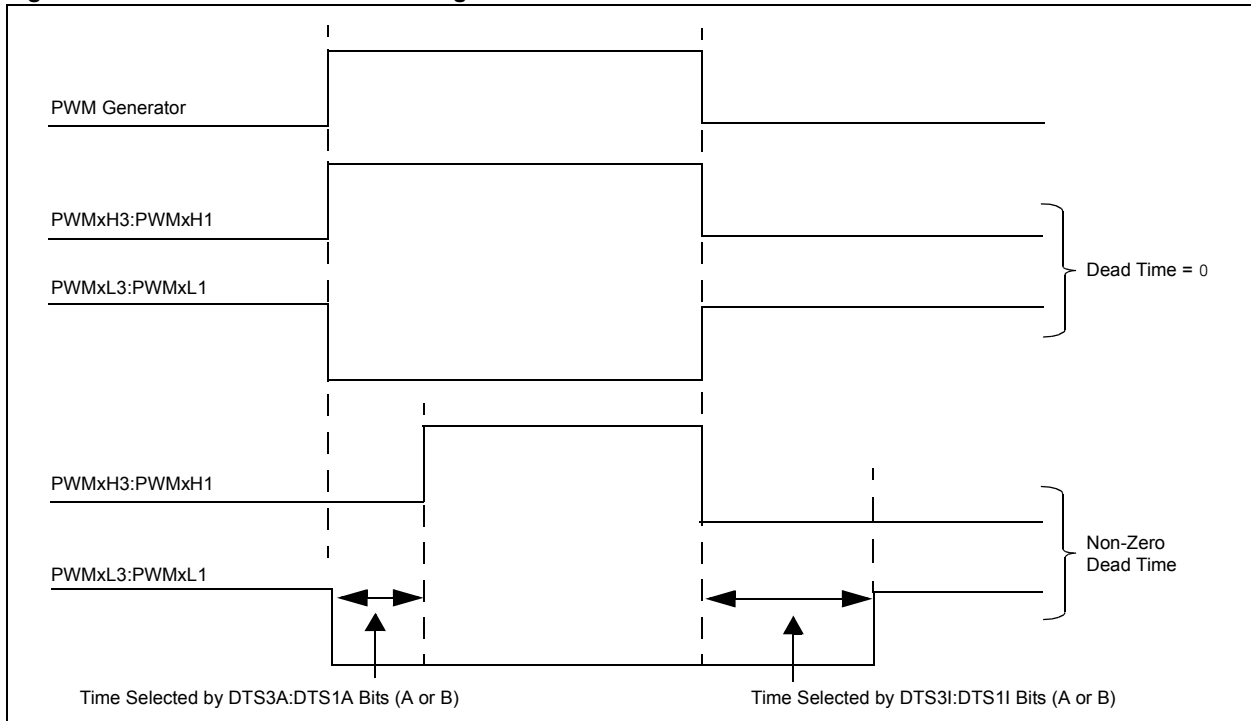


Figure 47-18: Dead-Time Insertion Diagram



47.12.1 Dead-Time Assignment

The Dead-Time Control Register 2 (PxDTCON2) contains control bits that allow the two programmable dead times to be assigned to each of the complementary outputs. There are two dead-time assignment control bits for each of the complementary outputs. For example, the Dead-Time Select for PWM1 Signal Going Active (DTS1A) and Dead-Time Select for PWM I/O Pair 1 Signal Going Inactive (DTS1I) control bits select the dead times to be used for the PWM1H1/PWM1L1 complementary output pair. The pair of dead-time selection control bits are referred to as the 'dead-time-select-active' and 'dead-time-select-inactive' control bits, respectively. The function of each bit in a pair is as follows:

- The DTS3A:DTS1A control bits select the dead time that is to be inserted before the high-side output is driven active.
- The DTS3I:DTS1I control bits select the dead time that is to be inserted before the low-side PWM output is driven active.

Table 47-3 summarizes the function of each dead-time selection control bit.

Table 47-3: Dead-Time Selection Bits

Bit	Function
DTS1A	Selects PWM1H1/PWM1L1 dead time inserted before PWM1H1 is driven active.
DTS1I	Selects PWM1H1/PWM1L1 dead time inserted before PWM1L1 is driven active.
DTS2A	Selects PWM1H2/PWM1L2 dead time inserted before PWM1H2 is driven active.
DTS2I	Selects PWM1H2/PWM1L2 dead time inserted before PWM1L2 is driven active.
DTS3A	Selects PWM1H3/PWM1L3 dead time inserted before PWM1H3 is driven active.
DTS3I	Selects PWM1H3/PWM1L3 dead time inserted before PWM1L3 is driven active.

47.12.2 Dead-Time Ranges

Dead Time Unit A and Dead Time Unit B are set by selecting an input clock prescaler value and a 6-bit unsigned dead-time count value.

Four input clock prescaler selections have been provided to allow a suitable range of dead times based on the device operating frequency. The clock prescaler option can be selected independently for each of the two dead-time values. The dead-time clock prescaler values are selected using the Dead Time Unit A. The Prescale Select (DTAPS) bits<1:0> and Dead Time Unit B Prescale Select (DTBPS) bits<1:0> in the Dead-Time Control Register 1 (PxDTCON1<15:14> and PxDTCON1<7:6>) SFR. The following clock prescaler options can be selected for each of the dead-time values:

- TCY
- 2 TCY
- 4 TCY
- 8 TCY

Equation 47-4: Dead-Time Calculation

$DT = \frac{\text{Dead Time}}{\text{Prescale Value} \cdot TCY}$
<p>Note: DT (Dead Time) is the DTA<5:0> or DTB<5:0> register value.</p>

Table 47-4 shows an example of the dead-time ranges as a function of the selected input clock prescaler and the device operating frequency.

Table 47-4: Example Dead-Time Ranges

Tcy (Fcy)	Prescaler Selection	Resolution	Dead-Time Range
62.5 ns (16 MHz)	1 Tcy	62.5 ns	62.5 ns-4 µs
62.5 ns (16 MHz)	4 Tcy	250 ns	250 ns-16 µs
125 ns (8 MHz)	1 Tcy	125 ns	125 ns-8 µs
125 ns (8 MHz)	2 Tcy	250 ns	250 ns-16 µs
250 ns (4 MHz)	1 Tcy	250 ns	250 ns-16 µs

47.12.3 Dead-Time Distortion

For short PWM duty cycles, the ratio of dead time to the active PWM time can become large. In an extreme case, when the duty cycle is less than or equal to the programmed duty cycle, no PWM pulse will be generated. In these cases, the inserted dead time introduces distortion into waveforms produced by the PWM module.

The user application can minimize dead-time distortion by keeping the PWM duty cycle at least three times larger than the dead time. Dead-time distortion can also be corrected by other techniques, such as closed loop current control.

A similar effect occurs for duty cycles near 100%. The maximum duty cycle used in the application should be chosen such that the minimum inactive time of the PWM signal is at least three times larger than the dead time.

The following code examples demonstrate how to configure the MCPWM module.

Example 47-1: MCPWM Module Operating Mode and Time Selection

```
/* PWM time base operates in a Free Running mode */

P1TCONbits.PTMOD = 0b00;

/* PWM time base input clock period is Tcy (1:1 prescale) */
/* PWM time base output post scale is 1:1 */

P1TCONbits.PTCKPS = 0b00;
P1TCONbits.PTOPS = 0b00;

/* Choose PWM time period based on input clock selected */
/* Refer to Equation 47-1 */
/* PWM switching frequency is 20 kHz */
/* Fcy is 16 MHz */

P1TPER = 799;
```

Example 47-2: MCPWM Module Output Mode Selection

```
/* PWM I/O pairs 1 to 3 are in complementary mode */
/* PWM pins are enabled for PWM output */

PWM1CON1bits.PMOD1 = 0;
PWM1CON1bits.PMOD2 = 0;
PWM1CON1bits.PMOD3 = 0;
PWM1CON1bits.PEN1H = 1;
PWM1CON1bits.PEN2H = 1;
PWM1CON1bits.PEN3H = 1;
PWM1CON1bits.PEN1L = 1;
PWM1CON1bits.PEN2L = 1;
PWM1CON1bits.PEN3L = 1;

/* Immediate update of PWM enabled */

PWM1CON2bits.IUE = 1;
```

Example 47-3: Dead-Time Insertion (Complementary PWM Output Mode Only)

```
/* Clock period for Dead Time Unit A is Tcy */
/* Clock period for Dead Time Unit B is Tcy */

P1DTCN1bits.DTAPS = 0b00;
P1DTCN1bits.DTBPS = 0b00;

/* Dead time value for Dead Time Unit A */
/* Dead time value for Dead Time Unit B */

P1DTCN1bits.DTA = 10;
P1DTCN1bits.DTB = 20;

/* Dead Time Unit selection for PWM signals */
/* Dead Time Unit A selected for PWM active transitions */
/* Dead Time Unit B selected for PWM inactive transitions */

P1DTCN2bits.DTS3A = 0;
P1DTCN2bits.DTS2A = 0;
P1DTCN2bits.DTS1A = 0;

P1DTCN2bits.DTS3I = 1;
P1DTCN2bits.DTS2I = 1;
P1DTCN2bits.DTS1I = 1;
```

Example 47-4: MCPWM Module I/O Pin Control

```
/* PWM I/O pin controlled by PWM Generator */

P1OVDCONbits.POVD3H = 1;
P1OVDCONbits.POVD2H = 1;
P1OVDCONbits.POVD1H = 1;
P1OVDCONbits.POVD3L = 1;
P1OVDCONbits.POVD2L = 1;
P1OVDCONbits.POVD1L = 1;
```

Example 47-5: MCPWM Module Duty Cycle Initialization

```
/* Initialize duty cycle values for PWM1, PWM2 and PWM3 signals */

P1DC1 = 200;
P1DC2 = 200;
P1DC3 = 200;
```

Example 47-6: Enabling PWM Pulse Generation

```
P1TCONbits.PTEN = 1;
```

47.13 PWM FAULT HANDLING

There are two Fault pins, $\overline{\text{FLTxA}}$ and $\overline{\text{FLTxB}}$, associated with the PWM module. When asserted, these pins can optionally drive each of the PWM I/O pins to a defined state. This action takes place without software intervention, so Fault events can be managed quickly.

These Fault pins can have other multiplexed functions depending on the PIC24F device variant. When used as a Fault input, each Fault pin is readable using its corresponding PORT register. The $\overline{\text{FLTxA}}$ and $\overline{\text{FLTxB}}$ pins function as active low inputs so that it is easy to inclusively OR many sources to the same input through an external pull-up resistor. When not used with the PWM module, these pins can be used as general purpose I/O or for another multiplexed function. Each Fault pin has its own Interrupt vector, interrupt flag bit, interrupt enable bit and interrupt priority bits.

The function of the $\overline{\text{FLTxA}}$ pin is controlled by the Fault A Configuration (PxFLTACON) register and the function of the $\overline{\text{FLTxB}}$ pin is controlled by the Fault B Configuration (PxFLTBCON) register.

47.13.1 Fault Pin Enable Bits

The PxFLTACON and PxFLTBCON registers each have four Fault Input Enable (FAEN<4:1> and FBEN<4:1>) bits that determine whether a particular pair of PWM I/O pins is to be controlled by the Fault input pin. To enable a specific PWM I/O pin pair for Fault overrides, the corresponding bit should be set in the PxFLTACON or PxFLTBCON register.

If all enable bits are cleared in the PxFLTACON or PxFLTBCON registers, that Fault input pin has no effect on the PWM module and no Fault interrupts are produced.

47.13.2 Fault States

The PxFLTACON and PxFLTBCON Special Function Registers each have eight bits that determine the state of each PWM I/O pin when the Fault input pin becomes active. When these bits are cleared, the PWM I/O pin is driven to the inactive state. If the bit is set, the PWM I/O pin is driven to the active state. The active and inactive states are referenced to the polarity defined for each PWM I/O pin (set by HPOL and LPOL Configuration bits).

A special case exists when a PWM module I/O pair is in Complementary PWM Output mode and both pins are programmed to be active on a Fault condition. The high-side pin will always have priority in Complementary PWM Output mode, so that both I/O pins cannot be driven active simultaneously.

47.13.3 Fault Input Modes

Each of the Fault input pins has two modes of operation:

- **Latched Mode:** When the Fault pin is driven low, the PWM outputs go to the states defined in the PxFLTACON and PxFLTBCON registers. The PWM outputs remain in this state until the Fault pin is driven high and the corresponding interrupt flag (FLTxAIF or FLTxBIF) has been cleared in software. When both of these actions have occurred, the PWM outputs return to normal operation at the beginning of the next PWM period or half-period boundary, regardless of the Immediate Update Enable (IUE) bit value. If the interrupt flag is cleared before the Fault condition ends, the PWM module waits until the Fault pin is no longer asserted to restore the outputs.
- **Cycle-by-Cycle Mode:** When the Fault input pin is driven low, the PWM outputs remain in the defined Fault states for as long as the Fault pin is held low. After the Fault pin is driven high, the PWM outputs return to normal operation at the beginning of the following PWM period (or half-period boundary in center-aligned modes) even when immediate updates are enabled.

The operating mode for each Fault input pin is selected using the Fault A Mode (FLTAM) bit and Fault B Mode (FLTBM) bit (PxFLTACON<7> and PxFLTBCON<7>).

47.13.3.1 ENTRY INTO A FAULT CONDITION

When a Fault pin is enabled and driven low, the PWM pins are immediately driven to their programmed Fault states regardless of the values in the PWM Duty Cycle (PxDCy) and Override Control (PxOVDCON) registers. The Fault action has priority over all other PWM control registers.

47.13.3.2 EXIT FROM A FAULT CONDITION

A Fault condition must be cleared by the external circuitry driving the Fault input pin high and clearing the Fault interrupt flag (Latched mode only). After the Fault pin condition has been cleared, the PWM module restores the PWM output signals on the next PWM period or half-period boundary. For edge-aligned PWM generation, the PWM outputs are restored when $PxTMR = 0$. For center-aligned PWM generation, the PWM outputs are restored when $PxTMR = 0$ or $PxTMR = PxTPER$, whichever event occurs first.

An exception to these rules occurs when the PWM time base is disabled ($PTEN = 0$). If the PWM time base is disabled, the PWM module restores the PWM output signals immediately after the Fault condition has been cleared.

47.13.4 Fault Pin Priority

If both Fault input pins have been assigned to control a particular pair of PWM pins, the Fault states programmed for the \overline{FLTxA} input pin will take priority over the \overline{FLTxB} input pin.

One of two actions will take place when the Fault A condition has been cleared. If the \overline{FLTxB} input is still asserted, the PWM outputs will return to the states programmed in the Fault B Control (PxFLTBCON) register on the next period or half-period boundary. If the \overline{FLTxB} input is not asserted, the PWM outputs will return to normal operation on the next period or half-period boundary.

Note: When the \overline{FLTxA} pin is programmed for Latched mode, the PWM outputs will not return to the Fault B states or normal operation until the Fault A interrupt flag has been cleared and the \overline{FLTxA} pin is deasserted.
--

47.13.5 Fault Pin Software Control

Each of the Fault pins can be controlled manually in software. Since each Fault input is shared with a PORT I/O pin, the PORT pin can be configured as an output by clearing the corresponding TRIS bit. When the PORT bit for the pin is cleared, the Fault input is activated.

Note: Caution should be exercised when controlling the Fault inputs in software. If the TRIS bit for the Fault pin is cleared, the Fault input cannot be driven externally.
--

47.13.6 Fault Timing Examples

The following figures provide examples of PWM Fault timing.

Figure 47-19: Example Fault Timing, Cycle-by-Cycle Mode

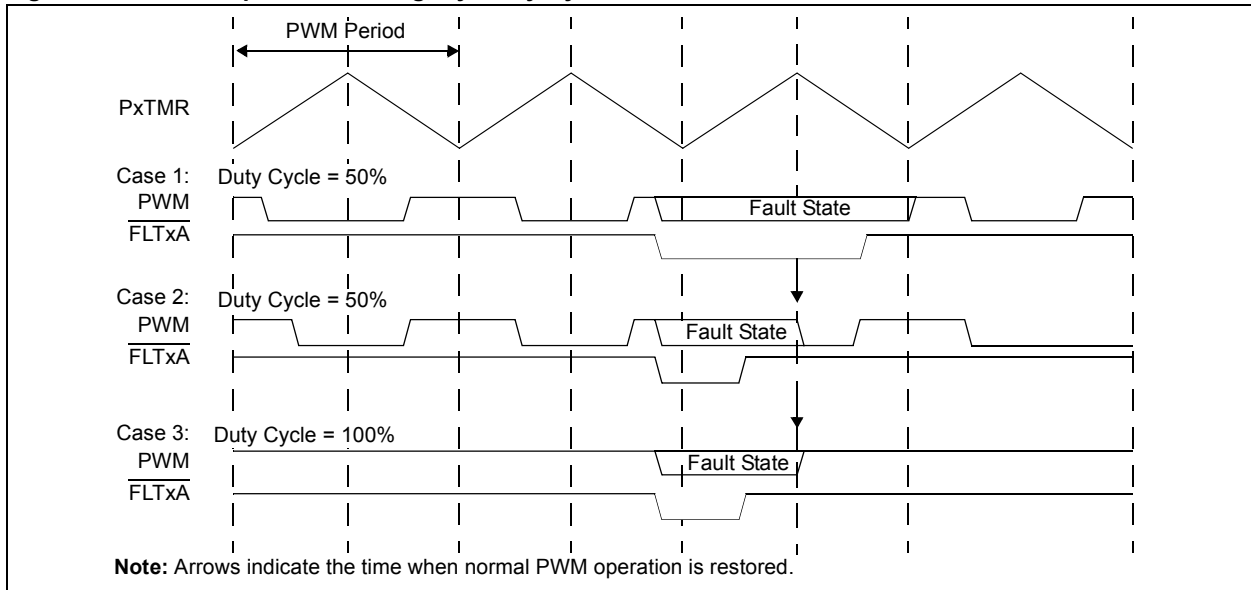


Figure 47-20: Example Fault Timing, Latched Mode

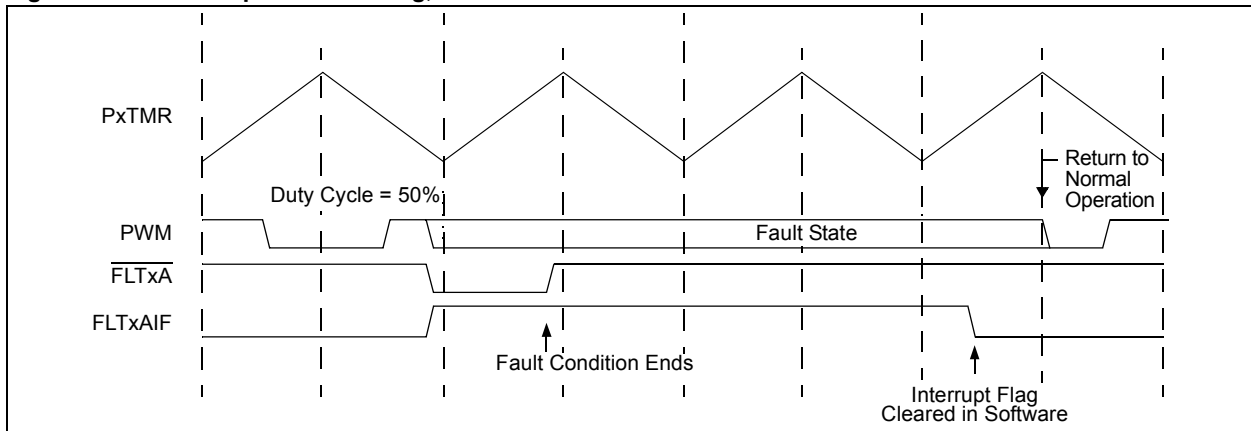
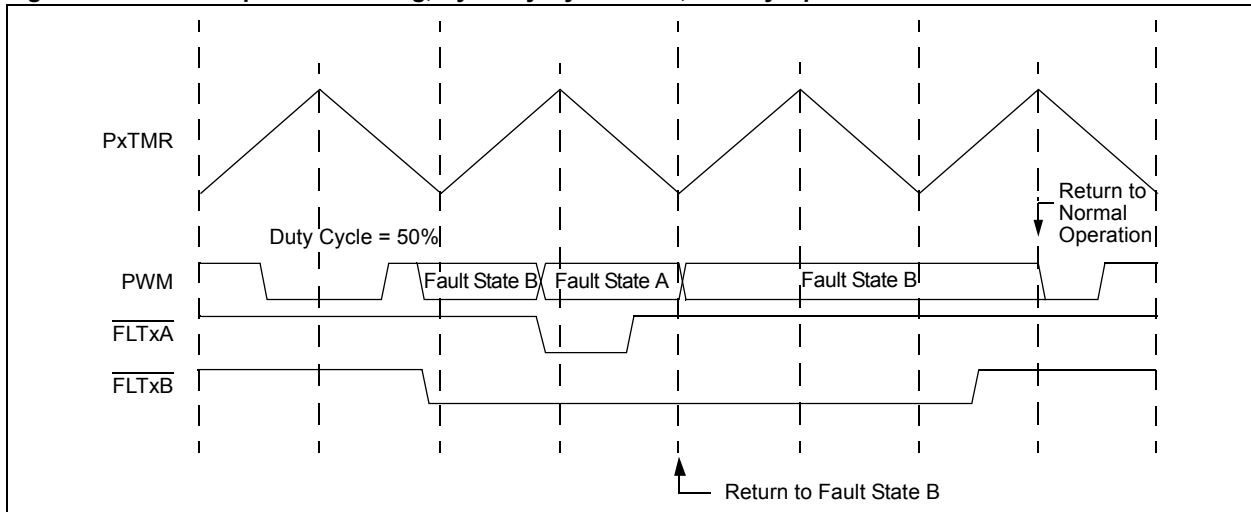


Figure 47-21: Example Fault Timing, Cycle-by-Cycle Mode, Priority Operation



47.14 SPECIAL FEATURES OF THE MCPWM MODULE

The following special features are available in the MCPWM module:

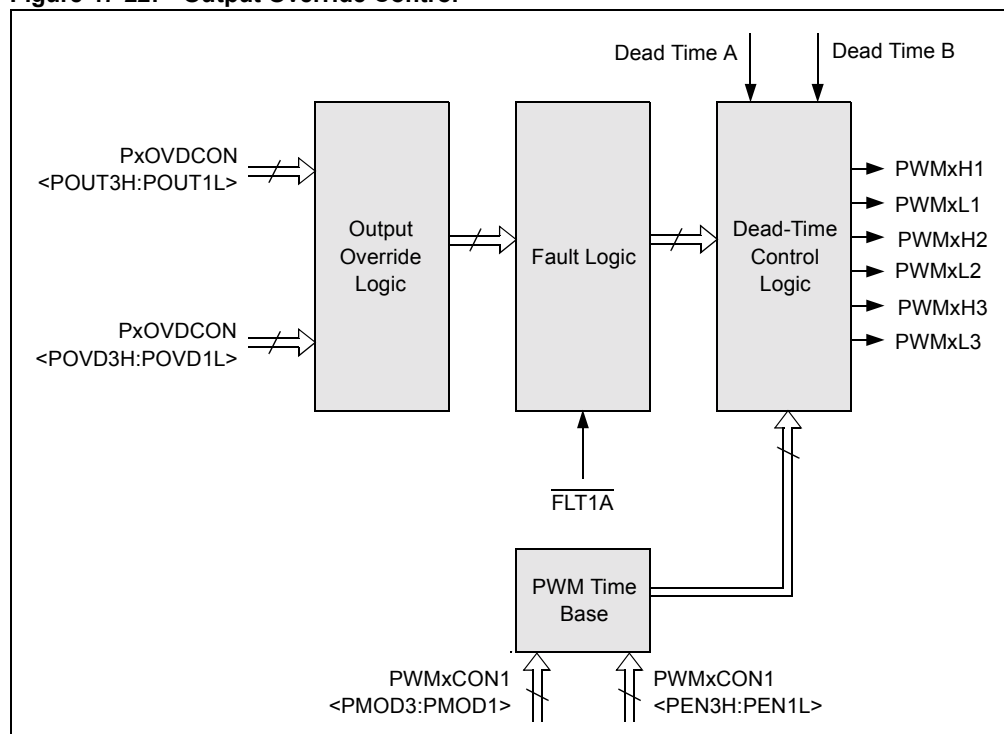
- PWM output override
- Special Event Trigger
- PWM update lockout
- Write-protected registers

47.14.1 PWM Output Override

The PWM output override bits allow the PWM I/O pins to be manually driven to specified logic states, independent of the duty cycle comparison units. The PWM override bits are useful when controlling various types of electrically commutated motors.

Figure 47-22 shows a block diagram of the PWM output override control.

Figure 47-22: Output Override Control



All control bits associated with the PWM output override function are in the Override Control (PxOVDCON) register. The upper half of the PxOVDCON register contains six PWM Output Override bits (POVD3H:POVD1L) that determine which PWM I/O pins will be overridden. The lower half of the PxOVDCON register contains six PWM Manual Output (POUT3H:POUT1L) bits that determine the state of the PWM I/O pin when it is overridden with the POVD3H:POVD1L bits.

The POVD bits are active-low control bits. When the POVD bits are set, the corresponding POUT3H:POUT1L bits have no effect on the PWM output. When one of the POVD bits is cleared, the output on the corresponding PWM I/O pin is determined by the state of the POUT bit. When a POUT bit is set, the PWM pin is driven to its active state. When the POUT bit is cleared, the PWM pin is driven to its inactive state.

The code shown in Example 47-7 demonstrates the PWM output override feature.

Example 47-7: Code for Using the MCPWM Output Override Feature

```

/* Output Override Synchronization */

/* Output overrides via the P1OVDCON register are synchronized to the PWM */
/* time base by setting the OSYNC bit */

PWM1CON2bits.OSYNC = 1;

/* Override control register configuration */
/* Output on the PWM1H3:PWM1H1 and PWM1L3:PWM1L1 I/O pins are controlled */
/* by the corresponding POUT3H:POUT1L bits in the P1OVDCON register */

P1OVDCONbits.POVD3H = 0;
P1OVDCONbits.POVD2H = 0;
P1OVDCONbits.POVD1H = 0;
P1OVDCONbits.POVD3L = 0;
P1OVDCONbits.POVD2L = 0;
P1OVDCONbits.POVD1L = 0;

/* PWM I/O pins are driven to active state by setting the corresponding bit */

P1OVDCONbits.POUT3H = 1;
P1OVDCONbits.POUT2H = 1;
P1OVDCONbits.POUT1H = 1;
P1OVDCONbits.POUT3L = 1;
P1OVDCONbits.POUT2L = 1;
P1OVDCONbits.POUT1L = 1;

```

47.14.1.1 OVERRIDE CONTROL FOR COMPLEMENTARY OUTPUT MODE

The PWM module does not allow certain overrides when a pair of PWM I/O pins are operating in Complementary PWM Output mode ($PMOD<3:1> = 0$). The module does not allow both pins in the output pair to become active simultaneously. The high-side pin in each output pair always takes priority.

Note: Dead-time insertion is still performed when PWM channels are overridden manually.

47.14.1.2 OVERRIDE SYNCHRONIZATION

If the Output Override Synchronization ($OSYNC = 1$) bit is set ($PWMxCON2<1>$), all output overrides performed using the $PxOVDCON$ register will be synchronized to the PWM time base. Synchronous output overrides will occur at the following times:

- Edge-Aligned mode when $PxTMR$ is zero
- Center-Aligned modes when $PxTMR$ is zero
- When the value of $PxTMR$ matches $PxTPER$

The override synchronization function, when enabled, can be used to avoid unwanted narrow pulses on the PWM output pins.

47.14.1.3 OUTPUT OVERRIDE EXAMPLES

Figure 47-23 shows an example of a waveform that might be generated using the PWM output override feature. This figure also shows a six-step commutation sequence for a BLDC motor. The motor is driven through a 3-phase inverter, as shown in Figure 47-24. When the appropriate rotor position is detected, the PWM outputs are switched to the next commutation state in the sequence. In this example, the PWM outputs are driven to specific logic states. The $PxOVDCON$ register values used to generate the signals in Figure 47-23 are given in Table 47-5.

The PWM Duty Cycle registers can be used in conjunction with the $PxOVDCON$ register. The Duty Cycle registers control the current delivered to the load and the $PxOVDCON$ register controls the commutation. Such an example is shown in Figure 47-24. The $PxOVDCON$ register values used to generate the signals in Figure 47-24 are given in Table 47-6.

Table 47-5: PWM Output Override Example 1

State	PxOVDCON<15:8>	PxOVDCON<7:0>
1	00000000b	00100100b
2	00000000b	00100001b
3	00000000b	00001001b
4	00000000b	00011000b
5	00000000b	00010010b
6	00000000b	00000110b

Figure 47-23: PWM Output Override Example 1

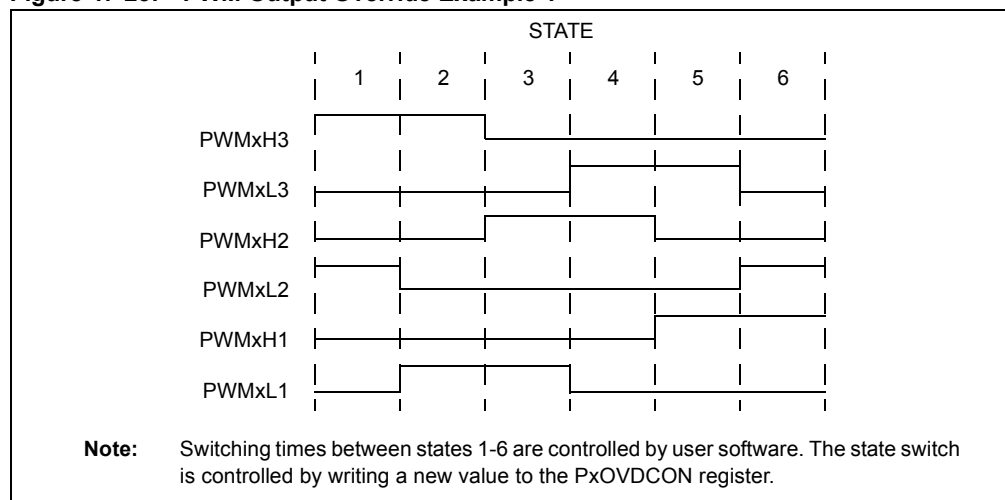
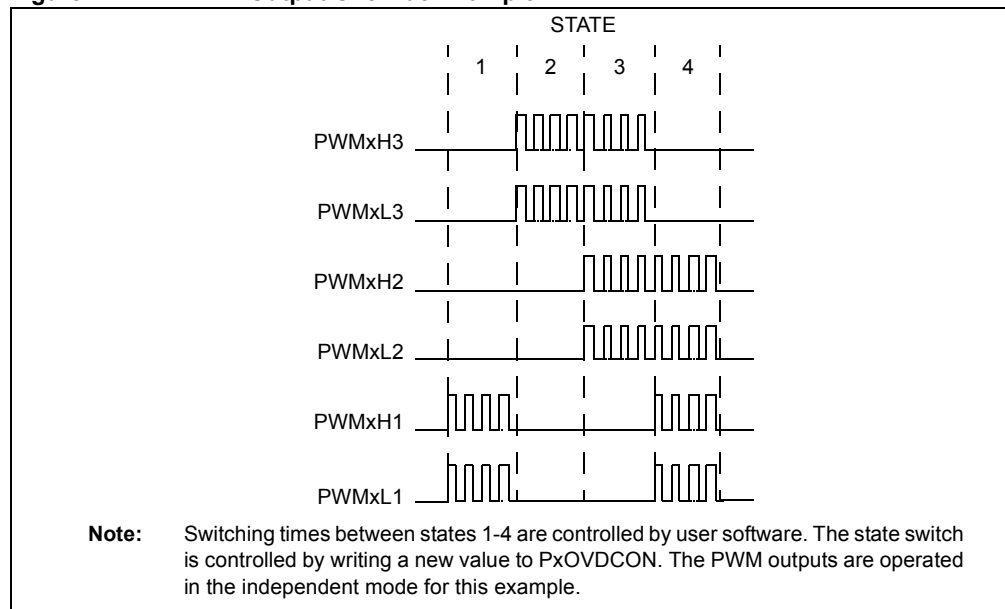


Table 47-6: PWM Output Override Example 2

State	PxOVDCON<15:8>	PxOVDCON<7:0>
1	11000011b	00000000b
2	11110000b	00000000b
3	00111100b	00000000b
4	00001111b	00000000b

Figure 47-24: PWM Output Override Example 2



47.14.2 Special Event Trigger

The PWM module has a Special Event Trigger that allows analog-to-digital conversions to be synchronized to the PWM time base. The analog-to-digital sampling and conversion time can be programmed to occur at any point within the PWM period. The Special Event Trigger can minimize the delay between the time the analog-to-digital conversion results are acquired and the time the duty cycle value is updated.

The PWM Special Event Trigger has one SFR (PxSECMP) and four Postscaler Control bits (SEVOPS<3:0>) to control its operation. The PxTMR value, for which a Special Event Trigger should occur, is loaded into the Special Event Compare (PxSECMP) register.

When the PWM time base is in Up/Down Counting mode, an additional control bit is required to specify the counting phase for the Special Event Trigger. The count phase is selected using the Special Event Trigger Time Base Direction (SEVTDIR) bit in the MSb of the Special Event Compare (PxSECMP<15>) register. If the SEVTDIR bit is cleared, the Special Event Trigger will occur on the upward counting cycle of the PWM time base. If the SEVTDIR bit is set, the Special Event Trigger will occur on the downward count cycle of the PWM time base. The SEVTDIR control bit has no effect unless the PWM time base is configured for Up/Down Counting mode.

The code in Example 47-8 demonstrates how to trigger an analog-to-digital conversion based on MCPWM special event generation.

Example 47-8: Triggering ADC Based on MCPWM Special Event Generation

```
/* Select Special Event time base direction such that trigger will occur */
/* when PWM time base is counting downwards */

P1SECMPbits.SEVTDIR = 1;

/* Select PWM Special Event Trigger Output Postscale value to 1:1 */

PWM1CON2bits.SEVOPS = 0b0000;

/* Assign special event compare value */

P1SECMPbits.SEVTCMP = 100;

/* Choose ADC1 trigger source such that MCPWM module stops sampling and */
/* starts conversion */

AD1CON1bits.SSRC = 0b011;
```

47.14.2.1 SPECIAL EVENT TRIGGER ENABLE

The PWM module always produces the Special Event Trigger signal. This signal may optionally be used by the A/D Converter module. Refer to **Section 17. “10-Bit A/D Converter”** in the *“PIC24F Family Reference Manual”* for more information on using the Special Event Trigger.

47.14.2.2 SPECIAL EVENT TRIGGER POSTSCALER

The PWM Special Event Trigger has a postscaler that allows a 1:1 to 1:16 postscale ratio. The postscaler is useful when synchronized A/D conversions do not need to be performed during every PWM cycle. The postscaler is configured by writing the PWM Special Event Trigger Output Postscale Select (SEVOPS) control bits in the PWM Control Register 2 (PWMxCON2<11:8>) SFR.

The special event output postscaler is cleared on the following events:

- Any write to the Special Event Compare (PxSECMP) register
- Any device Reset

47.14.3 PWM Update Lockout

In some applications, it is important that all duty cycle and period registers be written before the new values take effect. The update disable feature allows the user application to specify when new duty cycle and period values can be used by the module. The PWM update lockout feature is enabled by setting the PWM Update Disable (UDIS) bit in the PWM Control Register 2 (PWMxCON2<0>) SFR.

The UDIS bit affects all duty cycle registers, PxDC3:PxDC1, and the PWM time base period buffer, PxTPER. To execute an update lockout, perform the following steps:

- Set the UDIS bit
- Write all duty cycle registers and PxTPER, if applicable
- Clear the UDIS bit to re-enable updates

Note: Immediate updates must be disabled (IUE = 0) to use the PWM update lockout feature.
--

47.14.4 Write-Protected Registers

If the PWMLOCK input signal is asserted (PWMLOCK = 1), the PWMxCON1, PxFLTACON and PxFLTBCON registers are write-protected. To gain write access to these locked registers, the user must write two consecutive values (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the PWM1CON1, PxFLTACON or PxFLTBCON registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access.

To write to all registers, the PWMxCON1, PxFLTACON and PxFLTBCON registers require three unlock operations.

If the PWMLOCK input signal is deasserted (PWMLOCK = 0), the PWMKEY functionality is disabled, and the PWMxCON1, PxFLTACON and PxFLTBCON registers may be written without restrictions.

47.15 OPERATION IN POWER-SAVING MODES

47.15.1 PWM Operation in Sleep Mode

When the device enters Sleep mode, the system clock is disabled. Since the clock for the PWM time base is derived from the system clock source (Tcy), that clock will also be disabled. All enabled PWM output pins will be frozen in the output states that were in effect prior to entering Sleep mode.

If the PWM module is used to control a load in a power application, the PWM module outputs must be placed into a safe state before executing the `PWRSV` instruction. Depending on the application, the load may begin to consume excessive current when the PWM outputs are frozen in a particular output state. For example, the `PxOVDCON` register can be used to manually turn off the PWM output pins, as shown in Example 47-9.

Example 47-9: Manually Placing PWM Pins Into an Inactive State

```
; This code example drives all PWM pins to the inactive state
; before executing the PWRSV instruction.

CLR          P1OVDCON      ; Force all PWM outputs inactive
PWRSV        #0            ; Put the device in Sleep mode
SETM.B       P1OVDCONH     ; Set the POVD bits when the device wakes up
```

The Fault A and Fault B input pins, if enabled to control the PWM pins via the `PxFLTACON` and `PxFLTBCON` registers, continue to function normally when the device is in Sleep mode. If one of the Fault pins is driven low while the device is in Sleep mode, the PWM outputs are driven to the programmed Fault states in the `PxFLTACON` and `PxFLTBCON` registers.

The Fault input pins can also wake the CPU from Sleep mode. If the Fault interrupt enable bit is set (`FLTxAIE = 1` or `FLTxBIE = 1`), the device will wake from Sleep mode when the Fault pin is driven low. If the Fault pin interrupt priority is greater than the current CPU priority, program execution starts at the Fault pin interrupt vector location upon wake-up. Otherwise, execution continues from the next instruction following the `PWRSV` instruction.

47.15.2 PWM Operation in Idle Mode

When the device enters Idle mode, the system clock sources remain functional and the CPU stops executing code. The PWM module can optionally continue to operate in Idle mode. The PWM Time Base Stop in Idle Mode (`PTSIDL`) bit in the PWM Time Base Control (`PxTCON<13>`) register determines whether the PWM module stops in Idle mode or continues to operate normally.

If `PTSIDL = 0`, the module operates normally when the device enters Idle mode. The PWM time base interrupt, if enabled, can be used to wake the device from Idle mode. If the PWM Time Base Interrupt Enable (`PTIE`) bit is set (`PTIE = 1`), the device will wake from Idle mode when the PWM time base interrupt is generated. If the PWM time base interrupt priority is greater than the current CPU priority, program execution starts at the PWM interrupt vector location upon wake-up. Otherwise, execution will continue from the next instruction following the `PWRSV` instruction.

If `PTSIDL = 1`, the module stops in Idle mode. If the PWM module is programmed to stop in Idle mode, the operation of the PWM outputs and Fault input pins is the same as the operation in Sleep mode. (See **Section 47.15.1 “PWM Operation in Sleep Mode”** for details.)

47.16 REGISTER MAP

A summary of the registers associated with the PIC24F Family Motor Control PWM module is provided in Table 47-7.

Table 47-7: Registers Associated with 8-Output MCPWM Module

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset
PxTCON	PTEN	—	PTSIDL	—	—	—	—	—	PTOPS<3:0>				PTCKPS<1:0>		PTMOD<1:0>		0000 0000 0000 0000
PxTMR	PTDIR	PWM Time Base Register															0000 0000 0000 0000
PxTPER	—	PWM Time Base Period Register															0111 1111 1111 1111
PxSECMP	SEVTDIR	PWM Special Event Compare Register															0000 0000 0000 0000
PWMxCON1	—	—	—	—	—	PMOD3	PMOD2	PMOD1	—	PEN3H	PEN2H	PEN1H	—	PEN3L	PEN2L	PEN1L	0000 0000 0xxx 0xxx ⁽¹⁾
PWMxCON2	—	—	—	—	SEVOPS<3:0>				—	—	—	—	—	IUE	OSYNC	UDIS	0000 0000 0000 0000
PxDTCON1	DTBPS<1:0>		Dead Time B Value Register						DTAPS<1:0>		Dead Time A Value Register						0000 0000 0000 0000
PxDTCON2	—	—	—	—	—	—	—	—	—	—	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I	0000 0000 0000 0000
PxFLTAON	—	—	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L	FLTAM	—	—	—	—	FAEN3	FAEN2	FAEN1	0000 0000 0000 0xxx ⁽²⁾
PxFLTBCON	—	—	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L	FLTBM	—	—	—	—	FBEN3	FBEN2	FBEN1	0000 0000 0000 0xxx ⁽²⁾
PxOVDCON	—	—	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L	—	—	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L	0011 1111 0000 0000
PxDC1	PWM Duty Cycle 1 Register																0000 0000 0000 0000
PxDC2	PWM Duty Cycle 2 Register																0000 0000 0000 0000
PxDC3	PWM Duty Cycle 3 Register																0000 0000 0000 0000
PWMKEY ⁽³⁾	PWMLOCK<15:0>																0000 0000 0000 0000

Legend: — = unimplemented, read as '0'; x = bit is unknown

- Note 1:** The Reset condition of the PEN3H:PEN1H and PEN3L:PEN1L bits depends on the value of the PWMPIN Configuration bit in the FPOR Device Configuration register. When PWMPIN is set to '0', Reset values are '1' and when PWMPIN is set to '1', Reset values are '0'.
- Note 2:** In devices where the PWMLOCK bit is present in the FOSCSEL Configuration register, the Reset value for the FAEN<3:1> and FBEN<3:1> bits is '1' when PWMLOCK is set to '1'. In all other configurations, the Reset value for these bits is '0'. Refer to the specific device data sheet for further details.
- Note 3:** This register is implemented only in devices where the PWMLOCK bit is present in the FOSCSEL Configuration register. Refer to the specific device data sheet for availability.

47.17 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Motor Control PWM module include the following:

Title	Application Note #
Using the dsPIC30F for Sensorless BLDC Control	AN901
Using the dsPIC30F for Vector Control of an ACIM	AN908
Sensored BLDC Motor Control Using dsPIC30F2010	AN957
An Introduction to AC Induction Motor Control Using the dsPIC30F MCU	AN984
Sinusoidal Control of PMSM Motors with dsPIC30F DSC	AN1017
Sensorless Field Oriented Control of a PMSM	AN1078
Sensorless BLDC Control With Back-EMF Filtering	AN1083
Power Factor Correction in Power Conversion Applications Using the dsPIC [®] DSC	AN1106
Sensorless BLDC Control with Back-EMF Filtering Using a Majority Function	AN1160
Sensorless Field Oriented Control (FOC) of an AC Induction Motor (ACIM)	AN1162
Sensorless Field Oriented Control (FOC) of an AC Induction Motor (ACIM) Using Field Awakening	AN1206
Integrated Power Factor Correction (PFC) and Sensorless Field Oriented Control (FOC) System	AN1208
Stepper Motor Control with dsPIC [®] DSCs	AN1307
Getting Started with the BLDC Motors and dsPIC30F Devices	GS001
Measuring Speed and Position with the QEI Module	GS002
Driving ACIM with the dsPIC DSC MCPWM Module	GS004
Using the dsPIC30F Sensorless Motor Tuning Interface	GS005

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

47.18 REVISION HISTORY

Revision A (June 2010)

This is the initial released revision of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Octopus, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICTail, REAL ICE, rLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2010, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-60932-335-6

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta

Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland

Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara

Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto

Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office

Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney

Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu

Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing

Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR

Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing

Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao

Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan

Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian

Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen

Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai

Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore

Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi

Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune

Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama

Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu

Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul

Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang

Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila

Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore

Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung

Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei

Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels

Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich

Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen

Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid

Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham

Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/05/10