Section 42. Enhanced Parallel Master Port (EPMP)

HIGHLIGHTS

This section of the manual contains the following major topics:

42.1 INTRODUCTION

The Enhanced Parallel Master Port (EPMP) provides a parallel 4-bit (Master mode only), 8-bit (Master and Slave modes) or 16-bit (Master mode only) data bus interface to communicate with off-chip modules such as memories, FIFOs, LCD controllers and other microcontrollers (see **Section 42.7 "Application Examples"**). This module can serve as either the master or the slave on the communication bus.

The access to the EPMP is done through Extended Data Space (EDS). For more information, refer to the PIC24F family reference manual, **Section 45. "Data Memory with Extended Data Space"**.

The Instruction Cycle Period (TCY) and Alternative Master Cycle Period (TAM) definitions are used in this document. The TCY is a minimum time required by the CPU to perform an instruction. The TAM is a period of the synchronization used to generate the EPMP interface signals if the Alternate Master (such as graphics module) controls the EPMP I/Os directly (refer to **Section 43. "Graphics Controller Module (GFX)"** for more details).

Key features of the EPMP module are:

- Extended Data Space (EDS) interface allows direct addressing from the CPU
- Up to 23 Programmable Address Lines
- Up to 2 Chip Select Lines
- Up to 2 Acknowledgement Lines (one per chip select)
- 4-bit, 8-bit or 16-bit wide Data Bus
- Programmable Strobe Options (per chip select):
  - Individual Read and Write Strobes, or
  - Read/$\overline{\text{Write}}$ Strobe with Enable Strobe
- Programmable Address/Data Multiplexing
- Programmable Address Wait States
- Programmable Data Wait States (per chip select)
- Programmable Polarity on Control Signals (per chip select)
- Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support
  - Address support
  - 4 bytes-deep, auto-incrementing buffer
- Alternate Master features (select devices only, refer to the specific device data sheet)

Table 42-1 lists the pin names with their descriptions.

Table 42-1: Parallel Master Port Pin Description

Pin Name	Type	Description
PMA<22:16>	O	Address bus bits 22-16
PMA<15>, PMCS2	O	Address bus bit 15
	O	Chip Select 2 (alternate location, see **Section 42.4.1.1 "Chip Selects"** for details)
	I/O	Data bus bit 15 when port size is 16-bit and address is multiplexed
PMA<14>, PMCS1	O	Address bus bit 14
	O	Chip Select 1 (alternate location, see **Section 42.4.1.1 "Chip Selects"** for details)
	I/O	Data bus bit 14 when port size is 16-bit and address is multiplexed
PMA<13:8>	O	Address bus bits 13-8
	I/O	Data bus bits 13-8 when port size is 16-bit and address is multiplexed
PMA<7:3>	O	Address bus bits 7-3
PMA<2>, PMALU	O	Address bus bit 2
	O	Address latch-upper strobe for multiplexed address
PMA<1>, PMALH	O	Address bus bit 1
	O	Address latch-high strobe for multiplexed address
PMA<0>, PMALL	O	Address bus bit 0
	O	Address latch-low strobe for multiplexed address
PMD<15:8>	I/O	Data bus bits 15-8 when address is not multiplexed
PMD<7:4>	I/O	Data bus bits 7-4
	O	Address bus bits 7-4 when port size is 4-bit and address is multiplexed with 1 address phase
PMD<3:0>	I/O	Data bus bits 3-0
PMCS1	O	Chip Select 1
PMCS2	O	Chip Select 2
PMWR, PMENB	O	Write strobe or Enable signal depending on Strobe mode
PMRD, PMRD/$\overline{\text{PMWR}}$	O	Read strobe or Read/$\overline{\text{Write}}$ signal depending on Strobe mode
PMBE1	O	Byte indicator (see **Section 42.4.1.9 "Data Port Size"** for details)
PMBE0	O	Nibble or byte indicator (see **Section 42.4.1.9 "Data Port Size"** for details)
PMACK2	I	Acknowledgment 2
PMACK1	I	Acknowledgment 1
Legend: I = Input O = Output		

42.2 EPMP MODULE REGISTERS

The EPMP module uses these Special Function Registers (SFRs):

- PMCON1
- PMCON2
- PMCON3
- PMCON4
- PMCS1CF and PMCS2CF
- PMCS1MD and PMCS2MD
- PMCS1BS and PMCS2BS
- PMDOUT1 and PMDOUT2
- PMDIN1 and PMDIN2
- PMSTAT

42.2.1 PMCON1 Register

The EPMP Control Register 1 (Register 42-1) contains the bits that control much of the module's basic functionality. A key bit is PMPEN, which is used to reset the module and enable or disable the module. When the module is disabled, all the associated I/O pins return to their designated I/O function. In addition, any read or write operations, active or pending, are stopped and the BUSY bit in PMCON2 is cleared. The data within the module registers are retained, including PMSTAT. Thus, the module could be disabled after a reception, and the last received data and status would still be available for processing. When the module is enabled, the buffer control logic is reset along with PMSTAT.

This register allows Master/Slave mode selection, and configuration options for both modes. All other bits in the PMCON1 register control address multiplexing, chip select signals configuration, address latch signals polarity, bus keeper functionality and Interrupt Request mode. These are discussed more in detail in **Section 42.4.1 "Parallel Master Port Configuration Options"**.

42.2.2 PMCON2 Register

The EPMP Control Register 2 (Register 42-2) contains bits that control the operational modes for an Alternate Master, such as a graphics subsystem. It also contains the universal status flag, BUSY, used in Master modes to indicate that an operation by the module is in progress. Low byte of this register contains the EDS end address for Chip Select 2.

Refer to **Section 42.5 "Alternate Master"**, for details on the use of the PMCON2 register.

42.2.3 PMCON3 and PMCON4 Registers

The EPMP Control Registers 3 and 4 (Register 42-3 and Register 42-4) enable various port control and address signals controls associated with this module. Setting these bits allocates the corresponding microcontroller pins to the EPMP module; clearing the bits allocates the pins to port I/O or other peripheral modules associated with the pins. Also, PMCON3 register contains Wait states bits for the address latch strobes.

42.2.4 PMCS1CF and PMCS2CF Registers

The EPMP Chip Select Configuration Registers (Register 42-5) contain bits that select control signal polarity, data bus size and strobe mode for chip select configurations.

42.2.5 PMCS1BS and PMCS2BS Registers

The EPMP Chip Select Base Registers (Register 42-6) contain the start addresses for the address range of each chip select within EDS.

42.2.6 PMCS1MD and PMCS2MD Registers

The EPMP Chip Select Mode Registers (Register 42-7) contain bits that control the operational modes of the module.

Details on the use of the PMCSxMD bits to configure EPMP operation are provided in **Section 42.4 "Master Port Modes".**

42.2.7 PMDOUT1 and PMDOUT2 Registers

The EPMP Data Output 1 and Data Output 2 Registers are used only in Slave mode for buffered output data. These registers act as a buffer for outgoing data. Refer to **Section 42.3.2 "Buffered Parallel Slave Port (PSP) Mode"** for information on their operation.

42.2.8 PMDIN1 and PMDIN2 Registers

The EPMP Data Input 1 and Data Input 2 Registers are used in Slave modes to buffer incoming data. These registers hold data that are asynchronously clocked in. Refer to **Section 42.3.2 "Buffered Parallel Slave Port (PSP) Mode"** for information on their operation.

In Master mode, PMDIN1 is the holding register for incoming data. Refer to **Section 42.4.2 "Read Operation"** for more information on its operation in Master mode.

42.2.9 PMSTAT Register

The EPMP Status Register (Register 42-8) contains status bits associated with buffered operating modes when the port is functioning as a slave port. This includes the overflow, underflow and full flag bits. Refer to **Section 42.3.2 "Buffered Parallel Slave Port (PSP) Mode"** for more information on these flags.

42.2.10 Additional Registers

In addition to the EPMP-specific registers, the PADCFG1 register also affects the configuration of the EPMP module. The PMPTTL bit (PADCFG1<0>) allows users to select between TTL and Schmitt Trigger (ST) digital input buffers for greater compatibility with external circuits. Setting PMPTTL selects TTL input buffers; the default configuration is ST buffers. The PADCFG1 register is also described in **Section 29. "Real-Time Clock and Calendar (RTCC)"**.

Also to enable the EPMP interrupts the PMPIE bit in IEC2 register must be set. The EPMP interrupt flag PMPIF is located in IFS2 register. After the interrupt is processed, the flag must be cleared by the software. Refer to **Section 8. "Interrupts"** for more information.

Register 42-1: PMCON1: EPMP Control Register 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	—	MODE1	MODE0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n – Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15 **PMPEN:** Enhanced Parallel Master Port Enable bit
1 = EPMP enabled
0 = EPMP disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX1:ADRMUX0:** Address/Data Multiplexing Selection bits
11 = Lower address bits are multiplexed with data bits using 3 address phases
10 = Lower address bits are multiplexed with data bits using 2 address phases
01 = Lower address bits are multiplexed with data bits using 1 address phase
00 = Address and data appear on separate pins

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **MODE1:MODE0:** Parallel Port Mode Select bits
11 = Master mode
10 = Enhanced PSP; pins used are PMRD, PMWR, PMCS1, PMD<7:0> and PMA<1:0>
01 = Buffered PSP; pins used are PMRD, PMWR, PMCS1 and PMD<7:0>
00 = Legacy Parallel Slave Port; PMRD, PMWR, PMCS1 and PMD<7:0> pins are used

bit 7-6 **CSF1:CSF0:** Chip Select Function bits
11 = Reserved
10 = PMA<15> used as Chip Select 2, PMA<14> used as Chip Select 1
01 = PMA<15> used as Chip Select 2, PMCS1 used as Chip Select 1
00 = PMCS2 used as Chip Select 2, PMCS1 used as Chip Select 1

bit 5 **ALP:** Address Latch Polarity bit
1 = Active-high ($\overline{\text{PMALL}}$, $\overline{\text{PMALH}}$ and $\overline{\text{PMALU}}$)
0 = Active-low (PMALL, PMALH and PMALU)

bit 4 **ALMODE:** Address Latch Strobe Mode bit
1 = Enable "smart" address strobes (each address phase is only present if the current access would cause a different address in the latch than the previous address)
0 = Disable "smart" address strobes

bit 3 **Unimplemented:** Read as '0'

bit 2 **BUSKEEP:** Bus Keeper bit
1 = Data bus keep their last value when not actively being driven
0 = Data bus is in high-impedance state when not actively being driven

bit 1-0 **IRQM1:IRQM0:** Interrupt Request Mode bits
11 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)
10 = Reserved
01 = Interrupt generated at the end of read/write cycle
00 = No Interrupt generated

Register 42-2: PMCON2: EPMP Control Register 2

R-0	U-0	R/C-0	R/C-0	R-0	R-1	R/W-0	R/W-0
BUSY	—	ERROR	TIMEOUT	AMREQ(1)	CURMST(1)	MSTSEL1(1)	MSTSEL0(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RADDR23	RADDR22	RADDR21	RADDR20	RADDR19	RADDR18	RADDR17	RADDR16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	C = Clearable bit
-n – Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15 **BUSY:** Busy bit (Master mode only)
1 = Port is busy
0 = Port is not busy

bit 14 **Unimplemented:** Read as '0'

bit 13 **ERROR:** Error bit
1 = Transaction error (illegal transaction was requested)
0 = Transaction completed successfully

bit 12 **TIMEOUT:** Time-Out bit
1 = Transaction timed out
0 = Transaction completed successfully

bit 11 **AMREQ:** Alternate Master Request bit(1)
1 = The Alternate Master is requesting use of EPMP
0 = The Alternate Master is not requesting use of EPMP

bit 10 **CURMST:** Current Master bit(1)
1 = EPMP access is granted to CPU
0 = EPMP access is granted to Alternate Master

bit 9-8 **MSTSEL1:MSTSEL0:** Enhanced Parallel Port Master Select bits(1)
11 = Alternate Master I/Os direct access (EPMP bypass mode)
10 = Reserved
01 = Alternate Master
00 = CPU

bit 7-0 **RADDR23:RADDR16:** Enhanced Parallel Master Port Reserved Address Space bits(2,3)

Note 1: These bits are unimplemented in devices that do not support Alternate Master operation. See **Section 42.5 "Alternate Master"** for more information.
2: If RADDR<23:16> = 00h, the last EDS address for the Chip Select 2 will be FFFFFFh. For the address range to be accessible, RADDR<23:16> must be greater than PMCS2BS<23:16>
3: Reserved Address Space is limited in some devices. The limit is dictated by the available address lines on the Enhanced Parallel Master Port.

Register 42-3: PMCON3: EPMP Control Register 3

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTWREN	PTRDEN	PTBE1EN	PTBE0EN	—	AWAITM1	AWAITM0	AWAITE
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PTEN22	PTEN21	PTEN20	PTEN19	PTEN18	PTEN17	PTEN16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n – Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15 **PTWREN:** Write/Enable Strobe Port Enable bit
1 = PMWR/PMENB port enabled
0 = PMWR/PMENB port disabled

bit 14 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/$\overline{\text{PMWR}}$ port enabled
0 = PMRD/$\overline{\text{PMWR}}$ port disabled

bit 13 **PTBE1EN:** High Nibble/Byte Enable Port Enable bit
1 = PMBE1 port enabled
0 = PMBE1 port disabled

bit 12 **PTBE0EN:** Low Nibble/Byte Enable Port Enable bit
1 = PMBE0 port enabled
0 = PMBE0 port disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-9 **AWAITM1:AWAITM0:** Address Latch Strobe Wait States bits
11 = Wait of 3½ TCY
10 = Wait of 2½ TCY
01 = Wait of 1½ TCY
00 = Wait of ½ TCY

bit 8 **AWAITE:** Address Hold After Address Latch Strobe Wait States bits
1 = Wait of 1¼ TCY
0 = Wait of ¼ TCY

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **PTEN22:PTEN16:** EPMP Address Port Enable bits
1 = PMA<22:16> function as EPMP address lines
0 = PMA<22:16> function as port I/Os

Register 42-4: PMCON4: EPMP Control Register 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n – Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15 **PTEN15:** PMA15 Port Enable bit
1 = PMA15 functions as either address line 15 or Chip Select 2
0 = PMA15 functions as port I/O

bit 14 **PTEN14:** PMA14 Port Enable bit
1 = PMA14 functions as either address line 14 or Chip Select 1
0 = PMA14 functions as port I/O

bit 13-3 **PTEN13:PTEN3:** EPMP Address Port Enable bits
1 = PMA<13:3> function as EPMP address lines
0 = PMA<13:3> function as port I/Os

bit 2-0 **PTEN2:PTEN0:** PMALU/PMALH/PMALL Strobe Enable bits
1 = PMA<2:0> function as either address lines or address latch strobes
0 = PMA<2:0> function as port I/Os

Register 42-5: PMCSxCF: Chip Select x Configuration Registers

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
CSDIS(1)	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
ACKP	PTSZ1	PTSZ0	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n – Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15 **CSDIS:** Chip Select x Disable bit(1)
1 = Disable the Chip Select x functionality
0 = Enable the Chip Select x functionality

bit 14 **CSP:** Chip Select x Polarity bit
1 = Active-high (PMCSx)
0 = Active-low ($\overline{\text{PMCSx}}$)

bit 13 **CSPTEN:** PMCSx Port Enable bit
1 = PMCSx port enabled
0 = PMCSx port disabled

bit 12 **BEP:** Chip Select x Nibble/Byte Enable Polarity bit
1 = Nibble/Byte enable active-high (PMBE0, PMBE1)
0 = Nibble/Byte enable active-low ($\overline{\text{PMBE0}}$, $\overline{\text{PMBE1}}$)

bit 11 **Unimplemented:** Read as '0'

bit 10 **WRSP:** Chip Select x Write Strobe Polarity bit
For Slave modes and Master mode when SM = 0
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Master mode when SM = 1
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 9 **RDSP:** Chip Select x Read Strobe Polarity bit
For Slave modes and Master mode when SM = 0
1 = Read strobe active-high (PMRD)
0 = Read strobe active-low ($\overline{\text{PMRD}}$)
For Master mode when SM = 1
1 = Read/Write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/Write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

bit 8 **SM:** Chip Select x Strobe Mode bit
1 = Read/Write and Enable strobes (PMRD/$\overline{\text{PMWR}}$ and PMENB)
0 = Read and Write strobes (PMRD and PMWR)

bit 7 **ACKP:** Chip Select x Acknowledge Polarity bit
1 = ACK active-high (PMACKx)
0 = ACK active-low ($\overline{\text{PMACKx}}$)

Note 1: In some PIC24F family devices, dedicated EPMP Chip Select signals are not available. Instead, the Chip Select signals are mapped to the most significant address lines and can be optionally enabled through the CSF<1:0> bits (PMCON1<7:6>).

Register 42-5: PMCSxCF: Chip Select x Configuration Registers (Continued)

bit 6-5 **PTSZ1:PTSZ0:** Chip Select x Port Size bits
11 = Reserved
10 = 16-bit Port Size (PMD<15:0>)
01 = 4-bit Port Size (PMD<3:0>)
00 = 8-bit Port Size (PMD<7:0>)

bit 4-0 **Unimplemented:** Read as '0'

Note 1: In some PIC24F family devices, dedicated EPMP Chip Select signals are not available. Instead, the Chip Select signals are mapped to the most significant address lines and can be optionally enabled through the CSF<1:0> bits (PMCON1<7:6>).

Register 42-6: PMCSxBS: Chip Select x Base Address Registers

R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
BASE23(2)	BASE22(2)	BASE21(2)	BASE20(2)	BASE19(2)	BASE18(2)	BASE17(2)	BASE16(2)
bit 15							bit 8

R/W(1)	U-0	U-0	U-0	R/W(1)	U-0	U-0	U-0
BASE15(2)	—	—	—	BASE11(2)	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n – Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15-7 **BASE23:BASE15:** Chip Select x Base Address bits(2)

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **BASE11:** Chip Select x Base Address bit(2)

bit 2-0 **Unimplemented:** Read as '0'

Note 1: Refer to the specific device data sheet for the default Reset values.
2: If the whole PMCS2BS register is written together as 0x0000 then the last EDS address for the Chip Select 1 will be 0xFFFFFF. In this case the Chip Select 2 must not be used. PMCS1BS has no such feature.

Register 42-7: PMCSxMD: Chip Select x Mode Registers

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n – Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15-14 **ACKM1:ACKM0:** Chip Select x Acknowledge Mode bits
11 = Reserved
10 = PMACKx used to determine when a read/write operation is complete
01 = PMACKx used to determine when a read/write operation is complete with time-out
If DWAITM<3:0> = 0, the maximum time-out is 255 TCY, otherwise, the maximum time-out is DWAITM<3:0> number cycles.
00 = PMACKx is not used

bit 13-11 **AMWAIT2:AMWAIT0:** Chip Select x Alternate Master Wait States bits
111 = Wait of 10 Alternate Master cycles
.
.
.
001 = Wait of 4 Alternate Master cycles
000 = Wait of 3 Alternate Master cycles

bit 10-8 **Unimplemented:** Read as '0'

bit 7-6 **DWAITB1:DWAITB0:** Chip Select x Data Setup Before Read/Write Strobe Wait States bits
11 = Wait of 3¼ TCY
10 = Wait of 2¼ TCY
01 = Wait of 1¼ TCY
00 = Wait of ¼ TCY

bit 5-2 **DWAITM3:DWAITM0:** Chip Select x Data Read/Write Strobe Wait States bits
For Write operations:
1111 = Wait of 15½ TCY
.
.
.
0001 = Wait of 1½ TCY
0000 = Wait of ½ TCY

For Read operations:
1111 = Wait of 15¾ TCY
.
.
.
0001 = Wait of 1¾ TCY
0000 = Wait of ¾ TCY

Register 42-7: PMCSxMD: Chip Select x Mode Registers (Continued)

bit 1-0 **DWAITE1:DWAITE0:** Chip Select x Data Hold After Read/Write Strobe Wait States bits

For Write operations:

11 = Wait of 3¼ TCY
10 = Wait of 2¼ TCY
01 = Wait of 1¼ TCY
00 = Wait of ¼ TCY

For Read operations:

11 = Wait of 3 TCY
10 = Wait of 2 TCY
01 = Wait of 1 TCY
00 = Wait of 0 TCY

Register 42-8: PMSTAT: EPMP Status Register (Slave mode only)

R-0	R/W-0 HS	U-0	U-0	R-0	R-0	R-0	R-0
IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
bit 15							bit 8

R-1	R/W-0 HS	U-0	U-0	R-1	R-1	R-1	R-1
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend:	HS = Hardware Set bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n – Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable input buffer registers are full
0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full input register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer x Status Full bit
1 = Input buffer contains unread data (reading buffer will clear this bit)
0 = Input buffer does not contain unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable output buffer registers are empty
0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty output register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer x Status Empty bit
1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains untransmitted data

42.3 SLAVE PORT MODES

In Slave mode, the EPMP module provides an 8-bit data bus and all the necessary control signals to operate as a slave parallel device. It is also configurable for operation in Legacy, Buffered and Addressable modes. Slave mode provides several options for a more flexible interface:

- 8-bit data bus
- Address lines (Addressable mode only)
- Control lines (read, write and chip select)
- Selectable polarity on all control lines

To use the EPMP as a slave, the module must be enabled (PMPEN = 1) and the mode must be set to one of the possible Slave modes (MODE<9:8> = 00, 01 or 10). The polarity for PMRD, PMWR and PMCS1 control signals can be selected with CSP, WRSP and RDSP bits in PMCS1CF register. The Slave mode supports only the interface with separate PMRD and PMWR strobes (SM bit in PMCS1CF register is ignored).

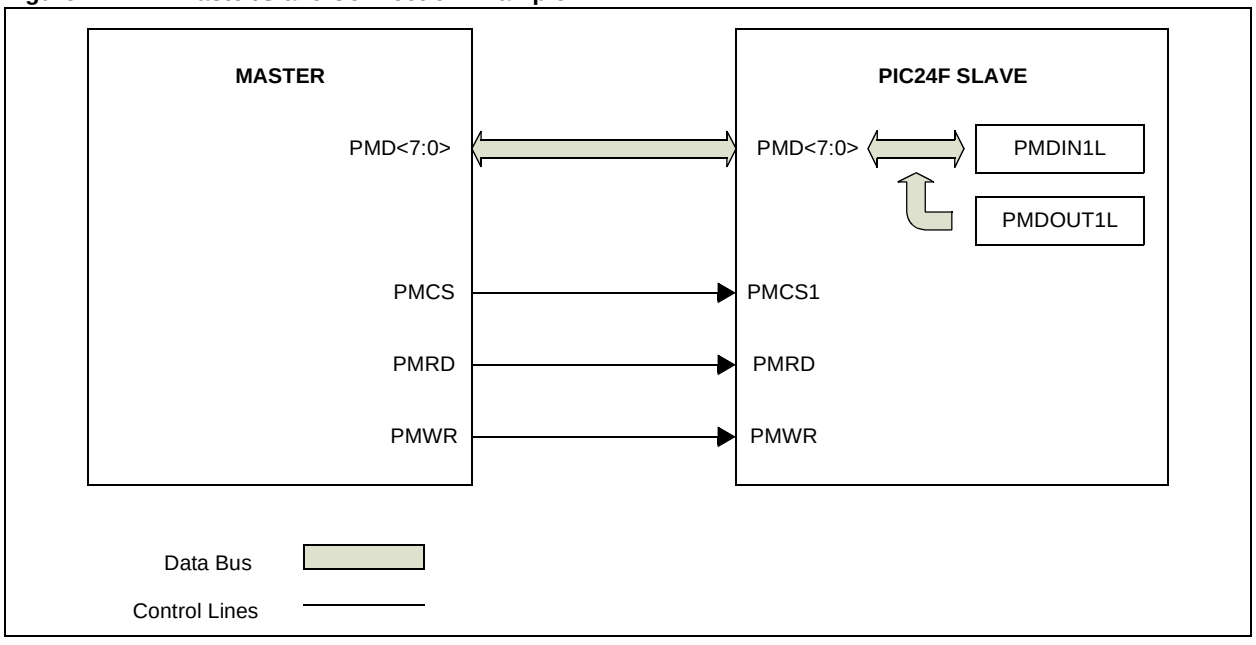
Note: For all control lines (and PMA<1:0> in Addressable PSP mode), the corresponding control bits in the PMCON3 and PMCON4 registers must be configured for parallel port operation. See **Section 42.4.1.2 "Port Pin Control"** for more details.

42.3.1 Legacy Mode

In Legacy mode (MODE<9:8> = 00), the module is configured as a Parallel Slave Port (PSP) with the associated enable module pins dedicated to the module. In this mode, an external device, such as another microcontroller or microprocessor, can asynchronously read and write data using the 8-bit data bus (PMD<7:0>), the read (PMRD), write (PMWR) and Chip Select (PMCS1) inputs.

Note: PMCS1 at PMA14 location is used as the chip select input in all Slave modes. PMCS2 is used only in Master modes.

Figure 42-1: Master/Slave Connection Example

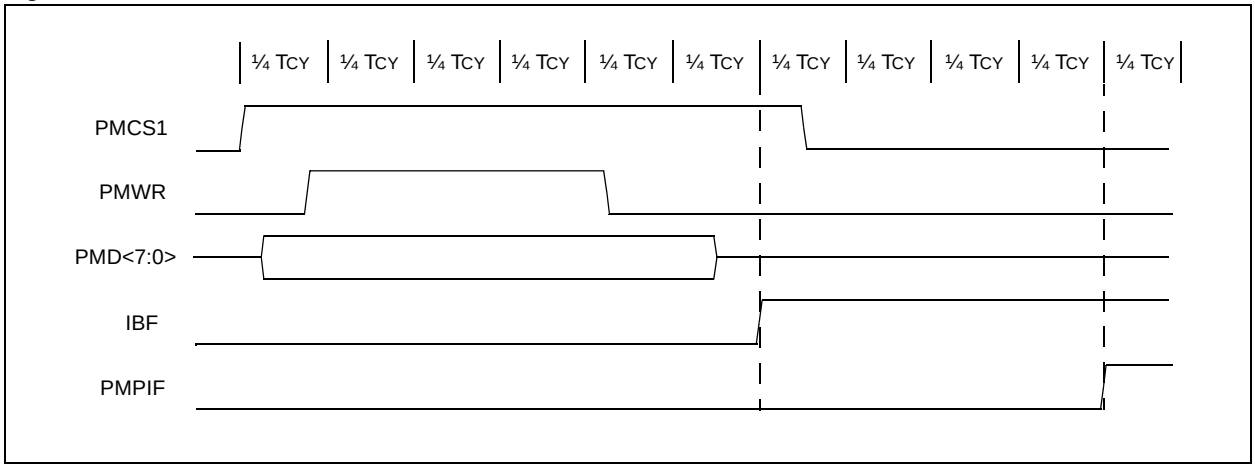


42.3.1.1 WRITE TO SLAVE PORT

When the chip select is active and a write strobe occurs, the data from PMD<7:0> is captured into the lower 8 bits of the PMDIN1 register (PMDIN1<7:0>). The PMPIF and IBF flag bits are set when the write ends.

The timing for the control signals in Write mode is shown in Figure 42-2.

Figure 42-2: Slave Port Write Waveforms

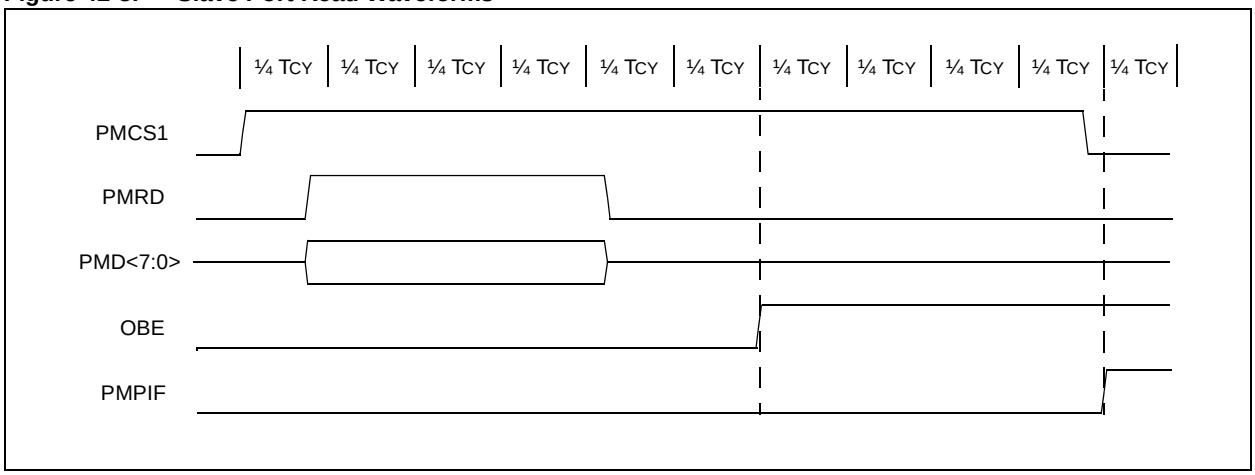


42.3.1.2 READ FROM SLAVE PORT

When chip select is active and a read strobe occurs, the data from the lower 8 bits of the PMDOUT1 register (PMDOUT1<7:0>) is presented onto PMD<7:0>. The data in PMDIN1<7:0> is read out, and the Output Buffer Empty Flag (OBE), is set. If the user writes new data to PMDIN1<7:0> to clear OBE, the data is immediately read out; however, the OBE is not cleared.

The timing for the control signals in Read mode is shown in Figure 42-3.

Figure 42-3: Slave Port Read Waveforms



42.3.1.3 INTERRUPT OPERATION

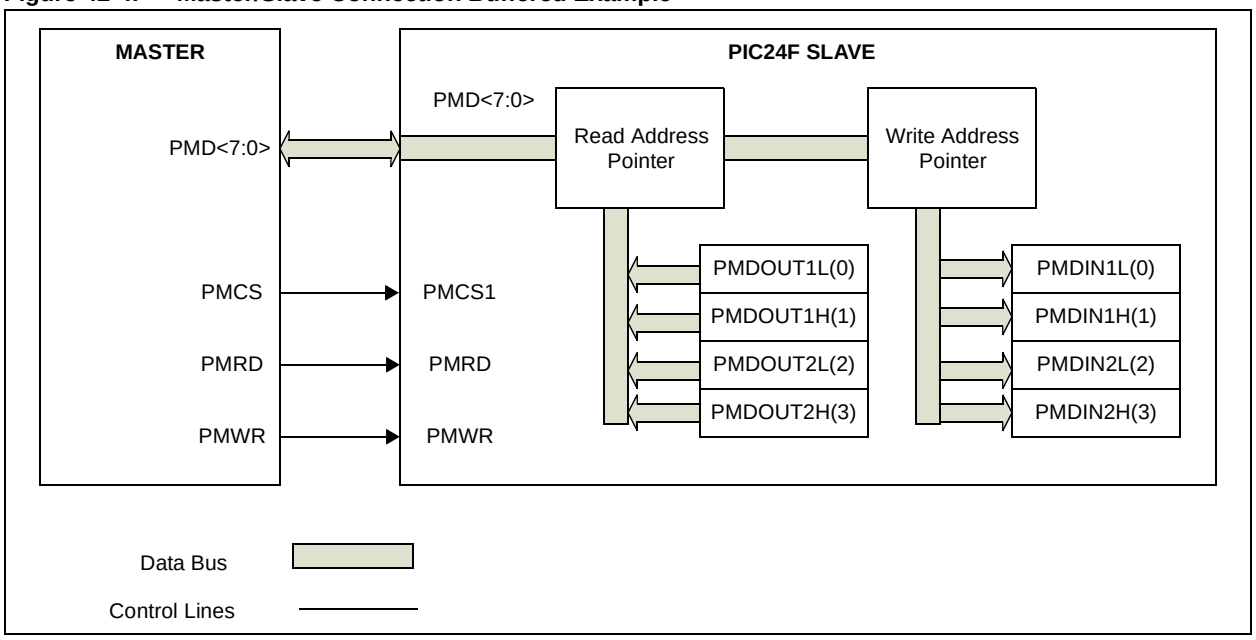
When the read or write operation is completed, the port pins return to the input state and the PMPIF bit is set. User applications should wait for PMPIF to be set before servicing the module. When this happens, the IBF and OBE bits can be polled and the required action taken.

42.3.2 Buffered Parallel Slave Port (PSP) Mode

Buffered Parallel Slave Port mode is functionally identical to the Legacy Parallel Slave Port mode with one exception – the implementation of 4-level read and write buffers. Buffered PSP mode is enabled by setting the MODE<1:0> bits (PMCON1<9:8>) to 01.

When the Buffered mode is active, the module uses the PMDIN1 and PMDIN2 registers as write buffers and the PMDOUT1 and PMDOUT2 registers as read buffers. Each register is split into two single-byte buffer registers, producing separate read and write buffers each 4 bytes deep. Buffers are numbered 0 through 3, starting with the lower byte of PMDIN1 or PMDOUT1 and progressing upward through the high byte of PMDIN2 (PMDOUT2).

Figure 42-4: Master/Slave Connection Buffered Example



42.3.2.1 READ FROM SLAVE PORT

For read operations, the bytes will be sent out sequentially, starting with Buffer 0 (PMDOUT1<7:0>) and ending with Buffer 3 (PMDOUT2<15:8>) for every read strobe. The module maintains an internal pointer to keep track of which buffer is to be read.

Each of the buffers has a corresponding read status bit, OBxE, in the PMSTAT register. This bit is cleared when a buffer contains data that have not been written to the bus, and is set when data is written to the bus. If the current buffer location being read from is empty, a buffer underflow is generated, and the Output Buffer Underflow Flag bit, OBUF (PMSTAT<6>), is set. If all four OBxE status bits are set, then the OBE bit will also be set.

42.3.2.2 WRITE TO SLAVE PORT

For write operations, the data is to be stored sequentially, starting with Buffer 0 (PMDIN1<7:0>) and ending with Buffer 3 (PMDIN2<15:8>). As with read operations, the module maintains an internal pointer to the buffer that is to be written next.

The input buffers have their own write status bits, IBxF. The bit is set when the buffer contains unread incoming data, and cleared when the data have been read. The flag bit is set on the write strobe. If a write occurs on a buffer when its associated IBxF bit is set, the Input Buffer Overflow Flag, IBOV, is set; any incoming data in the buffer will be lost. If all 4 IBxF flags are set, the Input Buffer Full Flag (IBF) is set.

Note:	Byte read from PMDIN1 will clear both IB0F and IB1F flags. Also, byte read from PMDIN2 register will clear IB2F and IB3F flags.

42.3.2.3 INTERRUPT OPERATION

In Buffered Slave mode, the module can be configured to generate an interrupt on every read or write strobe (IRQM<1:0> = 01). It can also be configured to generate an interrupt on a read from Read Buffer 3 or a write to Write Buffer 3 (IRQM<1:0> = 11), which is essentially an interrupt every fourth read or write strobe. When interrupting every fourth byte for input data, all input buffer registers should be read to clear the IBxF flags. If these flags are not cleared, then there is a risk of hitting an overflow condition. The PMSTAT register provides status information on all buffers.

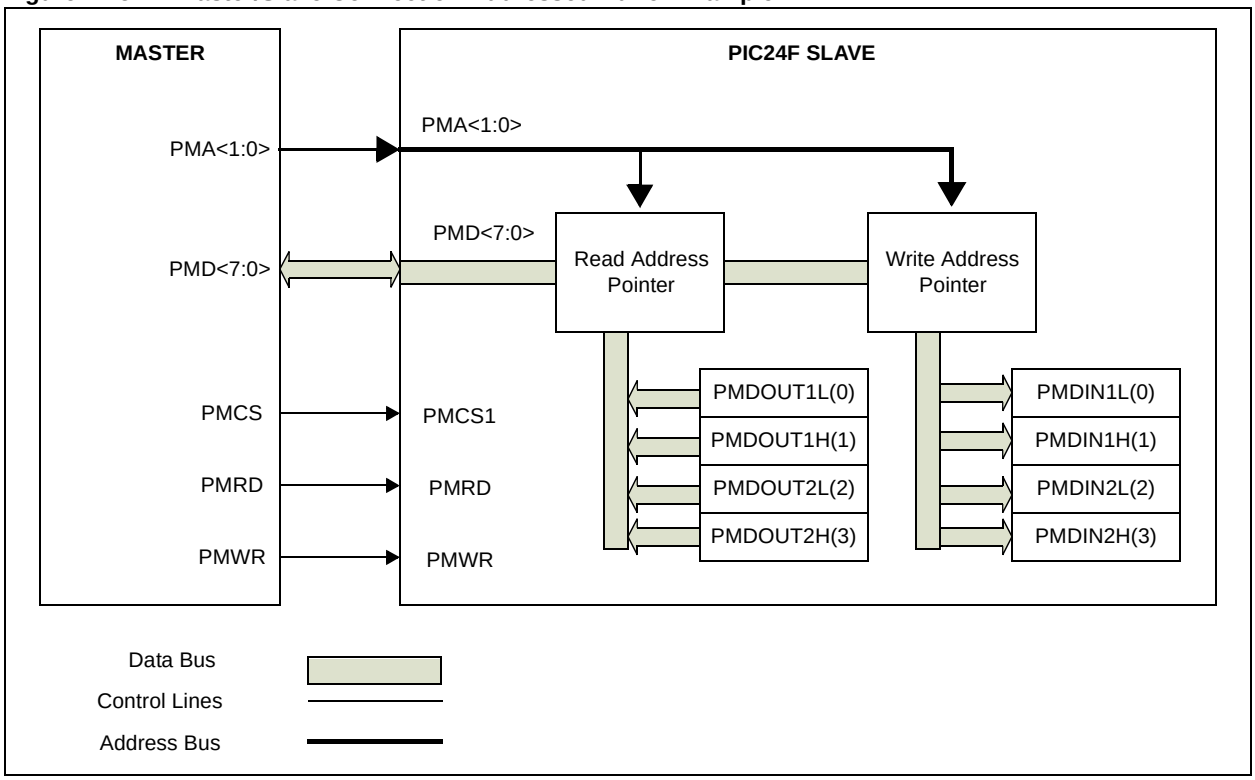
42.3.3 Addressable Parallel Slave Port Mode

In Addressable Parallel Slave Port mode, the module is configured with two extra inputs, PMA<1:0>. This makes the 4-byte buffer space directly addressable as fixed pairs of read and write buffers. The Addressable PSP mode is enabled by setting the MODE<1:0> bits (PMCON1<9:8>) to 10. As with Buffered Legacy mode, data is output from PMDOUT1 and PMDOUT2, and is read in PMDIN1 and PMDIN2. Table 42-2 lists the address resolution for the incoming address to the input and output registers.

Table 42-2: Slave Mode Address Resolution

PMA<1:0>	Output Register (Buffer)	Input Register (Buffer)
00	PMDOUT1<7:0>(0)	PMDIN1<7:0>(0)
01	PMDOUT1<15:8>(1)	PMDIN1<15:8>(1)
10	PMDOUT2<7:0>(2)	PMDIN2<7:0>(2)
11	PMDOUT2<15:8>(3)	PMDIN2<15:8>(3)

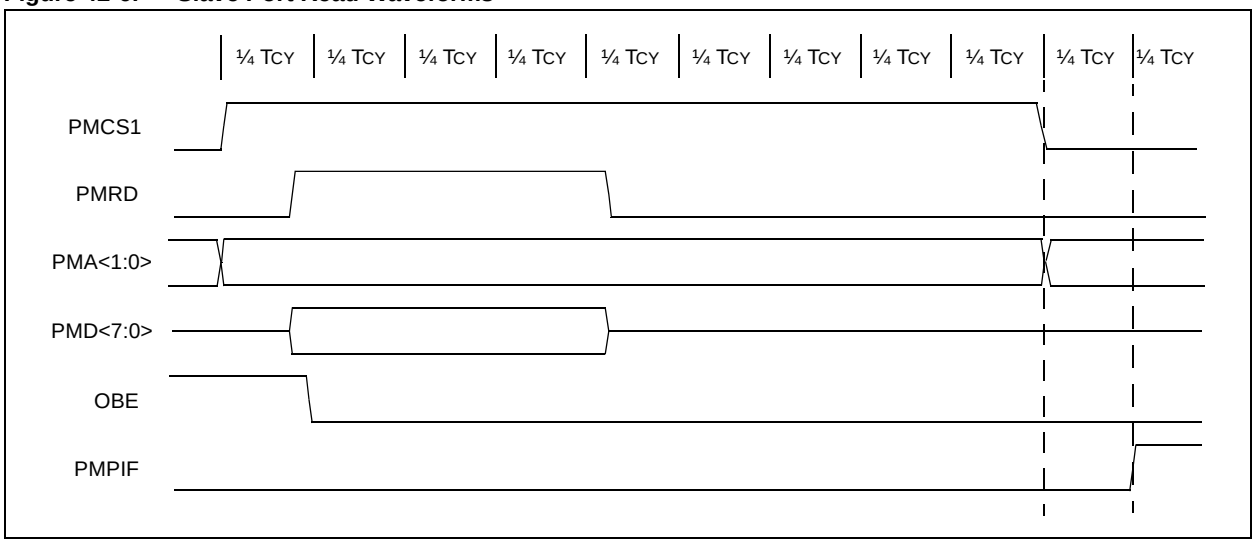
Figure 42-5: Master/Slave Connection Addressed Buffer Example



42.3.3.1 READ FROM SLAVE PORT

When chip select is active and a read strobe occurs, the data from one of the four output bytes is presented onto PMD<7:0>. Which byte is read depends on the 2-bit address placed on PMA<1:0>. Table 42-2 lists the corresponding output registers and their associated addresses. When an output buffer is read, the corresponding OBxE bit is set. The OBE flag bit is set when all the buffers are empty. If any buffer is already empty, OBxE = 1, the next read to that buffer will set the OBUF (PMSTAT<6>) flag.

Figure 42-6: Slave Port Read Waveforms

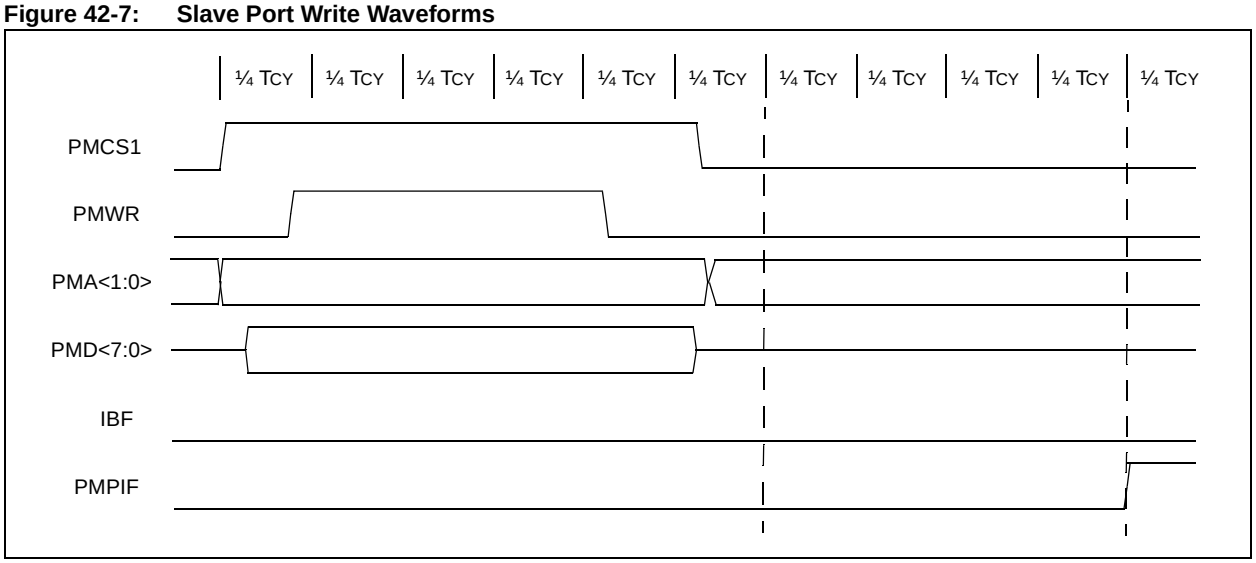


42.3.3.2 WRITE TO SLAVE PORT

When chip select is active and a write strobe occurs, the data from PMD<7:0> is captured into one of the four input buffer bytes. Which byte is written depends on the 2-bit address placed on PMA<1:0>. Table 42-2 lists the corresponding input registers and their associated addresses. When an input buffer is written, the corresponding IBxF bit is set. The IBF flag bit is set when all the buffers are written. If any buffer is already written, IBxF = 1, the next write strobe to that buffer will generate an OBUF event and the byte will be discarded.

Note:	Byte read from PMDIN1 will clear both IB0F and IB1F flags. Also, byte read from PMDIN2 register will clear IB2F and IB3F flags.

Figure 42-7: Slave Port Write Waveforms



42.3.3.3 INTERRUPT OPERATION

In Addressable PSP mode, the module can be configured to generate an interrupt on every read or write strobe. It can also be configured to generate an interrupt on any read from Read Buffer 3 or write to Write Buffer 3; in other words, an interrupt will occur whenever a read or write occurs when the PMA<1:0> pins are 11.

42.4 MASTER PORT MODES

In its Master modes, the EPMP module provides a 4-bit, 8-bit or 16-bit data bus, up to 23 bits of address, and all the necessary control signals to operate a variety of external parallel devices, such as memory devices, peripherals and slave microcontrollers. To use the EPMP as a master, the module must be enabled (PMPEN = 1) and the mode must be set to Master mode (MODE<1:0> = 11).

Because there are a number of parallel devices with a variety of control methods, the EPMP is designed to be extremely flexible to accommodate a range of configurations. Some of these features include:

- 4-bit, 8-bit and 16-bit wide data bus
- Up to 23 selectable address lines
- Up to 2 chip select lines
- Configurable address/data multiplexing
- Selectable polarity on all control lines
- External acknowledgement
- Configurable number of data Wait states on a chip select basis
- Configurable number of address Wait states

42.4.1 Parallel Master Port Configuration Options

42.4.1.1 CHIP SELECTS

Up to two chip select lines, PMCS1 and PMCS2 are available for the Master modes of the EPMP. In some modes, the two chip select lines may be multiplexed with address lines PMA<14> and PMA<15>, respectively, or they may be separate from the address pins. When the chip selects are multiplexed onto the PMA<15> and PMA<14> address pins, it is also necessary to set the PTEN15 and PTEN14 bits (PMPEN2<15:14>) to enable the corresponding chip select. The function of the chip select signals is configured using the Chip Select Function bits, CSF<1:0> (PMCON1 <7:6>).

Note:	The chip selects cannot be mapped to PMA<14> and PMA<15> for modes with 8-bit data bus (PTSZ<1:0)> = 00 (PMCSxCF<6:5>)) and 2 or 3 phases address multiplexing (ADRMUX<1:0> = 10 or 11 (PMCON1<12:11>)).

For EPMP, all external addresses are mapped into the EDS memory. This mapping is done by allocating a region of the EDS memory for each chip select, and then assigning each chip select to a particular external resource, such as a memory or external controller.

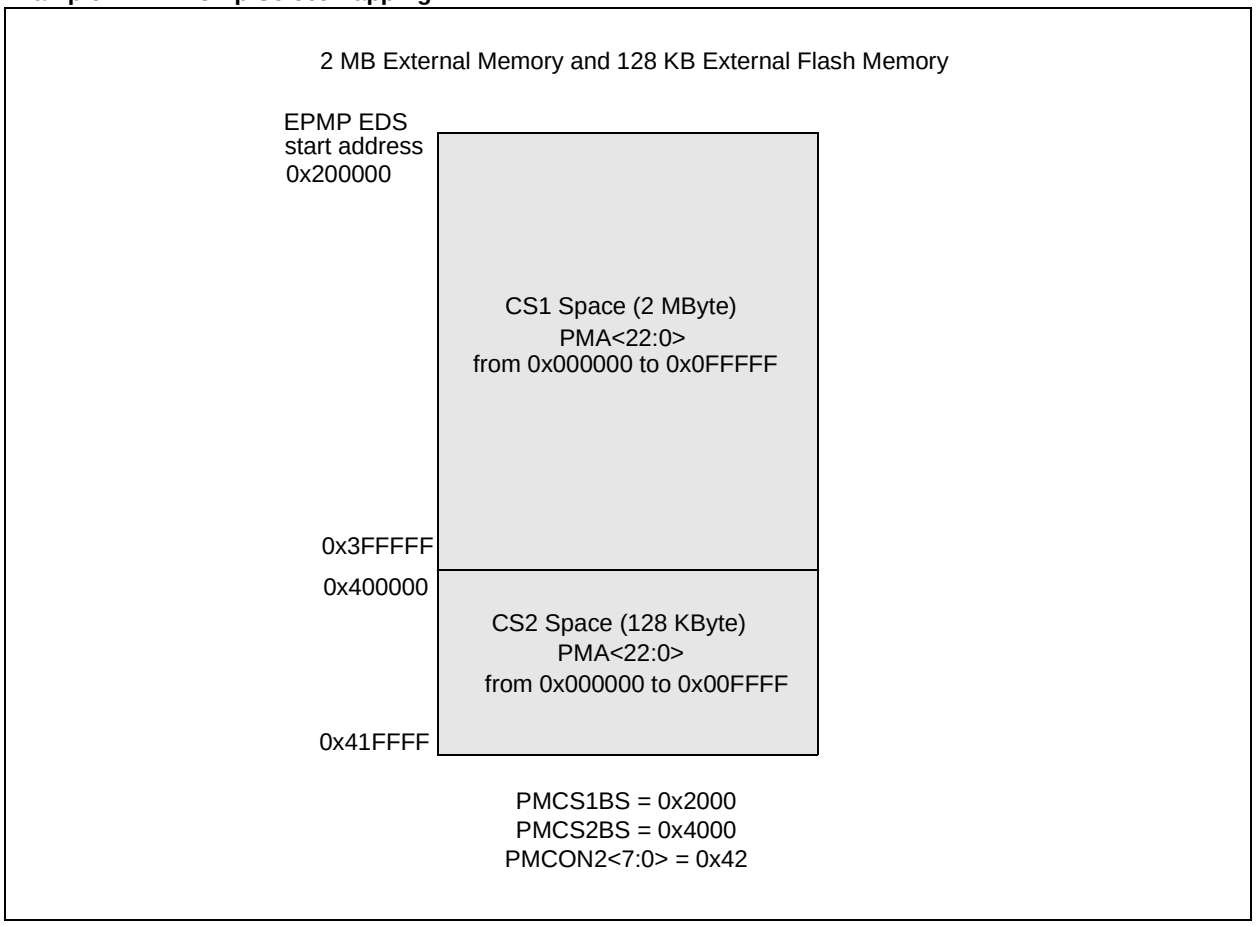
Note:	The region selected for the EPMP should not be used by another device resource such as internal RAM or SFRs.

Within the EDS, the EPMP address range is defined in registers PMCON2, PMCS1BS and PMCS2BS. Chip Select 1 is from the address in PMCS1BS register to the address in PMCS2BS register, Chip Select 2 is from the address in PMCS2BS register to the reserved address (RADDR<23:16>) in PMCON2 register.

Any accesses with addresses that fall outside of this range will have no effect. When all chip selects are disabled (CSDIS = 1 in PMCSxCF registers), all reads and writes from/to the EPMP will be ignored. When PMCS2BS is the same as or smaller than PMCS1BS or address in PMCON2 is the same as or smaller than PMCS2BS, then the corresponding address range no longer exists and the EPMP will not generate transactions for this chip select.

The base address of each chip select (PMCSxBS registers) is subtracted from the EDS address before it is driven out on the external address pins. This ensures that the resource for each chip select always “sees” address 0x000000 at its first address. Example 42-1 shows how to assign chip selects for external resources.

Example 42-1: Chip Select Mapping



42.4.1.2 PORT PIN CONTROL

The CSPTEN (PMCSxCF<13>), PTWREN, PTRDEN, PTBE1EN, PTBE0EN (PMCON3<15:12>) and PTENx bits (PMCON3<7:0>, PMCON4<15:0>) allow the user to conserve EPMP pins for other functions, and allow flexibility to control the external address.

Table 42-3: Port Enable Bits

EPMP Signal	Port Enable Bit	Control Register
PMRD	PTRDEN	PMCON3<14>
PMRD/$\overline{\text{PMWR}}$		
PMWR	PTWREN	PMCON3<15>
PMENB		
PMBE0	PTBE0EN	PMCON3<12>
PMBE1	PTBE1EN	PMCON3<13>
PMCSx	CSPTEN	PMCSxCF<13>
PMALL	PTEN0	PMCON4<0>
PMALH	PTEN1	PMCON4<1>
PMALU	PTEN2	PMCON4<2>
PMACKx	ACKM<1:0> ≠00	PMCSxMD<15:14>
PMAx	PTENx	PMCON3<7:0> and PMCON4<15:0>

When any one of these bits is set, the associated EPMP function is present on its associated pin; when clear, the associated pin returns to its defined I/O port function. For the PMA<22:0> pins, setting the corresponding PTENx bit enables the pin as an address pin. For the pins configured as Chip Select (PMCS1 or PMCS2) with CSPTEN set, the chip select pins drive the inactive state (configured through the CSP bits in PMCSxCF registers) when a read or write operation is not being performed. If the alternate chip select location is selected (CSF<1:0> ≠ 00 in PMCON1 register), then PTEN14 bit for PMCS1, and PTEN15 bit for PMCS2 must be used instead of CSPTEN bits. For the pins configured as address latches, the PTEN0, PTEN1 and PTEN2 bits also control the PMALL, PMALH and PMALU signals. When address multiplexing is used, the associated address latch signals should be enabled. The PMACKx pin is automatically enabled when ACKM = 01 or 10 (PMCSxMD<15:14>).

Note: When the address is multiplexed on 16-bit data bus (PTSZ<1:0> = 10 and ADRMUX<1:0> ≠ 00) PMA<15:8> ports are enabled and drive the data <15:8>. PTEN<15:8> bits have no effect.
In modes where there are unused address lines the corresponding ports have an I/O function and PTENx bits have no effect.
When the address is multiplexed with 1 phase on 4-bit data bus (PTSZ<1:0> = 01 and ADRMUX<1:0> = 01) PMD<7:4> ports are enabled and drive the address <7:4>. PTEN<7:4> bits have no effect.
Enabled EPMP signals will override the corresponding I/Os TRIS registers settings.

42.4.1.3 BUS KEEPER

To provide the lowest possible power consumption in low-power modes, the EPMP provides a Bus Keeper functionality, in which the last driven value on the data bus is kept, instead of letting the bus become high-impedance. This mode can be selected by setting the BUSKEEP bit (PMCON1<2>).

42.4.1.4 READ AND WRITE CONTROL

The EPMP module supports two distinct read/write signaling methods:

- When SM = 0 (PMCSxCF<8>), read and write strobes (PMRD and PMWR) are supplied on separate pins.
- When SM = 1 (PMCSxCF<8>), the read and write strobes are combined into a single control line, PMRD/$\overline{\text{PMWR}}$; a second control line, PMENB, determines when a read or write action is to be taken.

The selection of read/write signaling method and the polarity of the control signals can be done for each chip select separately. Most of the timing diagrams in this document are shown for the mode with the separate Read and Write strobes (PMRD and PMWR). The timing diagrams with Read/$\overline{\text{Write}}$ and Enable signals (PMRD/$\overline{\text{PMWR}}$ and PMENB) are displayed in Figure 42-8 and Figure 42-9.

Figure 42-8: Read/$\overline{\text{Write}}$ and Enable Signals Read Waveforms (SM = 1)

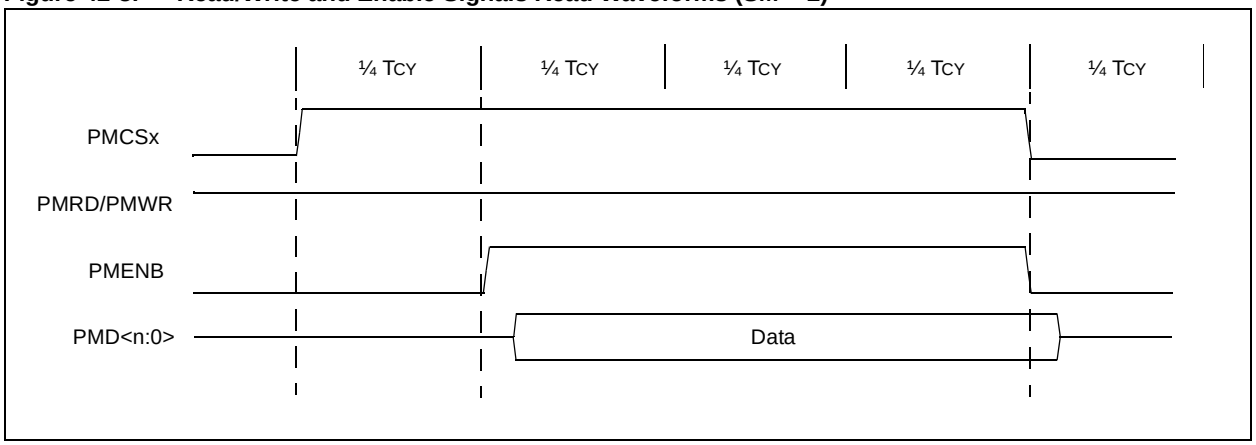
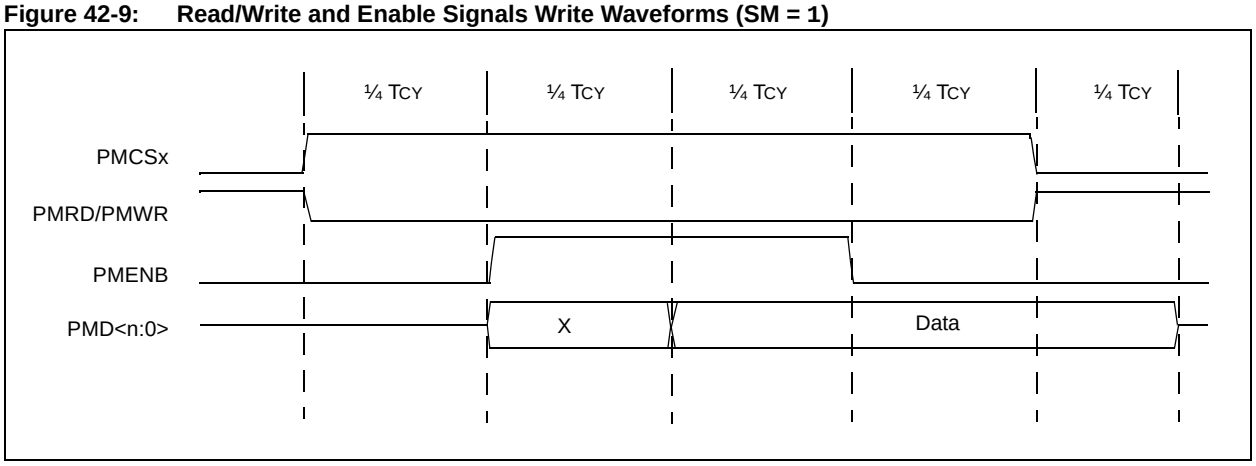


Figure 42-9: Read/$\overline{\text{Write}}$ and Enable Signals Write Waveforms (SM = 1)



42.4.1.5 CONTROL LINES POLARITY

All control signals (PMRD, PMWR, PMRD/$\overline{\text{PMWR}}$, PMENB, PMCS1, PMCS2, PMBE0, PMBE1, PMALL, PMALH, PMALU, PMACK1, PMACK2) can be individually configured for either positive or negative polarity.

Table 42-4: Control Signals Polarity Bits

EPMP Control Signal	Polarity Bit	Control register
PMRD	RDSP	PMCSxCF<9>
PMRD/$\overline{\text{PMWR}}$		
PMWR	WRSP	PMCSxCF<10>
PMENB		
PMBE0	BEP	PMCSxCF<12>
PMBE1		
PMCSx	CSP	PMCSxCF<14>
PMALL	ALP	PMCON1<5>
PMALH		
PMALU		
PMACKx	ACKP	PMCSxCF<7>

Configuration is controlled by separate bits in the PMCON1 and PMCSxCF registers. Note that the polarity of control signals that share the same output pin (for example, PMWR and PMENB) are controlled by the same bit; the configuration depends on which Master Port mode is being used. When PMA<15> and/or PMA<14> are used as chip select pins, their polarity is controlled by the PMCS1 and PMCS2 polarity controls, respectively. The PMALL, PMALH and PMALU signals share a single Configuration bit (ALP) since the polarity setting of these three signals should always be the same.

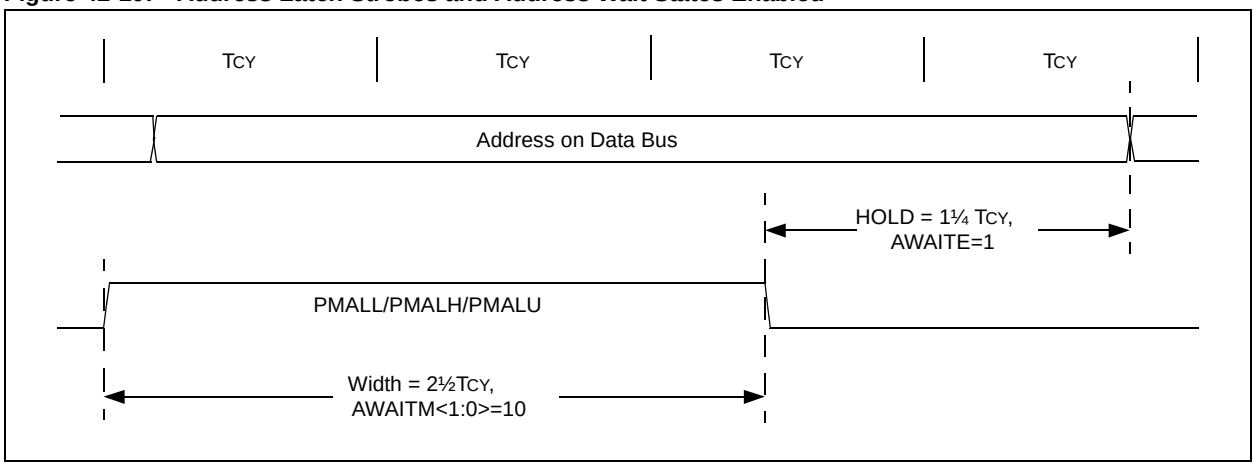
The polarity of the PMACKx input is determined by the ACKP bit. When ACKP is '0', the PMACKx input is active-low, and therefore acts as a BUSY signal. When ACKP is '1', the PMACKx input is active-high, and acts as an ACK signal.

42.4.1.6 ADDRESS WAIT STATES

In Master mode, when the address multiplexing is used (ADRMUX<1:0> $\neq$ 00), the user has control over the duration of the address phases by configuring the Address Wait states as multiples of TCY. The length of the assertion of the PMALL, PMALH and PMALU signals are configured using the AWAITM<1:0> and AWAITE bits in the PMCON3 register. The two AWAITM<1:0> bits set the width of the address latch strobes. The AWAITE bit sets the number of Wait cycles for the address hold time after the address latch strobes. Figure 42-10 is an example of the address Wait state settings.

Note:	Regardless of the value of AWAITM<1:0>, the timing from the assertion of the chip select to the assertion of the first address strobe signal is fixed at 1/4 TCY. Regardless of the value of AWAITM<1:0>, the timing from the end of the current Address Phase to the beginning of the next cycle is fixed at 1/4 TCY.

Figure 42-10: Address Latch Strobes and Address Wait States Enabled

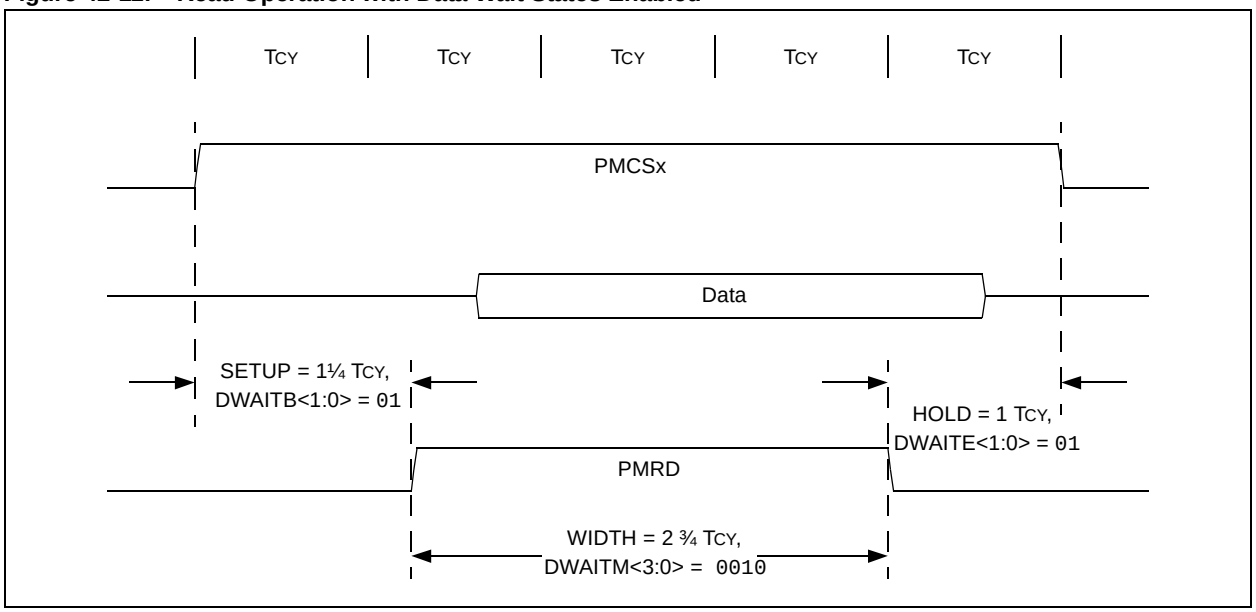


42.4.1.7 DATA WAIT STATES

The user has control over the duration of the read and write cycles by configuring the Data Wait states as multiples of TCY. Three portions of the data cycle, the beginning, middle and end, are configured using the corresponding DWAITB<1:0>, DWAITM<3:0> and DWAITE<1:0> bits in the PMCSxMD registers. The DWAITB<1:0> bits set the number of Wait cycles for the data setup prior to the PMRD and PMWR strobes (SM = 0), or prior to the PMENB strobe (SM = 1). The DWAITM<3:0> bits set the number of Wait cycles for the PMRD and PMWR strobes (SM = 0), or for the PMENB strobe (SM = 1).

The DWAITE<1:0> bits set the number of Wait cycles for the data hold time after the PMRD and PMWR strobes (SM = 0), or after the PMENB strobe (SM = 1). Figure 42-11 is an example of a read operation using data Wait states.

Figure 42-11: Read Operation with Data Wait States Enabled



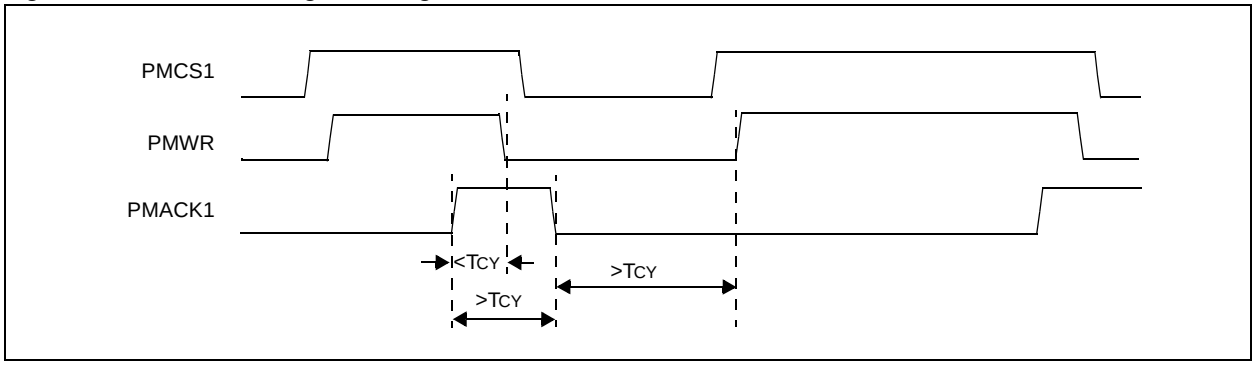
42.4.1.8 EXTERNAL ACKNOWLEDGEMENT

An external PMACKx input can be used to determine when the current read or write operation has completed. This mode is configured on a chip select basis by setting ACKM<1:0> bits in PMCSxMD registers. If ACKM<1:0> = 10, the read or write operation will be stretched until PMACKx is asserted from an external device or the number of wait cycles specified with DWAIT<3:0> is reached. If DWAIT<3:0> = 0000 the read or write operation is suspended until PMACKx is asserted.

When ACKM<1:0> = 01 a time-out for the read or write operation can be specified by writing the DWAITM<3:0> field with a value greater than '0'. The read or write operation is completed once PMACKx are asserted or the number of wait cycles specified with DWAITM<3:0> is reached, whichever comes first. If the operation is aborted due to a time-out, the TIMEOUT bit in PMCON2 register is set and the EPMP interrupt is generated. If DWAITM<3:0> = 0000 the time-out event is generated if PMACKx is not asserted within 255 TCY.

Due to synchronization, there could be up to one TCY delay between the time that PMACKx is asserted and when the read/write operation completes. For accesses that require two data phases (i.e., 8-bit read/write to a 4-bit port and 16-bit read/write to an 8-bit port), PMACKx must be asserted after each data phase by the slave device. Timing for the Acknowledgement signal is shown in Figure 42-12.

Figure 42-12: Acknowledgement Signal Waveforms



42.4.1.9 DATA PORT SIZE

The EPMP supports various data port widths of 4/8/16 bits, as configured for each chip select using the PTSZ<1:0> bits in PMCSxCF registers. The PMBE0 and PMBE1 signals functionality depends on the data port width and EDS access size. The EPMP address bus directs the 16-bit data words, and these signals are used to indicate nibbles and bytes. The PMBE0 and PMBE1 functions are listed in Table 42-5.

Table 42-5: Port Size Summary

		EDS Access Size	
		8-Bit (Byte)	**16-Bit (Word)**
Port Size	4-bit (PTSZ<1:0> = 01)	2x4-bit Data Phases PMBE1 = Byte address PMBE0 = Nibble address	4x4-bit Data Phases PMBE1 = Byte address PMBE0 = Nibble address
	8-bit (PTSZ<1:0> = 00)	1x8-bit Data Phase PMBE1 = Not used PMBE0 = Byte address	2x8-bit Data Phases PMBE1 = Not used PMBE0 = Byte address
	16-bit (PTSZ<1:0> = 10)	1x16-bit Data Phase PMBE1 = Asserted for odd address PMBE0 = Asserted for even address	1x16-bit Data Phase PMBE1 = Asserted PMBE0 = Asserted

42.4.1.9.1 8-Bit Access over a 4-Bit Port

When a byte (8-bit) read or write is performed to the EPMP memory space and data port size is 4-bit (PTSZ<1:0> = 01), the EPMP will perform two 4-bit (nibble) data accesses. Since the address on the EPMP interface is a word address, PMBE1 line indicates high/low byte and PMBE0 line indicates high/low nibble. Timing for this mode is shown in Figure 42-13 and Figure 42-14.

Note:	It is not possible to directly access only a single nibble. Therefore, nibble writes must be done by performing an 8-bit read-modify-write operation in software.

Figure 42-13: 8-Bit Access Over a 4-Bit Port Read Waveforms

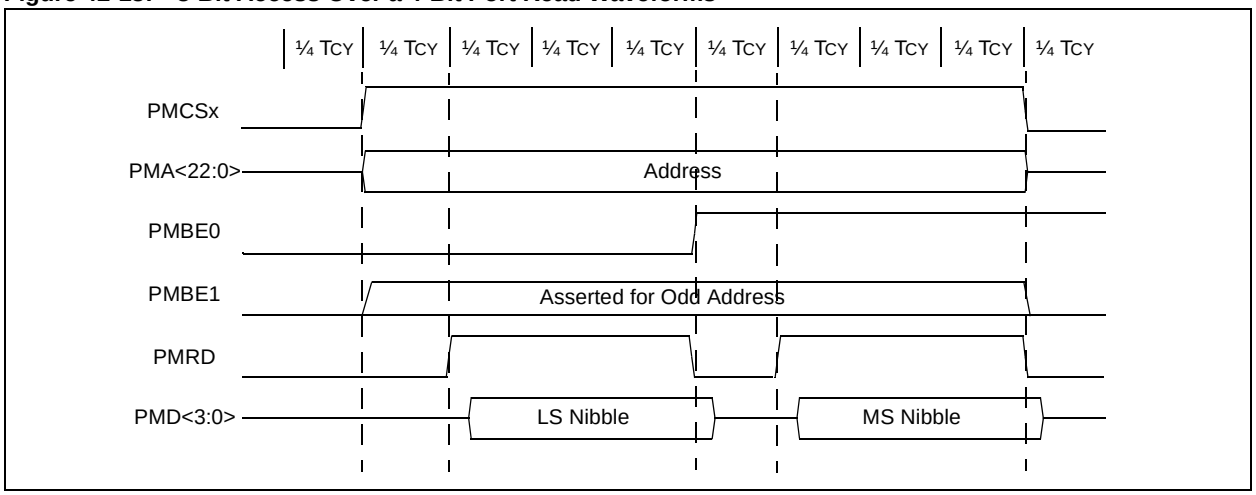
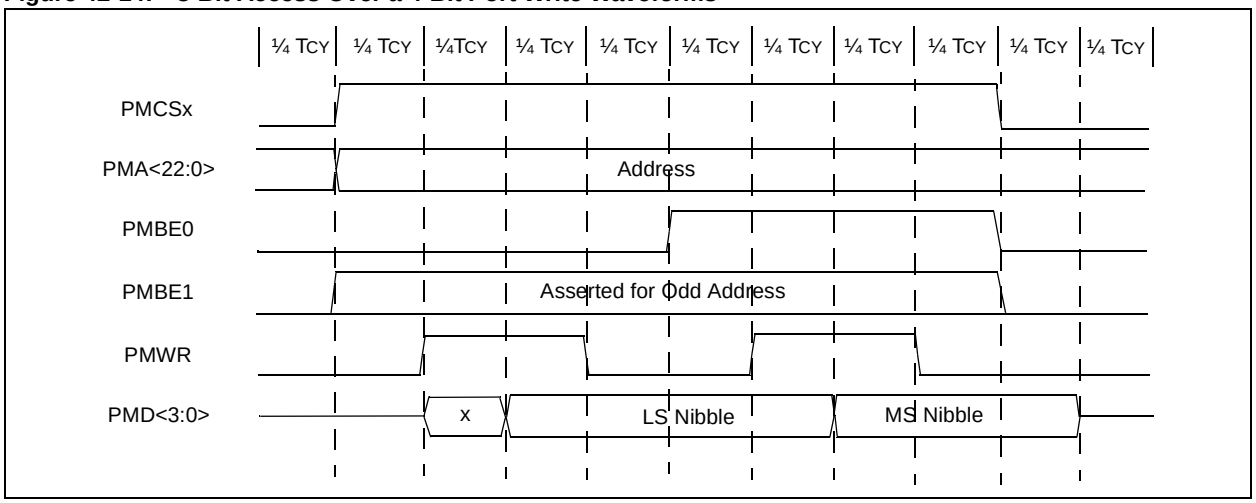


Figure 42-14: 8-Bit Access Over a 4-Bit Port Write Waveforms



42.4.1.9.2 8-Bit Access over an 8-Bit Port

When a byte read or write is performed to the EPMP memory space and data port size is 8-bit (PTSZ<1:0> = 00), the EPMP will perform a single byte data access. Since the address on the EPMP interface is a word address, PMBE0 line indicates high/low byte and PMBE1 line is not used.

Timing for this mode is shown in Figure 42-15 and Figure 42-16.

Figure 42-15: 8-Bit Access Over an 8-Bit Port Read Waveforms

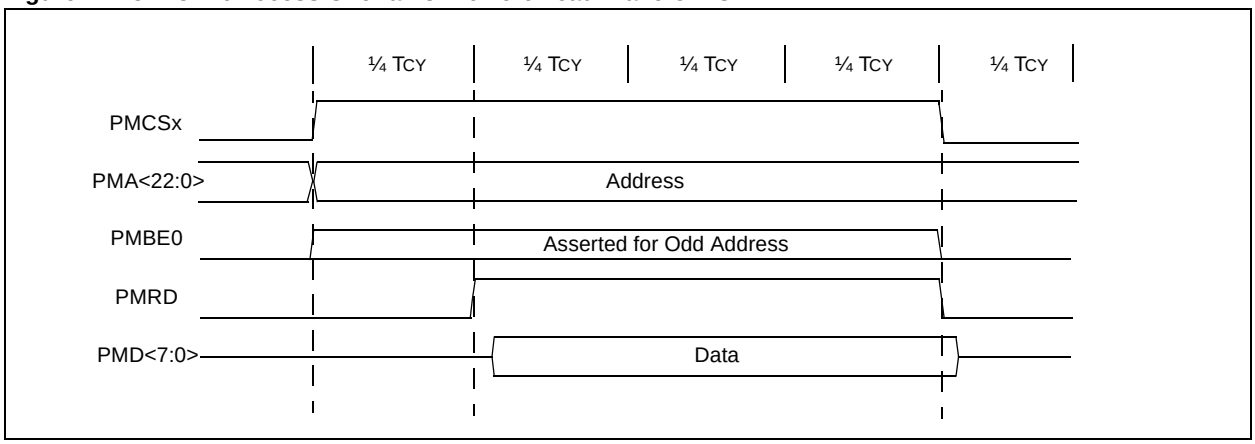
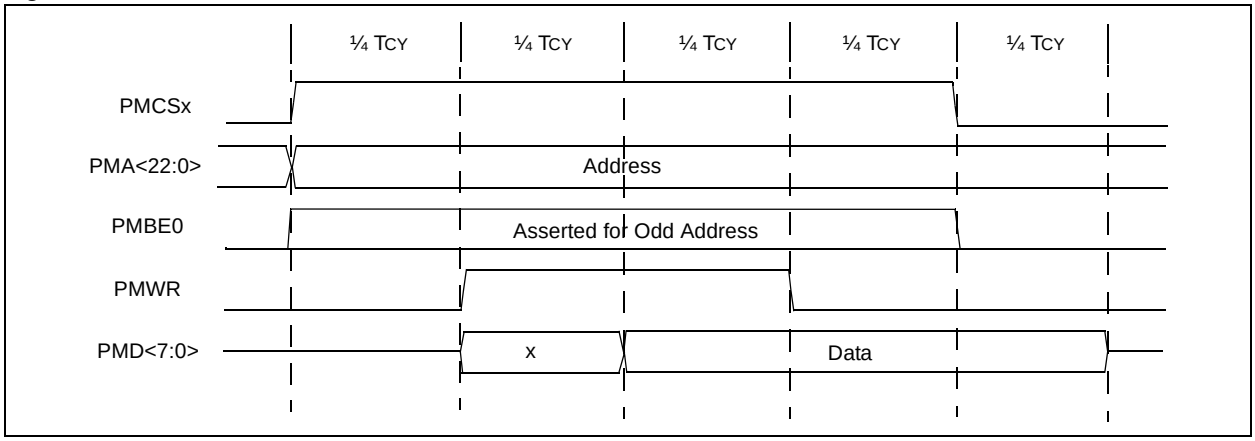


Figure 42-16: 8-Bit Access Over an 8-Bit Port Write Waveforms



42.4.1.9.3 8-Bit Access over a 16-Bit Port

When a byte (8-bit) read or write is performed to the EPMP memory space and data port size is 16-bit (PTSZ<1:0> = 10), the EPMP will perform a single word data access. In the case of a read, the 16-bit data will be returned unmodified to the CPU core, which then selects the appropriate byte. In the case of a write, the PMBE0 and PMBE1 lines will indicate which byte is to be written (PMBE0 for even addresses, PMBE1 for odd addresses).

Timing for this case is displayed in Figure 42-17 and Figure 42-18.

Figure 42-17: 8-Bit Access Over a 16-Bit Port Read Waveforms

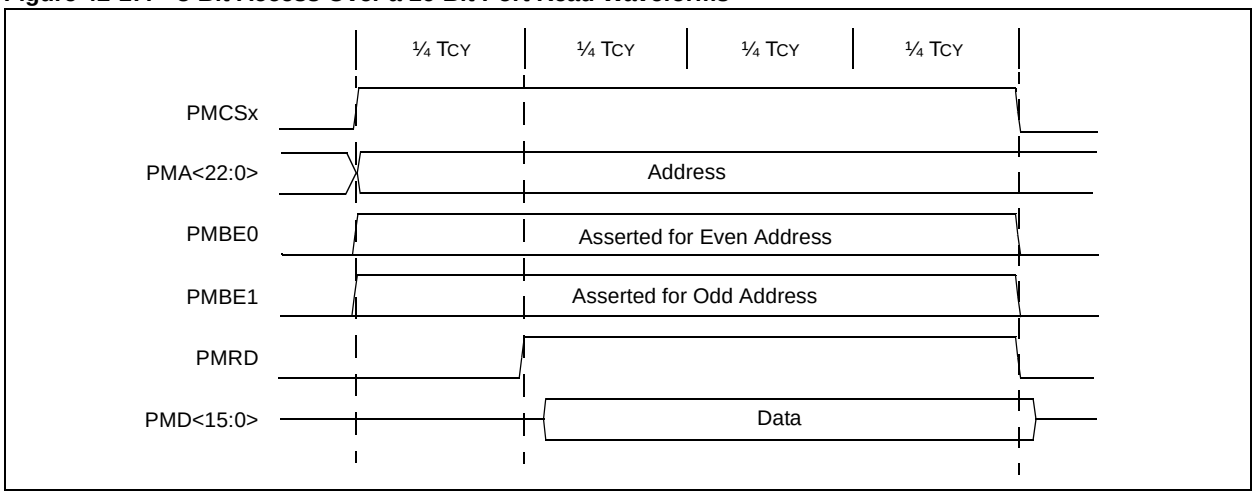
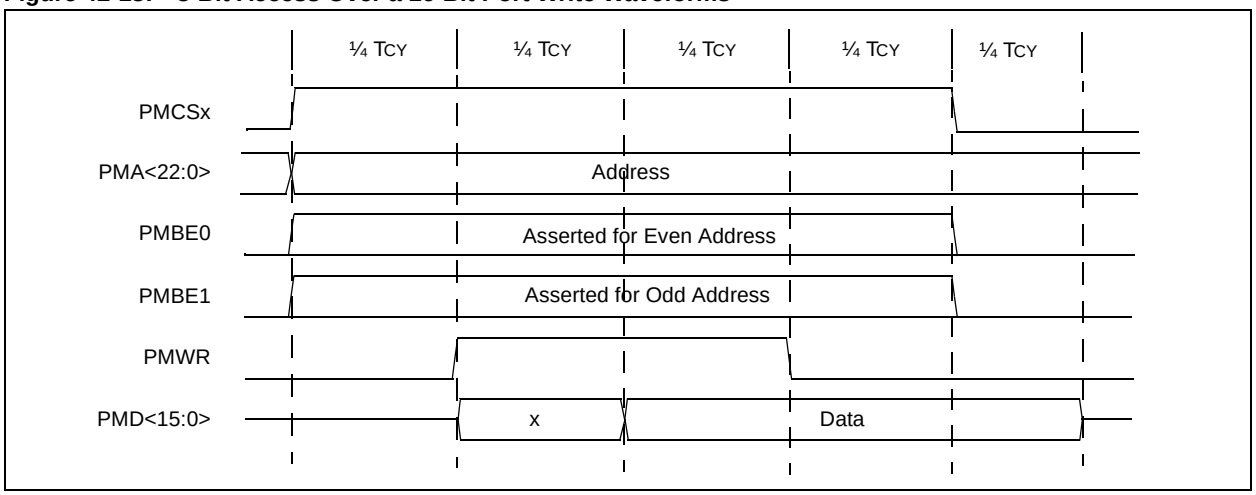


Figure 42-18: 8-Bit Access Over a 16-Bit Port Write Waveforms



42.4.1.9.4 16-Bit Access over a 4-Bit Port

When a word (16-bit) read or write is performed to the EPMP memory space and data port size is 4-bit (PTSZ<1:0> = 01), the EPMP will perform four 4-bit (nibble) data accesses. Since the address on the EPMP interface is a word address, PMBE1 line indicates high/low byte and PMBE0 line indicates high/low nibble.

Timing for this mode is displayed in Figure 42-19 and Figure 42-20.

Figure 42-19: 16-Bit Access Over a 4-Bit Port Read Waveforms

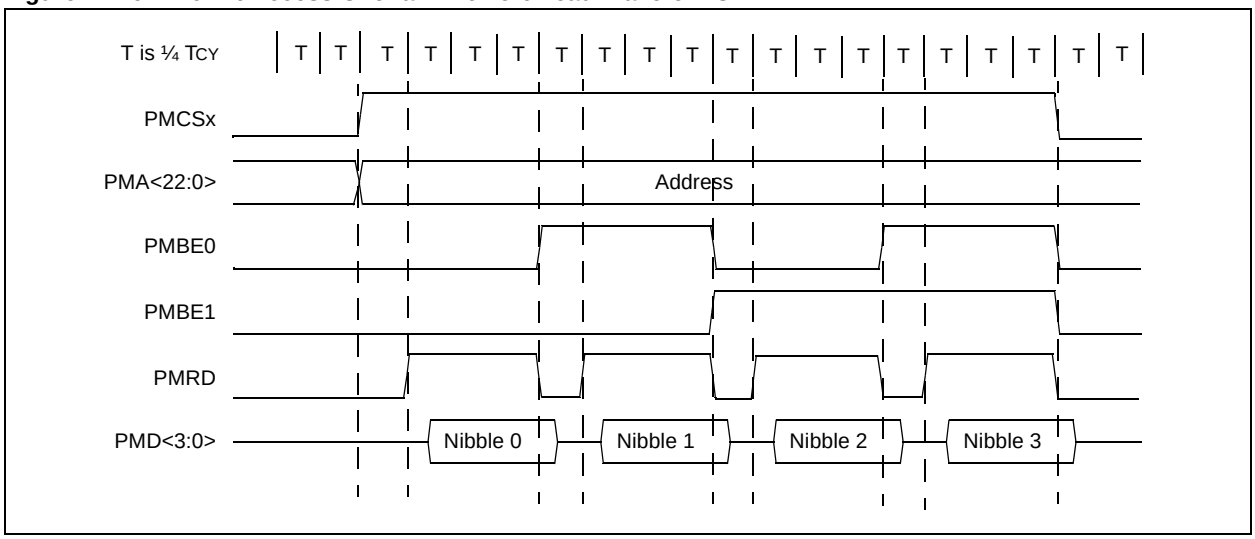
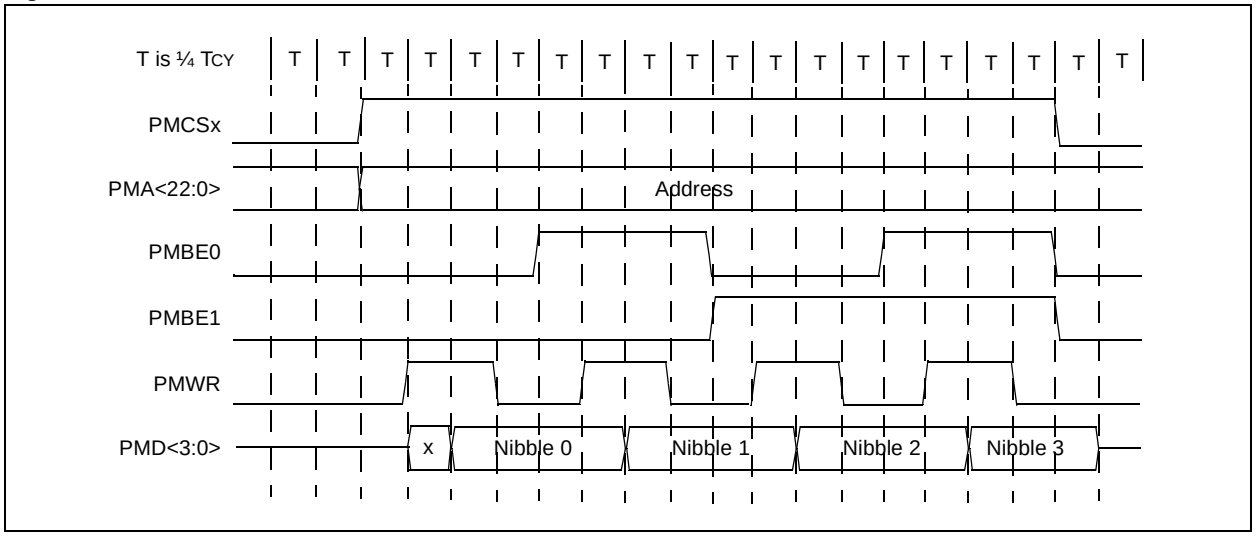


Figure 42-20: 16-Bit Access Over a 4-Bit Port Write Waveforms



42.4.1.9.5 16-Bit Access over an 8-Bit Port

When a word (16-bit) read or write is performed to the EPMP memory space and data port size is 8-bit (PTSZ<1:0> = 00), the EPMP will perform two 8-bit data transfers with PMBE0 line used to indicate high/low byte of the word. PMBE1 line is not used in this case.

Timing for this mode is displayed in Figure 42-21 and Figure 42-22.

Figure 42-21: 16-Bit Access Over an 8-Bit Port Read Waveforms

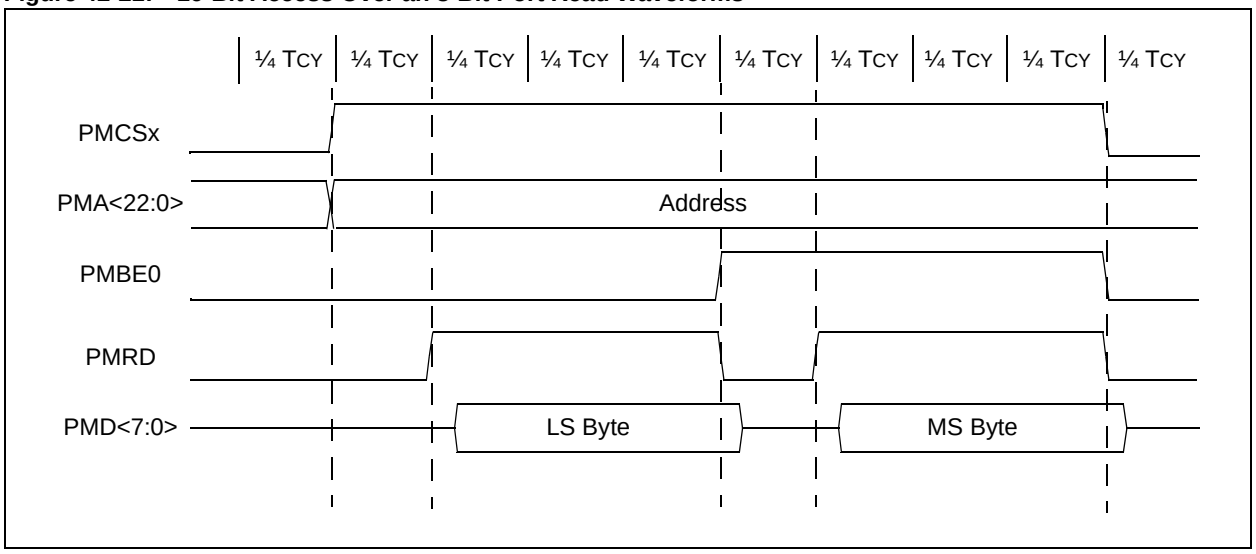
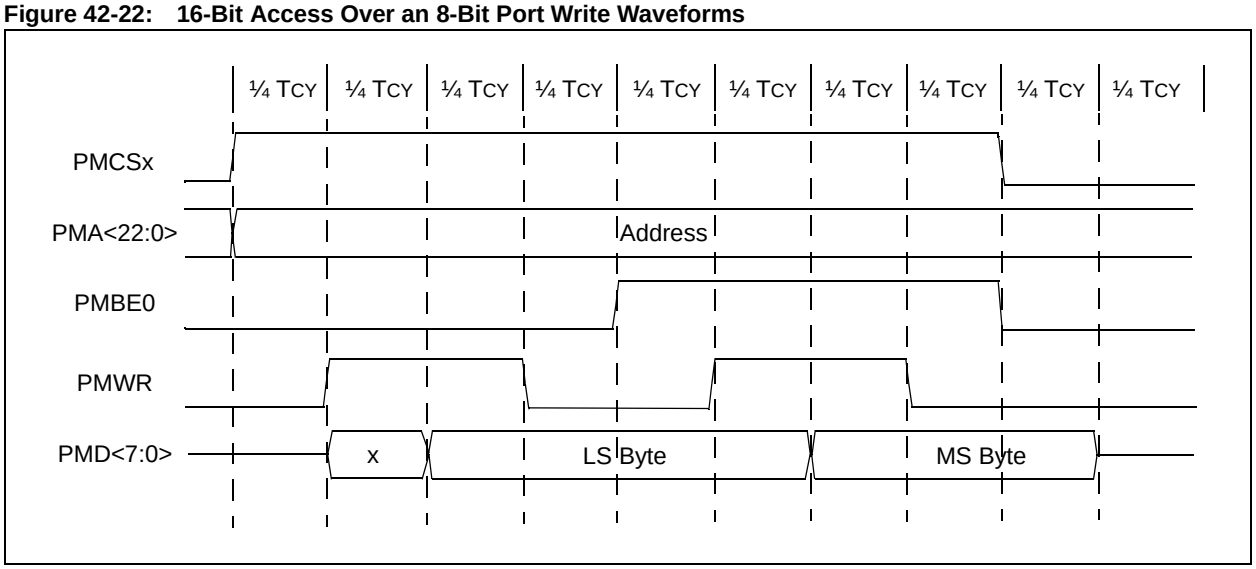


Figure 42-22: 16-Bit Access Over an 8-Bit Port Write Waveforms



42.4.1.9.6 16-Bit Access over a 16-Bit Port

When a word (16-bit) read or write is performed to the EPMP memory space and data port size is 16-bit (PTSZ<1:0> = 10), the EPMP will perform a single word data access. In this case both PMBE1 and PMBE0 lines are asserted.

Timing for this mode is displayed in Figure 42-23 and Figure 42-24.

Figure 42-23: 16-Bit Access Over a 16-Bit Port Read Waveforms

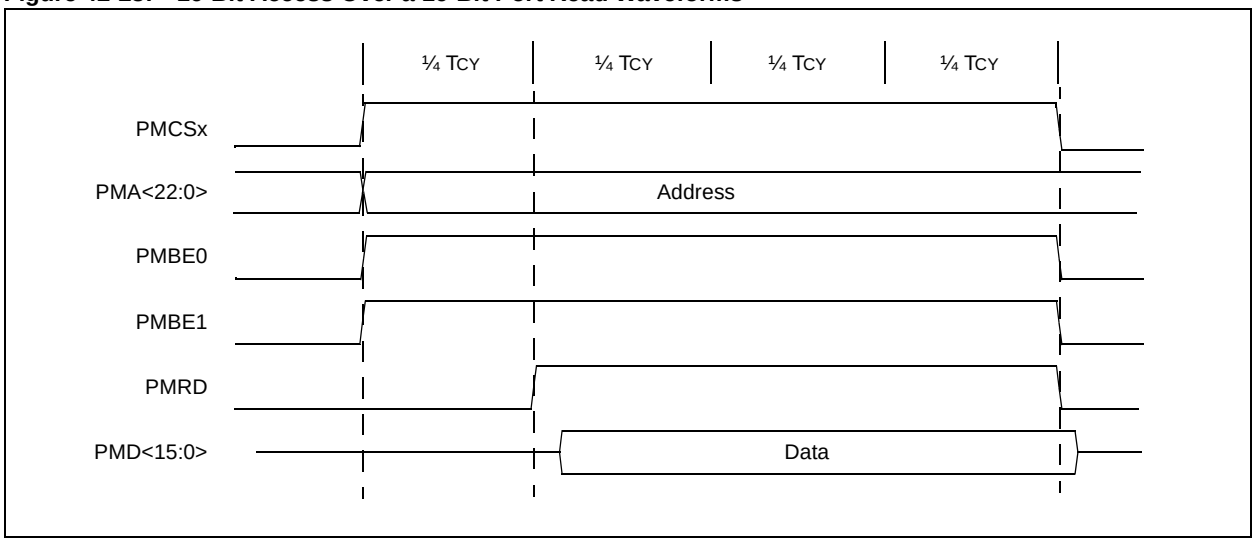
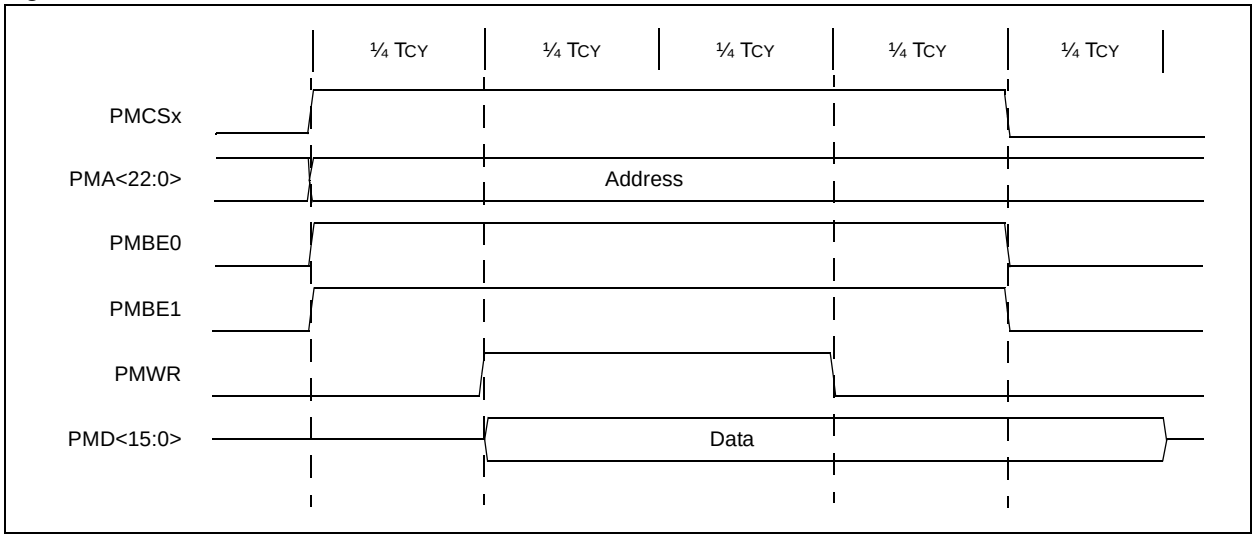


Figure 42-24: 16-Bit Access Over a 16-Bit Port Write Waveforms



42.4.1.10 ADDRESS MULTIPLEXING

Address multiplexing allows some or all address line signals to be generated from the data bus during the address cycle of a read/write operation. This can be a useful option for address lines PMA<22:0> needed as general purpose I/O pins. This is accomplished using the ADRMUX<1:0> (PMCON1<12:11>) bits. There are several Address Multiplexing modes available (listed in Table 42-6), based on the number of address phases and data port sizes. The address and data lines can have different locations depending on the mode used.

Table 42-6: Address Multiplexing Summary

Data Port Size	PMA<22:16>	PMA<15:8>	PMA<7:0>	PMD<15:8>	PMD<7:4>	PMD<3:0>
Demultiplexed Address (ADRMUX<1:0> = 00)						
16-bit (PTSZ = 10)	Addr<22:16>	Addr<15:8>	Addr<7:0>	—	Data(1)	
8-bit (PTSZ = 00)	Addr<22:16>	Addr<15:8>	Addr<7:0>	—	Data(1)	
4-bit (PTSZ = 01)	Addr<22:16>	Addr<15:8>	Addr<7:0>	—	—	Data(1)
1 Address Phase (ADRMUX<1:0> = 01)						
16-bit (PTSZ = 10)	Addr<22:16>	Addr<15:8>	PMALH/PMALL	—	Addr<7:0>Data(1)	
		Data(1)	—	—	—	
8-bit (PTSZ = 00)	Addr<22:16>	Addr<15:8>	PMALL	—	Addr<7:0>Data(1)	
4-bit (PTSZ = 01)	Addr<22:16>	Addr<15:8>	PMALL	—	Addr<7:4>	Addr<3:0>
			—	—	—	Data(1)
2 Address Phases (ADRMUX<1:0> = 10)						
16-bit (PTSZ = 10)	—	Addr<15:8>	PMALH/PMALL	—	Addr<7:0>	
		—	PMALU	—	Addr<22:16>	
		Data(1)	—	—	Data(1)	
8-bit (PTSZ = 00)	Addr<22:16>	—	PMALL	—	Addr<7:0>	
			PMALH	—	Addr<15:8>	
			—	—	Data(1)	
4-bit (PTSZ = 01)	Addr<22:16>	Addr<15:8>	PMALL	—	Addr<3:0>	
			PMALH	—	Addr<7:4>	
			—	—	Data(1)	
3 Address Phases (ADRMUX<1:0> = 11)						
16-bit (PTSZ = 10)	Not used					
8-bit (PTSZ = 00)	—	—	PMALL	—	Addr<7:0>	
			PMALH	—	Addr<15:8>	
			PMALU	—	Addr<22:16>	
			—	—	Data(1)	
4-bit (PTSZ = 01)	Addr<22:16>	Addr<15:12>	PMALL	—	—	Addr<3:0>
			PMALH	—	—	Addr<7:4>
			PMALU	—	—	Addr<11:8>
			—	—	—	Data(1)

Note 1: Data may present either 1, 2 or 4 data phases, depending on EDS access size (see **42.4.1.9 "Data Port Size"** for details).

42.4.1.10.1 Demultiplexed Mode

In Demultiplexed mode (ADRMUX<1:0> = 00), data and address information are completely separated. Data is presented on PMD<15:0>, depending on the port size (PTSZ<1:0> bits), and address is presented on PMA<22:0>.

Timing for this mode is displayed in Figure 42-25 and Figure 42-26.

Figure 42-25: Demultiplexed Mode Read Waveforms

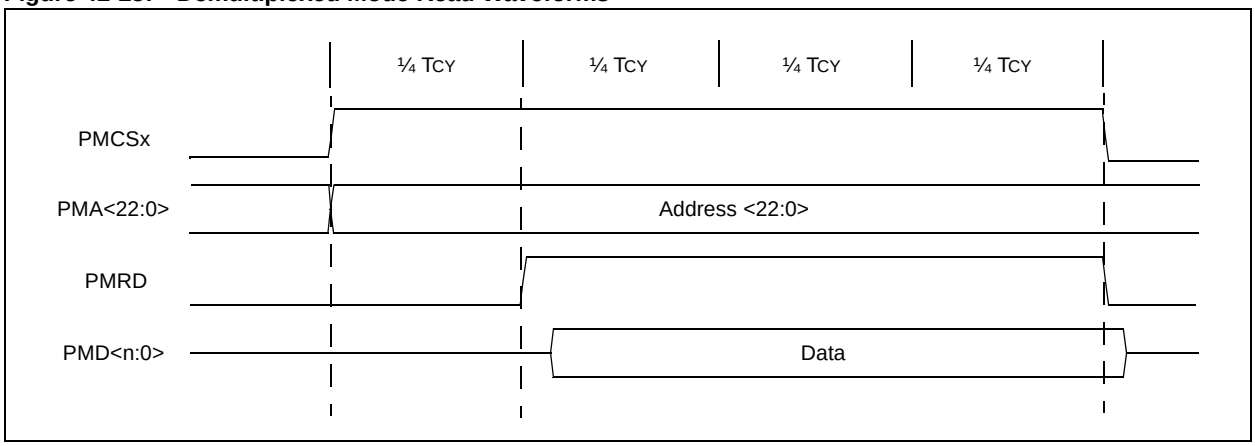
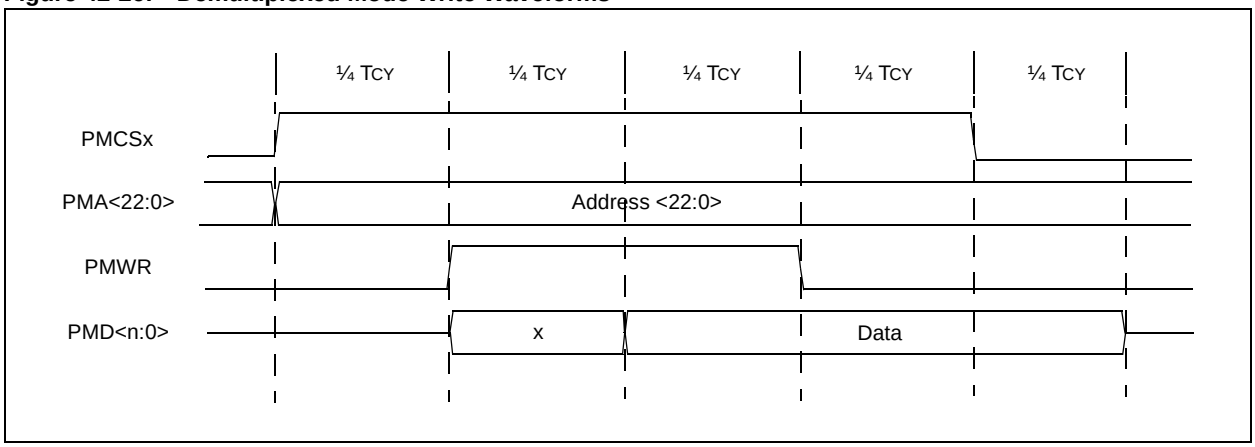


Figure 42-26: Demultiplexed Mode Write Waveforms



42.4.1.10.2 Single Address Phase Mode over a 4-Bit Port

When ADRMUX<1:0> = 01 and PTSZ<1:0> = 01, the lower 4 bits of the address are multiplexed with data in a single address phase. The PMA<0> pin is used for the address latch, and presents the Address Latch Low (PMALL) Enable strobe. The read and write operations consist of several cycles. During the first cycle the address bits <3:0> are presented on PMD<3:0> pins with the PMALL strobe active. During the next cycles, the data is transmitted. In this mode, the address bits <7:4> are presented on PMD<7:4> pins.

Timing for this mode is displayed in Figure 42-27 and Figure 42-28.

Figure 42-27: Single Address Phase Mode Over a 4-Bit Port Read Waveforms

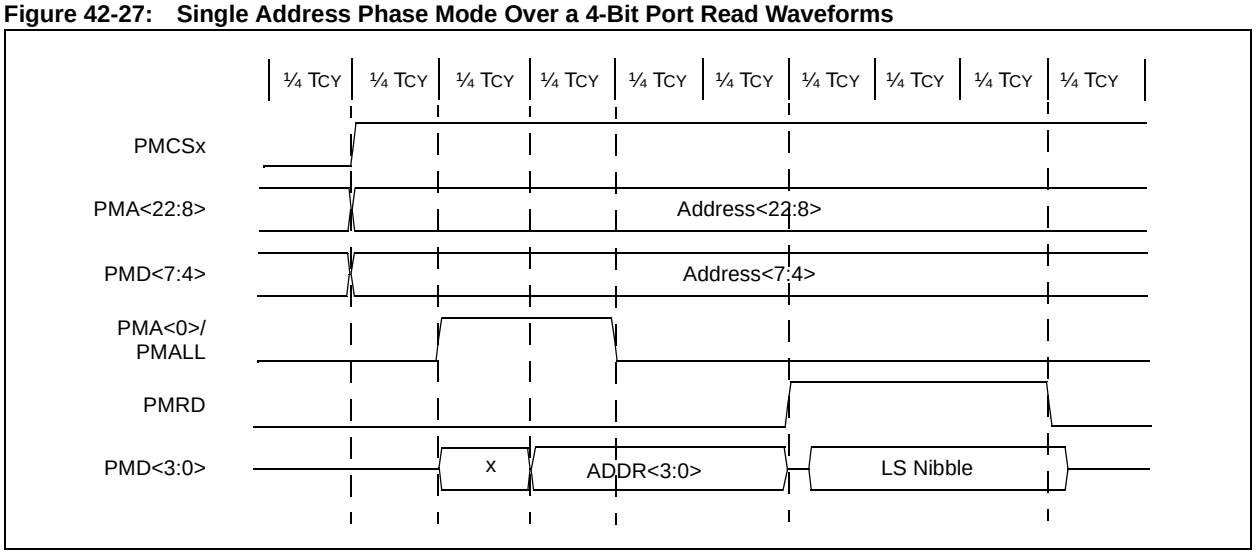
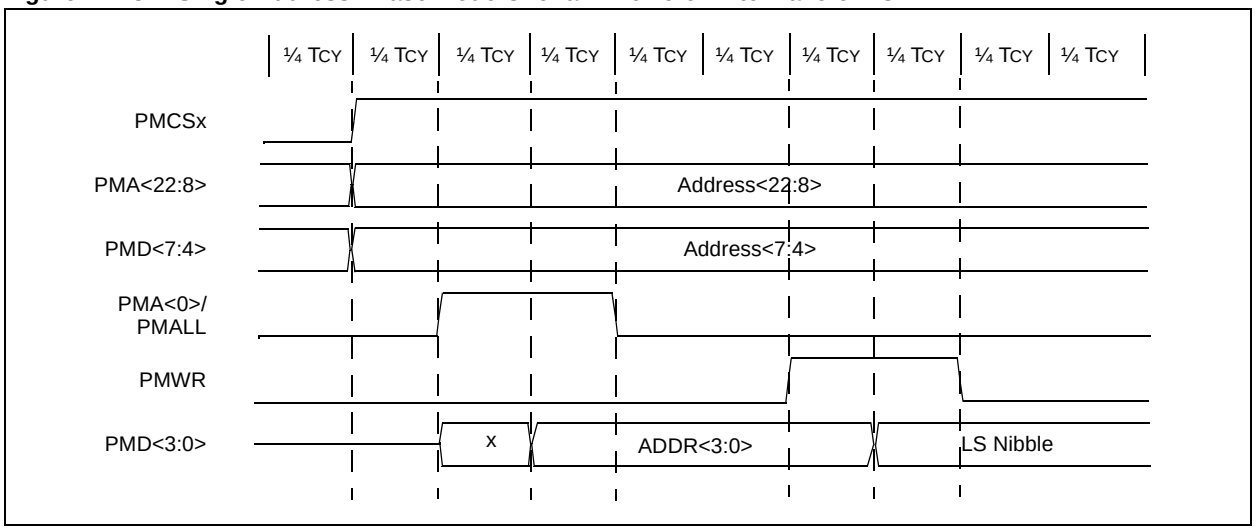


Figure 42-28: Single Address Phase Mode Over a 4-Bit Port Write Waveforms



42.4.1.10.3 Single Address Phase Mode over an 8-Bit Port

When ADRMUX<1:0> = 01 and PTSZ<1:0> = 00, the lower 8 bits of the address are multiplexed with data in a single address phase. The PMA<0> pin is used for the address latch, and presents the Address Latch Low (PMALL) Enable strobe. The read and write operations consist of several cycles. During the first cycle the address bits <7:0> are presented on PMD<7:0> pins with the PMALL strobe active. During the next cycles the data is transmitted.

Timing for this mode is displayed in Figure 42-29 and Figure 42-30.

Figure 42-29: Single Address Phase Mode Over an 8-Bit Port Read Waveforms

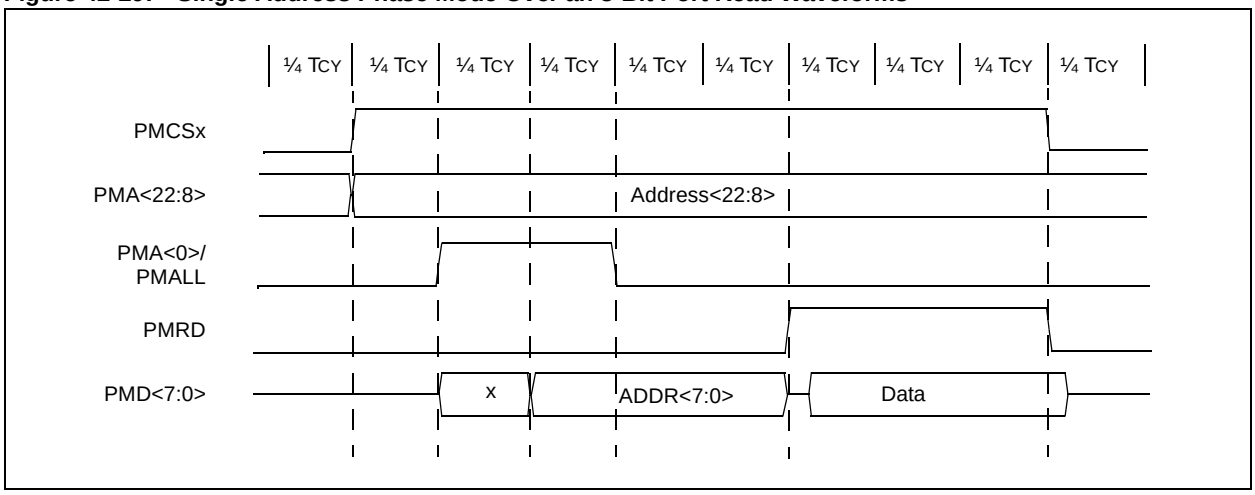
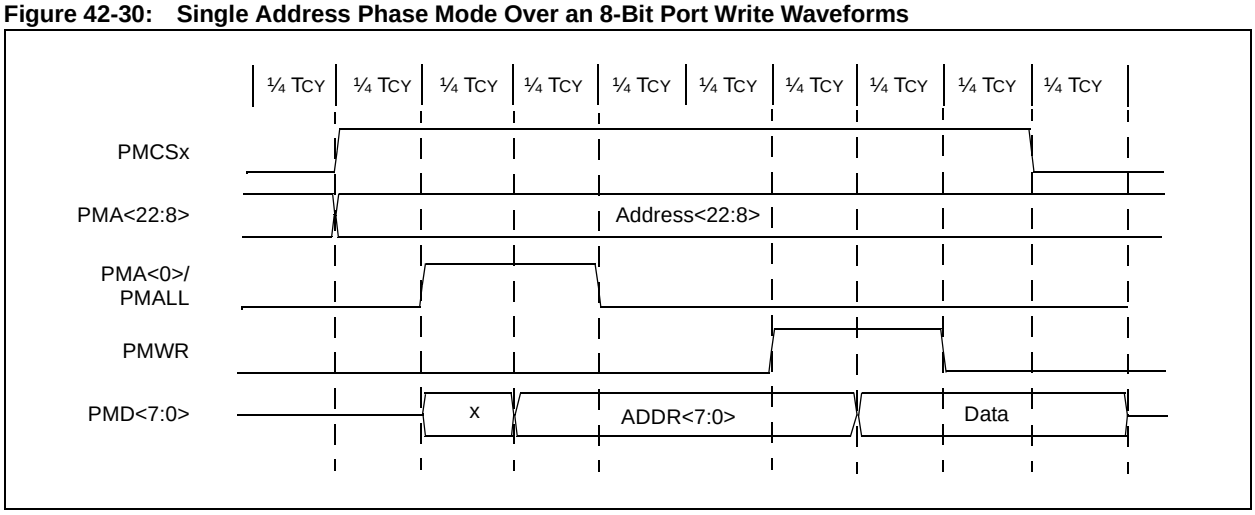


Figure 42-30: Single Address Phase Mode Over an 8-Bit Port Write Waveforms



42.4.1.10.4 Single Address Phase Mode over a 16-Bit Port

When ADRMUX<1:0> = 01 and PTSZ<1:0> = 10, the lower 16 bits of the address are multiplexed with data in a single address phase. The PMA<0> and PMA<1> pins are used for the address latches, and present the Address Latch Low (PMALL) and Address Latch High (PMALH) Enable strobes, respectively. In this mode, PMA<15:8> pins are used for the high part of the data bus. The read and write operations consist of several cycles. During the first cycle, the address bits <15:0> are presented on PMD<7:0> and PMA<15:8> with the PMALL and PMALH strobes active. During the next cycle the data is presented on these pins.

Timing for this mode is displayed in Figure 42-31 and Figure 42-32.

Figure 42-31: Single Address Phase Mode Over a 16-Bit Port Read Waveforms

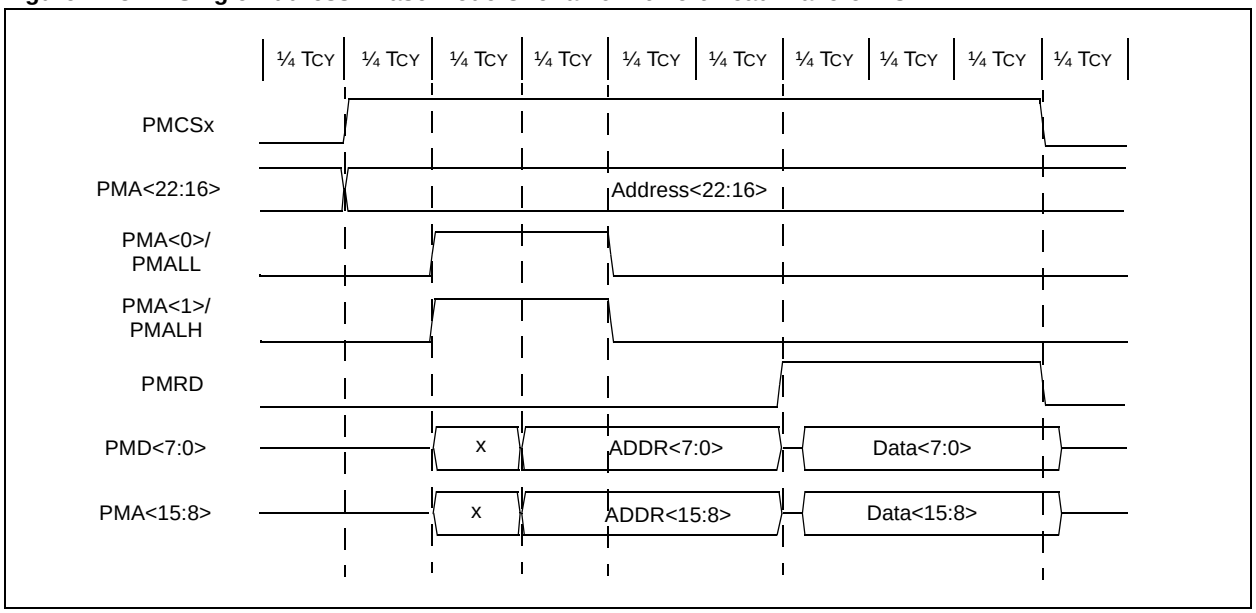
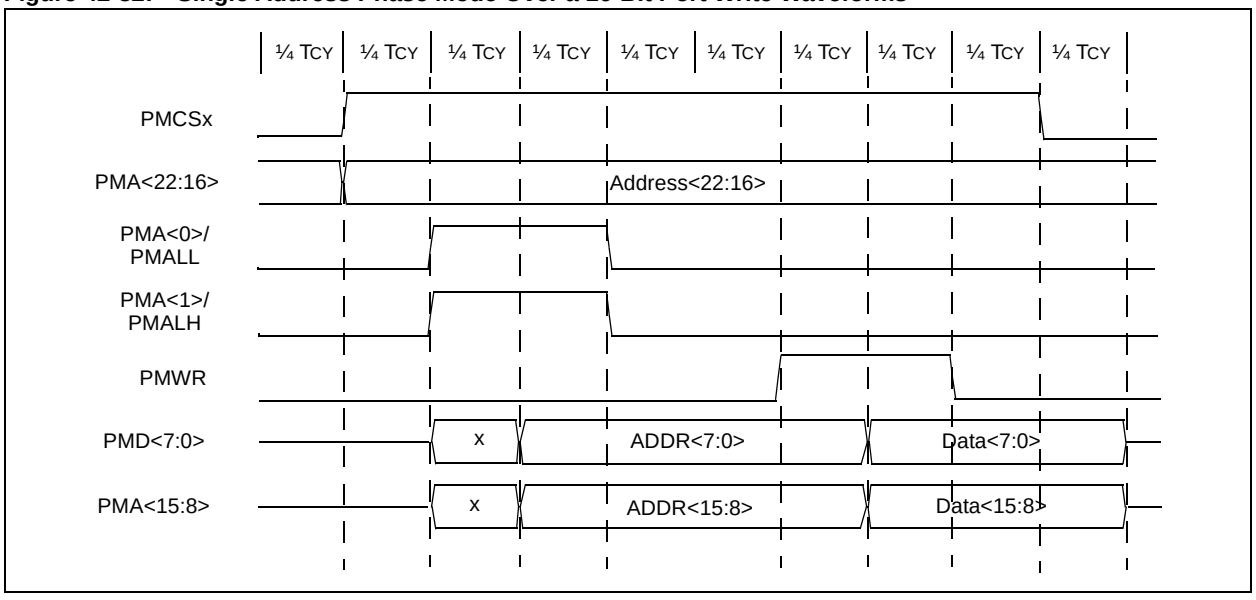


Figure 42-32: Single Address Phase Mode Over a 16-Bit Port Write Waveforms



42.4.1.10.5 Two Address Phases Mode over a 4-Bit Port

When ADRMUX<1:0> = 10 and PTSZ<1:0> = 01, the lower 8-bit of the address is multiplexed with data in two address phases. The PMA<0> and PMA<1> pins are used for the address latches, and present the Address Latch Low (PMALL) and Address Latch High (PMALH) Enable strobes, respectively. The read and write sequences take several cycles. During the first cycle, the address bits <3:0> are presented on the data bus with the PMALL strobe active. During the second cycle, the address bits <7:4> are presented with the PMALH strobes active. During the next cycles, the data is transmitted.

Timing for this mode is displayed in Figure 42-33 and Figure 42-34.

Figure 42-33: Two Address Phases Mode Over a 4-Bit Port Read Waveforms

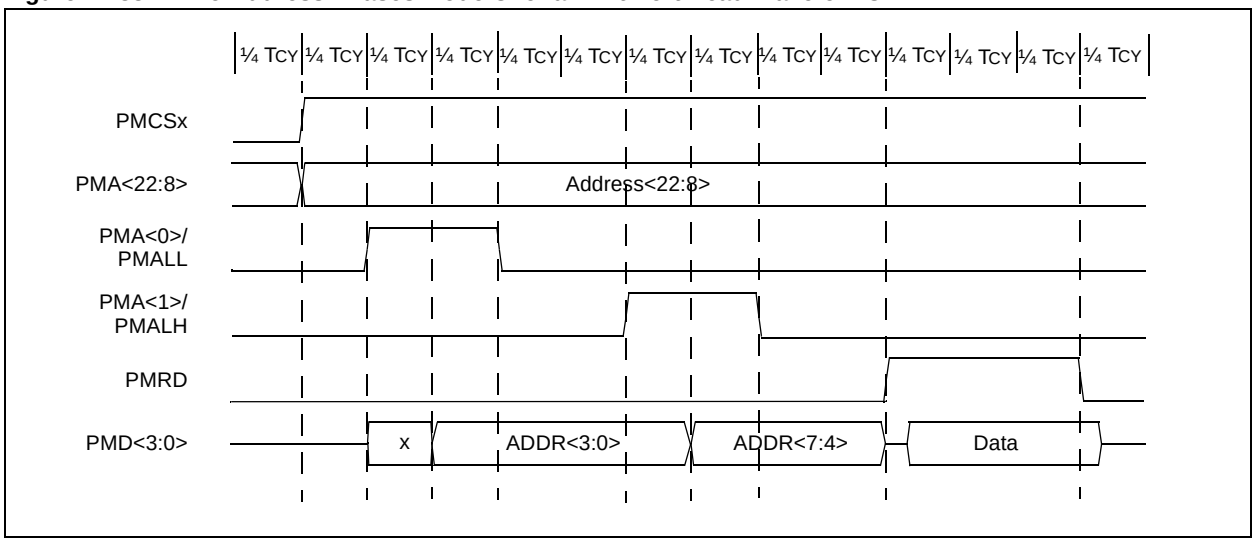
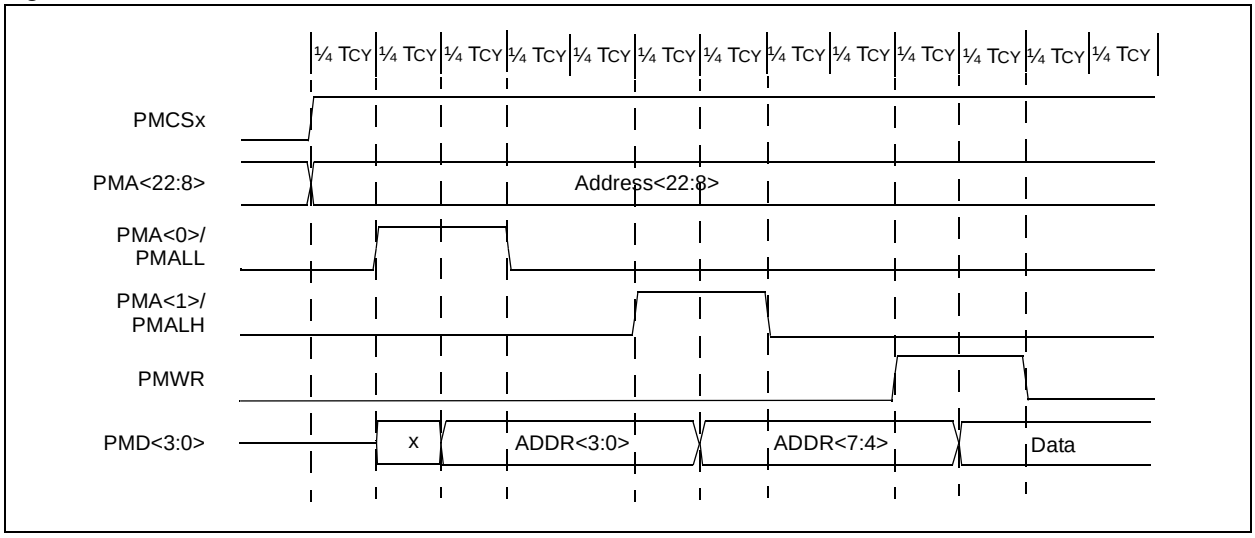


Figure 42-34: Two Address Phases Mode Over a 4-Bit Port Write Waveforms



42.4.1.10.6 Two Address Phases Mode over an 8-Bit Port

When ADRMUX<1:0> = 10 and PTSZ<1:0> = 00, the lower 16-bit of the address is multiplexed with data in two address phases. The PMA<0> and PMA<1> pins are used for the address latches, and present the Address Latch Low (PMALL) and Address Latch High (PMALH) Enable strobes, respectively. The read and write sequences take several cycles. During the first cycle, the address bits <7:0> are presented on the data bus with the PMALL strobe active. During the second cycle, the address bits <15:8> are presented with the PMALH strobes active. During the next cycles, the data is transmitted.

Timing for this mode is displayed in Figure 42-35 and Figure 42-36.

Figure 42-35: Two Address Phases Mode Over an 8-Bit Port Read Waveforms

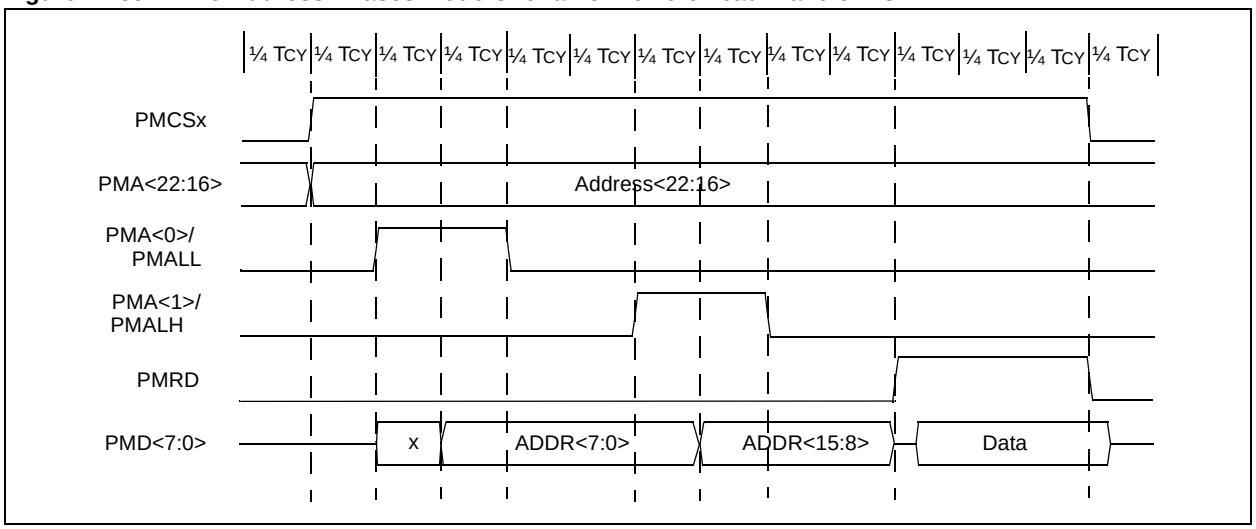
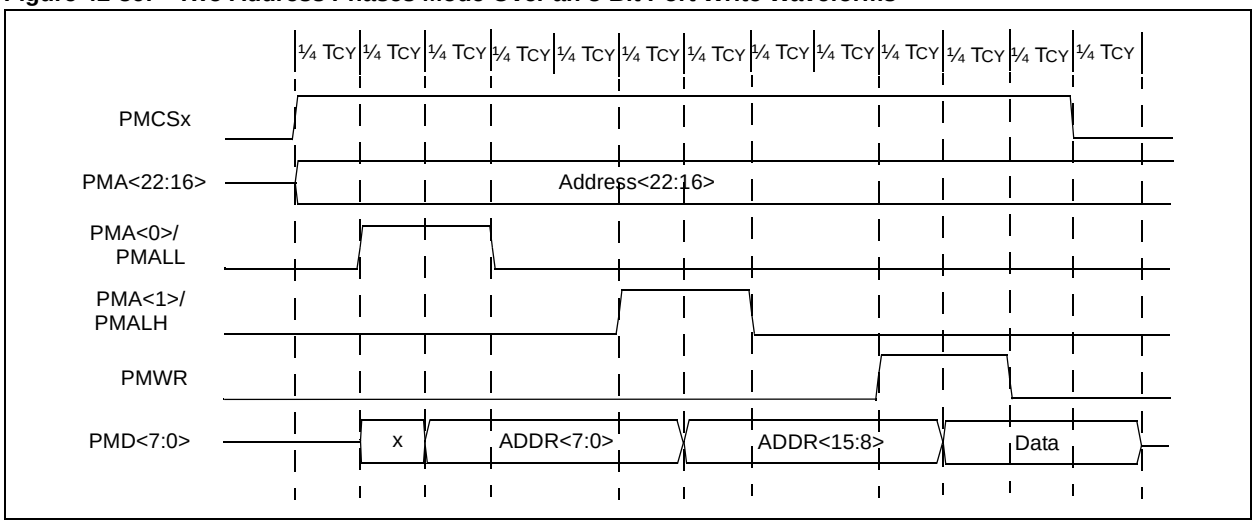


Figure 42-36: Two Address Phases Mode Over an 8-Bit Port Write Waveforms



42.4.1.10.7 Two Address Phases Mode over a 16-Bit Port

When ADRMUX<1:0> = 10 and PTSZ<1:0> = 10, the 23-bit address is multiplexed with data in two address phases. The PMA<0>, PMA<1> and PMA<2> pins are used for the address latches, and present the Address Latch Low (PMALL), Address Latch High (PMALH) and Address Latch Upper (PMALU) Enable strobes, respectively. In this mode PMA<15:8> pins are used for the high part of the data bus. The read and write sequences take several cycles. During the first cycle, the address bits <15:0> are presented on the data bus with the PMALL and PMALH strobes active. During the second cycle, the address bits <22:8> are presented with the PMALU strobe active. During the next cycles, the data is transmitted.

Timing for this mode is shown in Figure 42-37 and Figure 42-38.

Figure 42-37: Two Address Phases Mode Over a 16-Bit Port Read Waveforms

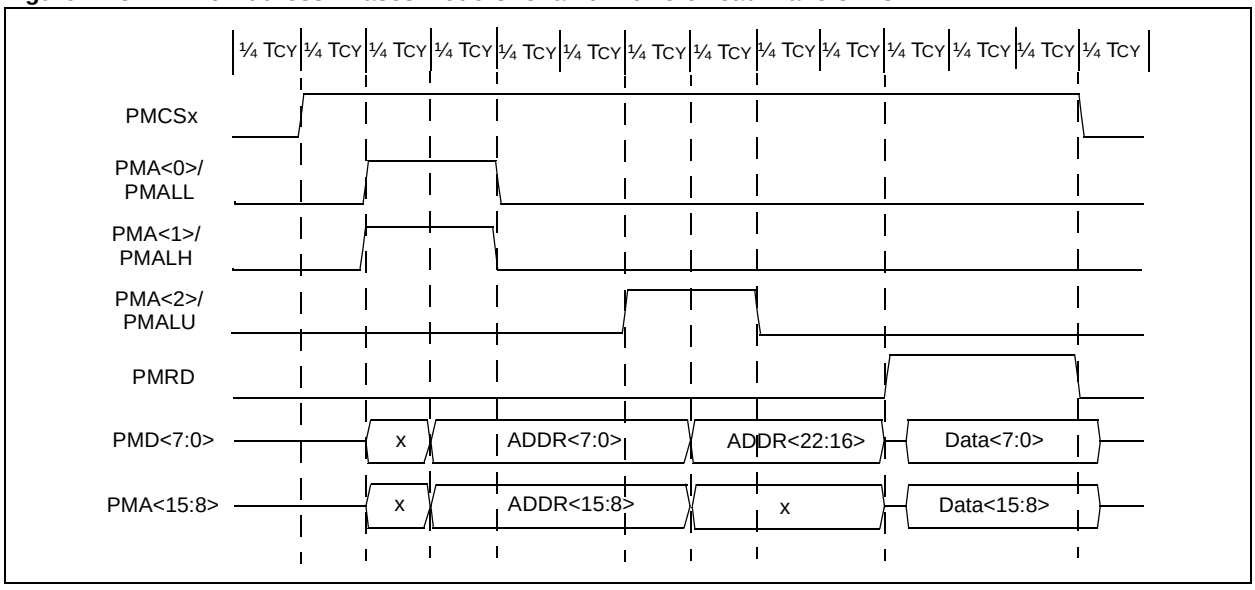
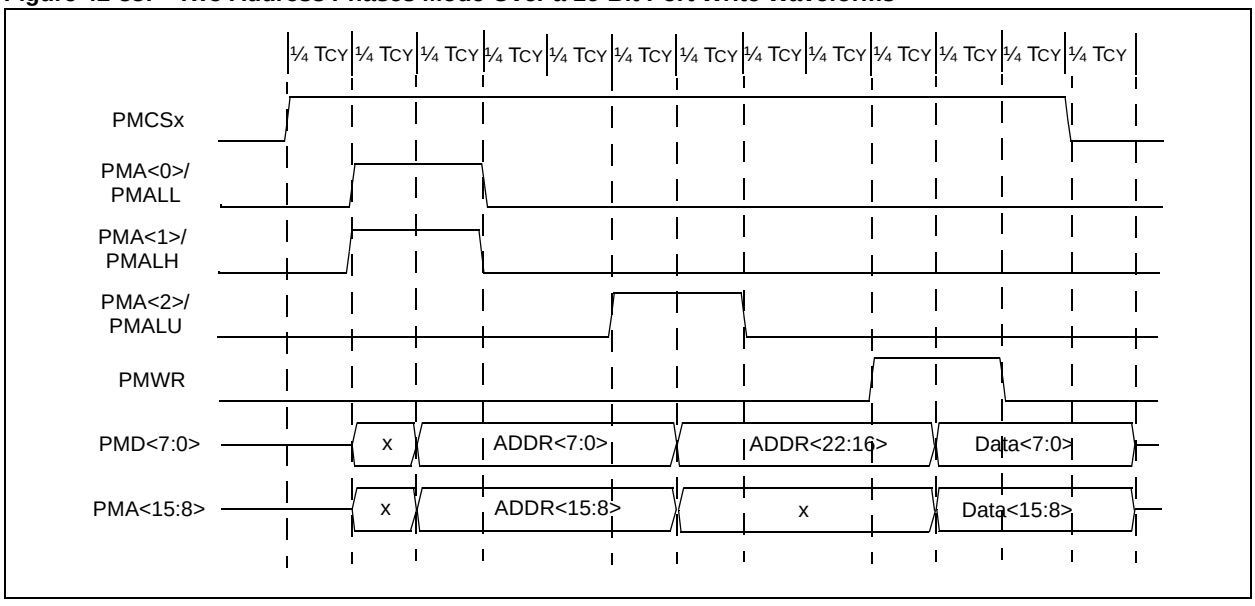


Figure 42-38: Two Address Phases Mode Over a 16-Bit Port Write Waveforms



42.4.1.10.8 Three Address Phases Mode over a 4-Bit Port

When ADRMUX<1:0> = 11 and PTSZ<1:0> = 01, the lower 12 address bits are multiplexed with data in three address phases. The PMA<0>, PMA<1> and PMA<2> pins are used to present the Address Latch Low (PMALL) Enable, Address Latch High (PMALH) Enable and Address Latch Upper (PMALU) Enable strobes, respectively. The read and write sequences take several cycles. During the first cycle, the address bits <3:0> are presented on the data bus with the PMALL strobe active. During the second cycle, the address bits <7:4> are presented with the PMALH strobe active. During the third cycle, the bits <11:8> are presented with the PMALU strobe active. During the next cycles, the data is transmitted.

Timing for this mode is shown in Figure 42-39 and Figure 42-40.

Figure 42-39: Three Address Phases Mode Over a 4-Bit Port Read Waveforms

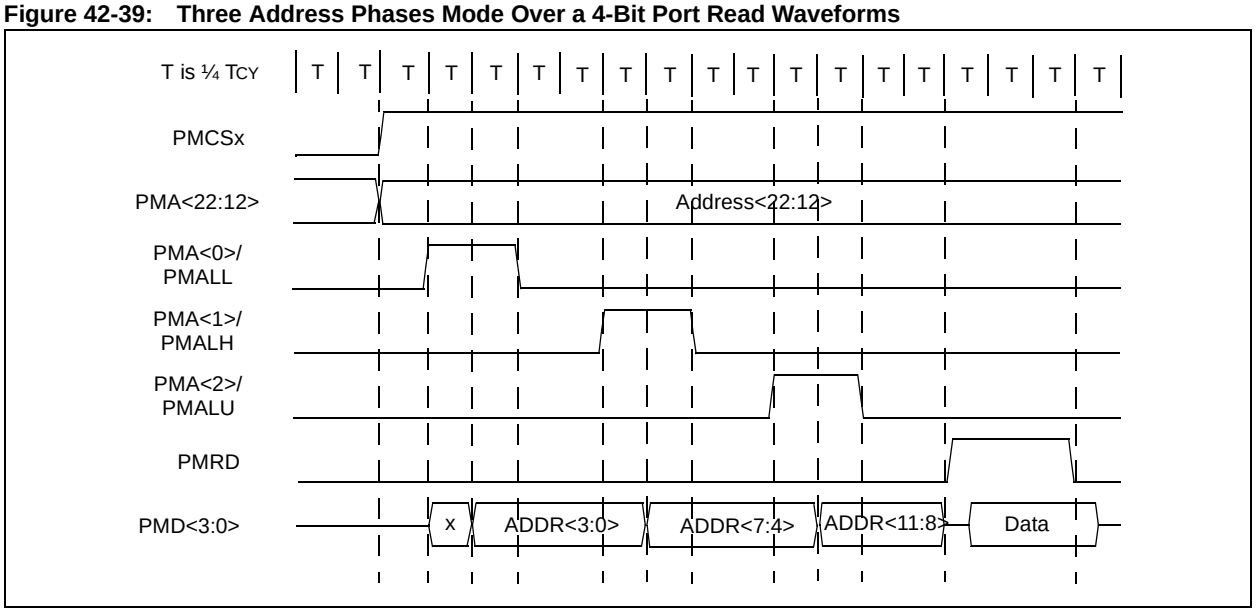
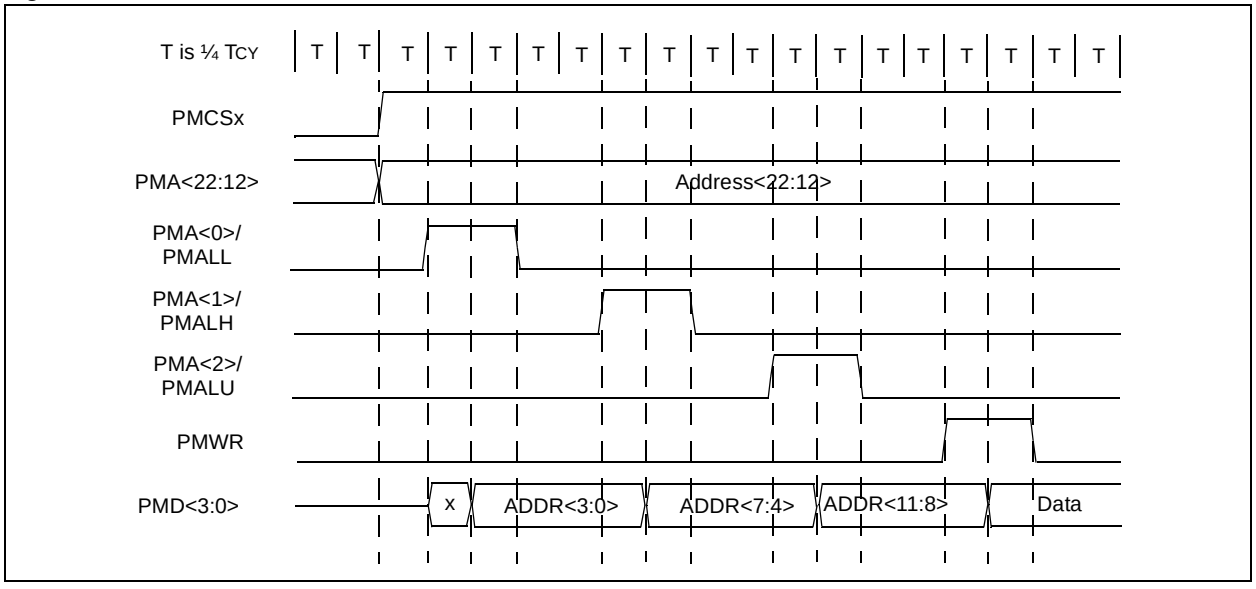


Figure 42-40: Three Address Phases Mode Over a 4-Bit Port Write Waveforms



42.4.1.10.9 Three Address Phases Mode over an 8-Bit Port

When ADRMUX<1:0> = 11 and PTSZ<1:0> = 00, all 23 address bits are multiplexed with data in three address phases. The PMA<0>, PMA<1> and PMA<2> pins are used to present the Address Latch Low (PMALL) Enable, Address Latch High (PMALH) Enable and Address Latch Upper (PMALU) Enable strobes, respectively. The read and write sequences take several cycles. During the first cycle, the lower eight bits of the address are presented on the data bus with the PMALL strobe active. During the second cycle, the next eight bits of the address are presented with the PMALH strobe active. During the third cycle, the upper seven bits of the address are presented with the PMALU strobe active. During the next cycles, the data is transmitted.

Timing for this mode is displayed in Figure 42-41 and Figure 42-42.

Figure 42-41: Three Address Phases Mode Over an 8-Bit Port Read Waveforms

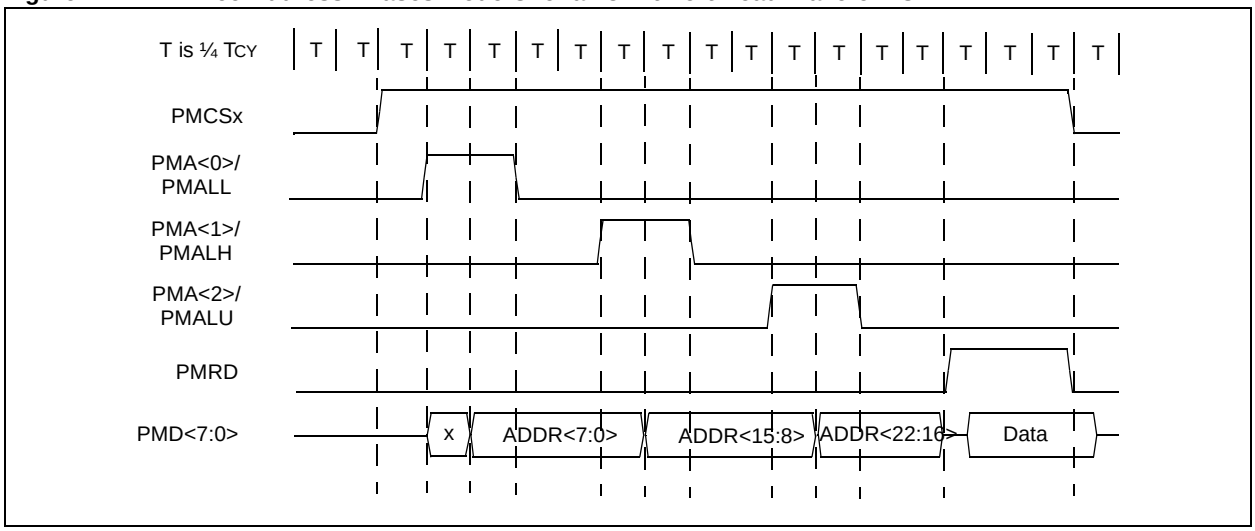
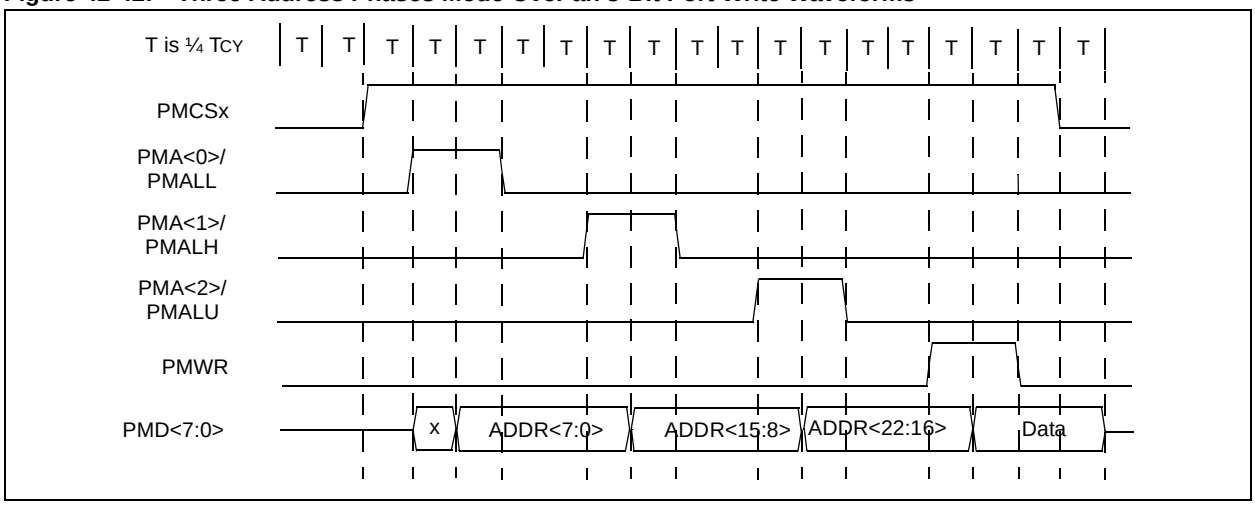


Figure 42-42: Three Address Phases Mode Over an 8-Bit Port Write Waveforms



42.4.1.10.10 The ALMODE Bit

When ALMODE = 1 (PMCON1<4>), control of the address strobes is put into “smart” mode, where only the relevant part of the address is driven out. An address part is considered relevant if it changes from the last access, and must be re-latched into an external address latch.

42.4.2 Read Operation

To perform a read on an external resource, the user simply performs a read from the corresponding address in the memory map. The EPMP breaks down the single read operation into the appropriate address and data phases (if required), stores the read data back from the external resource, and then drives the data back to the CPU.

The data presented back to the CPU is valid if the EPMP access time is equal to 1 TCY (acknowledgment is not used ACKM<1:0> = 00, address is not multiplexed ADRMUX<1:0> = 00 and data Wait states are set to minimum DWAITB<1:0> = 00, DWAITM<3:0> = 0000, DWAITE<1:0> = 00). Otherwise, either an interrupt driven or polling driven (BUSY bit in PMCON2) approach can be used to determine when the read cycle has completed. Once the data is available, it can be read from the PMDIN1 register. For a byte access the incoming data are placed in a low byte of PMDIN1 register for even byte address and in a high byte for the odd address.

Example 42-2: Read Operation Example (MPLAB® C30 Compiler)

```
#define EXTERNAL_RESOURCE_SIZE  0x20000L   // 2x128 Kbytes
#define CS_START_ADDRESS        0x200000L  // the address programmed for the EPMP chip select
                                           // in PMCSxBS register

// define an array in EPMP EDS space to access the external resource
__eds__ char pmp_data[EXTERNAL_RESOURCE_SIZE]
    __attribute__((space(eds), address(CS_START_ADDRESS), noload));
// temporary variable
char value;

 ...

// This code can be used if the EPMP access time is 1 Tcy.
value = pmp_data[2]; // read data from even byte address
value = pmp_data[3]; // read data from odd byte address

 ...

// This code can be used if the EPMP access time is more than 1 Tcy.
value = pmp_data[128];  // start an access at even byte address
                        // and get a dummy value
while(PMCON2bits.BUSY); // wait for the access is done
value = PMDIN1;         // read data from the low byte of PMDIN1

value = pmp_data[129];  // start an access at odd byte address
                        // and get a dummy value
while(PMCON2bits.BUSY); // wait for the access is done
value = PMDIN1>>8;      // read data from the high byte of PMDIN1
```

42.4.3 Write Operation

To perform a write on an external resource, users should simply perform a write to the corresponding address in the memory map. The EPMP breaks down the single write operation into the appropriate address and data phases (if required), and then performs the write operation. If the access time is more than 1 TCY the next operation may occur while the current write operation is pending. In this case either an interrupt driven or polling driven (BUSY bit in PMCON2) approach can be used to determine when the write cycle has completed, and the EPMP interface is available again.

Example 42-3: Write Operation Example (MPLAB® C30 Compiler)

```
#define EXTERNAL_RESOURCE_SIZE 0x20000L      // 2x128 Kbytes
#define CS_START_ADDRESS        0x200000L    // the address programmed for the EPMP chip select
                                             // in PMCS1BS register

// define an array in EPMP EDS space to access the external resource
__eds__ int pmp_data[EXTERNAL_RESOURCE_SIZE]
    __attribute__((eds, address(CS_START_ADDRESS), noload));
// temporary pointer
__eds__ int* pointer;

 ...

// This code can be used if the EPMP access time is 1 Tcy.
pointer = pmp_data;                          // assign pointer to the start address of the EPMP
                                             //  chip select region
*pointer++ = 1;                              // write '1' to external word address 0x000000
*pointer++ = 2;                              // write '2' to external word address 0x000001

 ...

// This code can be used if the EPMP access time is more than 1 Tcy.
pointer = pmp_data;                          // assign pointer to the start address of the EPMP
                                             //  chip select region
while(PMCON2bits.BUSY);                      // wait for the previous access is done
*pointer++ = 1;                              // write '1' to external word address 0x000000
while(PMCON2bits.BUSY);                      // wait for the previous access is done
*pointer++ = 2;                              // write '2' to external word address 0x000001
```

42.4.4 Parallel Master Port Status

42.4.4.1 THE BUSY BIT

In addition to the EPMP interrupt, a BUSY bit is provided in the PMCON2 register to indicate the status of the module. This bit is only used in Master mode.

While any read or write operation is in progress, the BUSY bit is set for all but the very last CPU cycle of the operation. In effect, if a single-cycle read or write operation is requested, the BUSY bit will never be active. This allows back-to-back transfers. It is only helpful if Wait states are enabled or multiplexed address/data is selected.

While the BUSY bit is set, any request by the user to initiate a new operation will be ignored. The user needs to try again after the BUSY flag is cleared.

42.4.4.2 THE TIMEOUT BIT

The TIMEOUT bit is provided in the PMCON2 register to indicate the status of the read or write operation. This bit is only used in Master mode when ACKM<1:0> = 01. While any read or write operation is aborted due to a time-out, the TIMEOUT bit is set and the EPMP interrupt is generated. This bit must be cleared by software (by writing a '0') before it can be set again.

42.4.4.3 THE ERROR BIT

REPEAT instruction with EDS to EDS moves is not supported. The ERROR bit (PMCON2<13>) indicates an error if REPEAT instruction is used to move external data. This bit must be cleared by software (by writing a '0') before it can be set again.

42.4.4.4 INTERRUPTS

The interrupt setting is configured using the IRQM<1:0> bits in the PMCON1 register.

When the EPMP module interrupt is enabled (IRQM<1:0> = 01) for the Master mode, the module will interrupt on any combination of the following:

- Interrupt due to a time-out if an external acknowledgment is used
- Interrupt after every completed read or write operation

42.5 ALTERNATE MASTER

On select PIC24F devices, the EPMP can be configured to allow another master (aside from the CPU) to control the port's operation and use its I/O pins. An example is the advanced graphics subsystem. This other system is known as the "Alternate Master".

Alternate Master operation is determined by the MSTSEL<1:0> bits (PMCON2<9:8>), as follows:

- When MSTSEL<1:0> = 00 and CURMST = 1, the CPU has complete control over the EPMP, and the Alternate Master has no access to the EPMP I/O pins.
- When MSTSEL<1:0> = 01 and CURMST = 0, the Alternate Master has complete control over the EPMP, and the CPU has no access to the EPMP I/O pins.
- When MSTSEL<1:0> = 11 and CURMST = 0, the Alternate Master bypasses the EPMP altogether, and accesses the EPMP I/O pins directly. In this case, the CPU has no access to the EPMP I/O pins, but the configuration of the EPMP I/O pins (i.e., polarity, chip select address ranges, etc.) is still governed by the settings in the EPMP.

Note:	Alternate Master operation is not available on all devices with the EPMP. Refer to the specific device data sheet to see which control options are implemented.

42.5.1 Switching from CPU EPMP access to Alternate Master

1. Wait until the current EPMP transaction completes by polling BUSY bit (PMCON2<15>).
2. Set the MSTSEL<1:0> register bits to 01 or 11.
3. After CURMST bit (PMCON2<10>) is cleared, the Alternate Master has an access to EPMP or EPMP I/O pins.

42.5.2 Switching from Alternate Master to CPU EPMP access

1. Set the MSTSEL<1:0> register bits to 00.
2. Wait until the CURMST bit (PMCON2<10>) is set.
3. The CPU may now access the EPMP through the EDS interface.

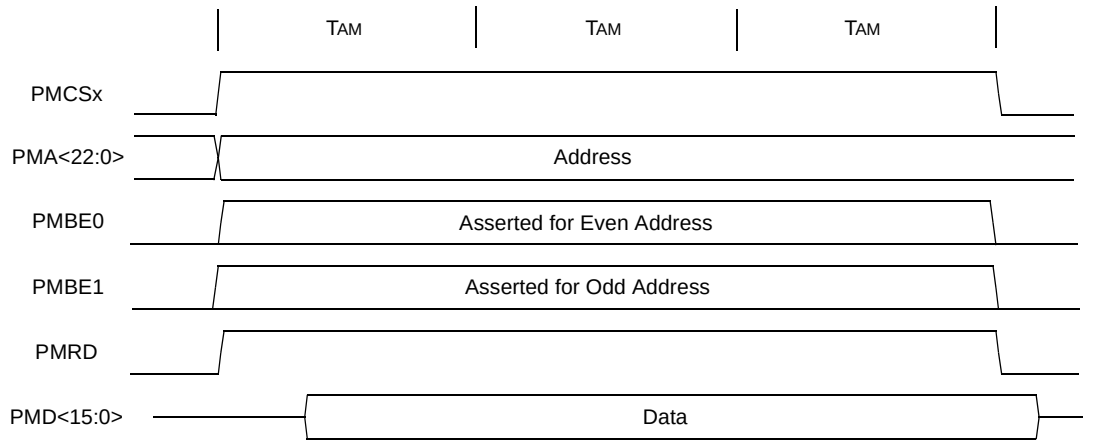
42.5.3 Alternate Master Direct Access of EPMP I/Os

The Alternate Master is capable of directly controlling the external pins, when a compatible external memory device such as an SRAM is present at the pins. This is done by setting MSTSEL<1:0> to '11'. It provides a faster access to external memories when throughput or latency is an issue. The configuration of the EPMP I/O pins is done through the EPMP Configuration registers. In this mode the address cannot be multiplexed with data (ADRMUX<1:0> bits in PMCON1 register must be set to '00') and port size is fixed to 16-bit (PTPZ<1:0> bits in PMCSxCF registers must be set to '10'). When the Alternate Master is directly driving the I/O pads, settings such as polarity and strobe mode, will be determined by the EPMP configuration (CSP, WRSP, RDSP and SM bits in PMCSxCF registers).

The control and address signals associated with this mode must be enabled in PMCON3 and PMCON4 registers. The chip select's address ranges must be defined in registers PMCON2, PMCS1BS and PMCS2BS. PMBE0 and PMBE1 signals indicate low/high byte for 8-bit access. The user has control over the duration of the Alternate Master transactions, on a chip select by chip select basis, by configuring the Wait states as multiples of Tam (Alternate Master cycle period). The Tam period value can be found in the device data sheet. The number of Wait states is defined with AMWAIT<2:0> bits in PMCSxMD registers. The data Wait states are not used in this mode (DWAITB<1:0>, DWAITM<3:0>, DWAITE<1:0> bits in PMCSxMD registers are ignored).

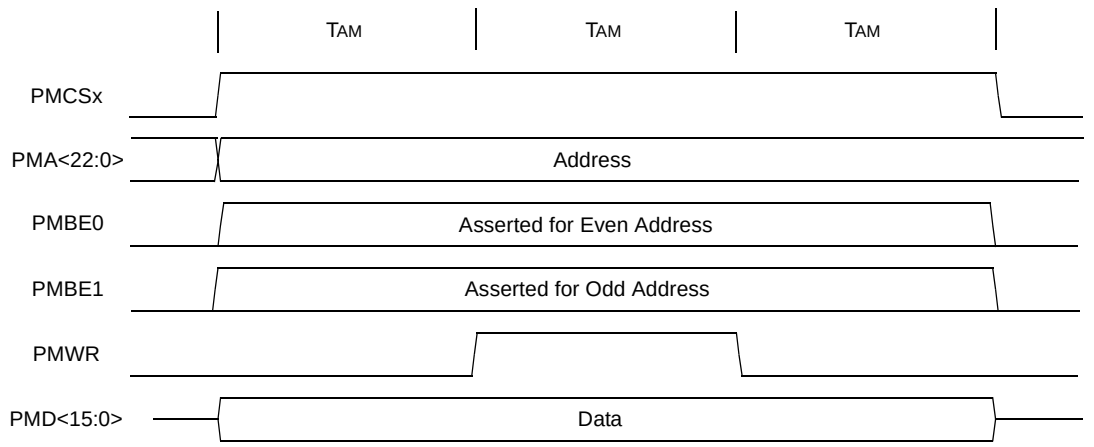
Timing for this mode is displayed in Figure 42-43, Figure 42-44, Figure 42-45 and Figure 42-46.

Figure 42-43: Alternate Master Direct 8-Bit Access Read Waveforms



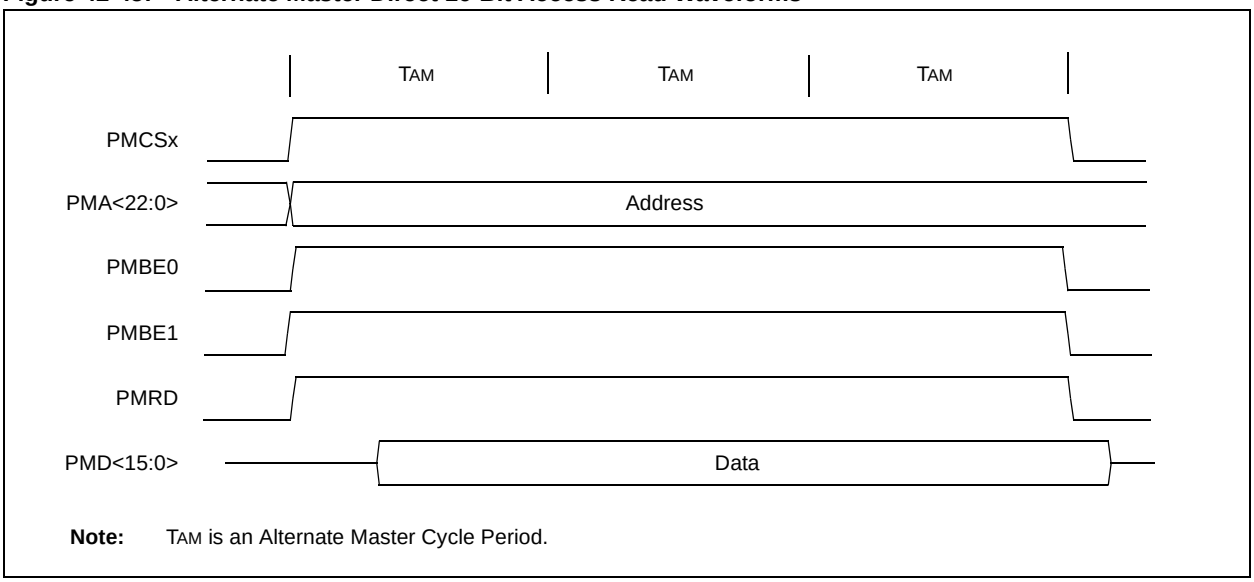
Note: TAM is an Alternate Master Cycle Period.

Figure 42-44: Alternate Master Direct 8-Bit Access Write Waveforms



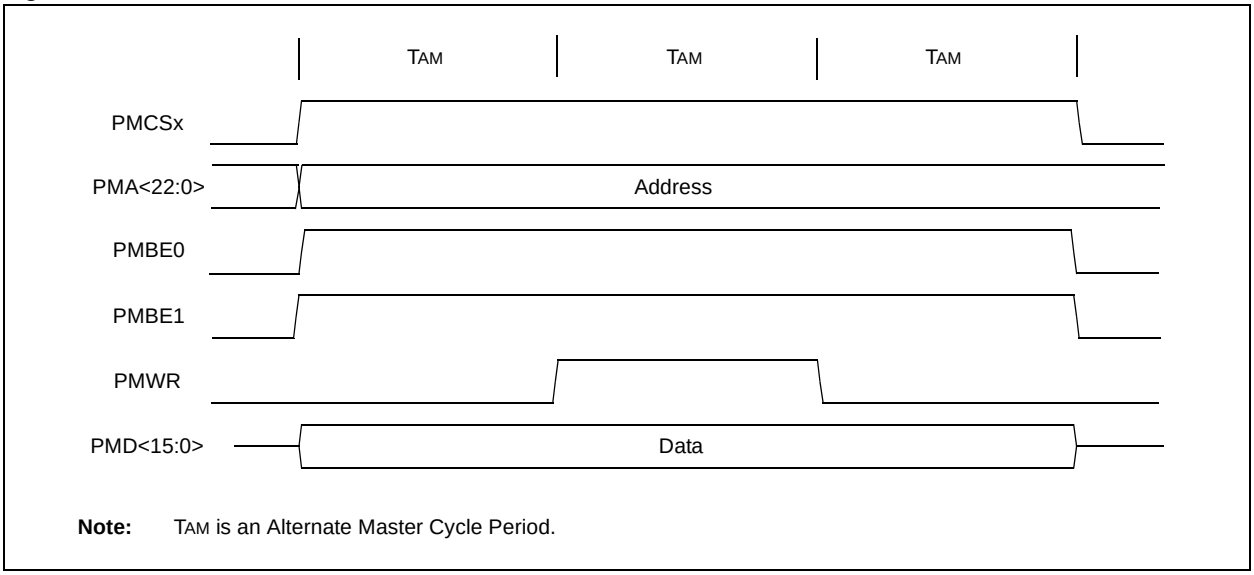
Note: TAM is an Alternate Master Cycle Period.

Figure 42-45: Alternate Master Direct 16-Bit Access Read Waveforms



Note: TAM is an Alternate Master Cycle Period.

Figure 42-46: Alternate Master Direct 16-Bit Access Write Waveforms



Note: TAM is an Alternate Master Cycle Period.

42.6 OPERATION IN POWER-SAVING MODES

The PIC24F family of devices has three power modes: the Normal Operational (Full-Power) mode, and the two Power-Saving modes, invoked by the PWRSAV instruction. Depending on the mode selected, entering a Power-Saving mode may also affect the operation of the module.

42.6.1 Sleep Mode

When the device enters Sleep mode, the system clock is disabled. The consequences of Sleep mode depend on which mode the module is configured at the time that Sleep mode is invoked.

42.6.1.1 MASTER MODE OPERATION

If the microcontroller enters Sleep mode while the module is operating in Master mode, EPMP operation will be suspended in its current state until clock execution resumes. As this may cause unexpected control pin timings, users should avoid invoking Sleep mode when continuous use of the module is needed.

42.6.1.2 SLAVE MODE OPERATION

While the module is inactive, but enabled for any Slave mode operation, any read or write operations occurring at that time will be able to complete without the use of the microcontroller clock. Once the operation is completed, the module will issue an interrupt according to the setting of the IRQMx bits. This interrupt can wake the device from Sleep mode.

42.6.2 Idle Mode

When the device enters Idle mode, the system clock sources remain functional. The PSIDL bit (PMCON1<13>) selects whether the module will stop or continue functioning on Idle. If PSIDL = 1, the module will behave the same way as it does in Sleep mode (i.e., slave reception is still possible even though the module clocks are not available, and the Master mode is suspended). If PSIDL = 0 (default), the module will continue operation in Idle mode. The current transaction in both Master and Slave modes will complete and issue an interrupt.

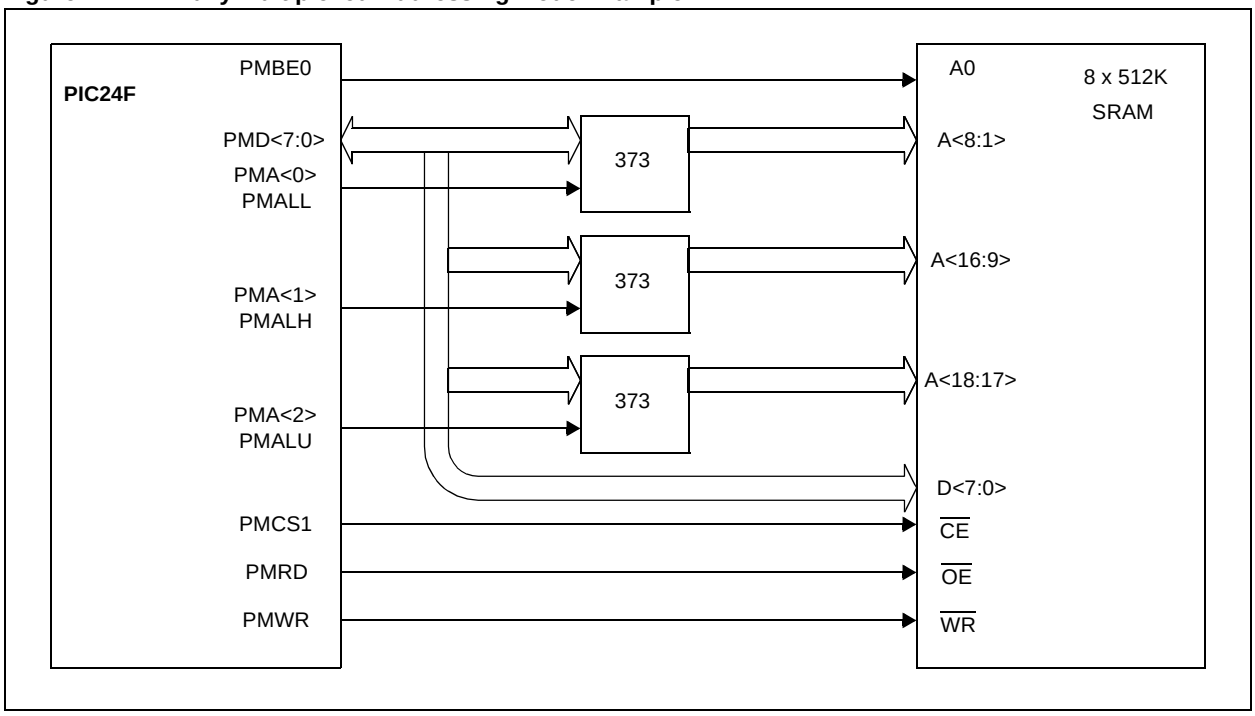
42.7 APPLICATION EXAMPLES

This section introduces some potential applications for the EPMP module.

42.7.1 Fully Multiplexed Address for Memory or Peripheral

Figure 42-47 and Example 42-4 demonstrate the hook up of an 8-bit memory or another addressable peripheral in Three Address Phases mode. Consequently, this mode achieves the best pin saving from the microcontroller perspective. However, for this configuration, there needs to be some external latches to maintain the address.

Figure 42-47: Fully Multiplexed Addressing Mode Example



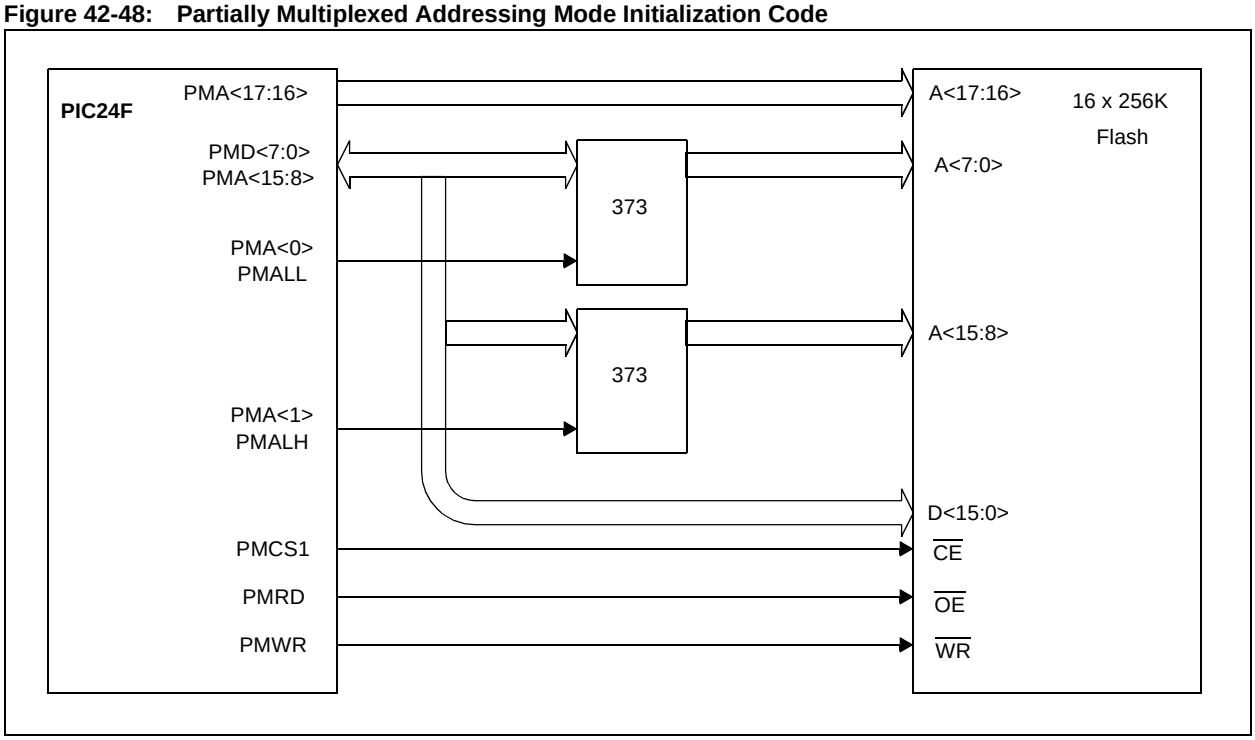
Example 42-4: Fully Multiplexed Addressing Mode Initialization Code

```
PMCON1bits.ADRMUX = 0b11;      // address is multiplexed with data using 3 address phases
PMCON1bits.MODE = 0b11;        // master mode
PMCON1bits.CSF = 0b00;         // PMCS1 pin used for chip select 1
                               // PMCS2 pin used for chip select 2
PMCON1bits.ALP = 1;            // set address latch strobes to high active level
PMCON1bits.ALMODE = 0;         // "smart" address strobes are not used
PMCON1bits.BUSKEEP = 0;        // bus keeper is not used

PMCS1BS = 0x2000;              // set CS1 start address to the start of the EPMP EDS space (0x200000),
                               // see this value in the device datasheet
PMCS2BS = 0x2800;              // set CS1 end address and CS2 start address to cover a 512KBytes region
                               // for CS1 (0x280000 EPMP EDS address)
                              // no need to set CS2 end address (RADDR) if CS2 is not used

PMCON3bits.PTWREN = 1;         // enable write strobe port
PMCON3bits.PTRDEN = 1;         // enable read strobe port
PMCON3bits.PTBE0EN = 1;        // enable byte enable port
PMCON3bits.AWAITM = 0b00;      // set address latch pulses width to 1/2 Tcy
PMCON3bits.AWAITE = 0;         // set address hold time to 1/4 Tcy

PMCON4bits.PTEN0 = 1;          // enable PMA0/ALL port
PMCON4bits.PTEN1 = 1;          // enable PMA1/ALH port
PMCON4bits.PTEN2 = 1;          // enable PMA2/ALU port

PMCS1CFbits.CSDIS = 0;         // enable CS1
PMCS1CFbits.CSP = 0;           // CS1 active low
PMCS1CFbits.CSPTEN = 1;        // enable CS1 port
PMCS1CFbits.BEP = 0;           // byte enable active low
PMCS1CFbits.WRSP = 0;          // write strobe active low
PMCS1CFbits.RDSP = 0;          // read strobe active low
PMCS1CFbits.SM = 0;            // read and write strobes on separate lines
PMCS1CFbits.PTSZ = 0b00;       // data bus width is 8-bit

PMCS1MDbits.ACKM = 0b00;       // PMACK is not used
PMCS1MDbits.DWAITB = 0b01;     // data setup before read/write strobe is 1+1/4 Tcy
PMCS1MDbits.DWAITM = 0b0100;   // read/write strobe width 3+1/2Tcy for write
                               // 3+3/4 Tcy for read
PMCS1MDbits.DWAITB = 0b01;     // data hold after read/write strobe is 1+1/4 Tcy for write
                               // 1 Tcy for read

PMCS2CFbits.CSDIS = 1;         // disable CS2 functionality

PMCON1bits.PMPEN = 1;          // enable EPMP
```

42.7.2 Partially Multiplexed Address for Memory or Peripheral

Partial multiplexing implies using more pins; however, for a few extra pins, some extra performance can be achieved. Figure 42-48 and Example 42-5 show an example of a memory or peripheral that is partially multiplexed with an external latch in One Address Phase mode.

Figure 42-48: Partially Multiplexed Addressing Mode Initialization Code



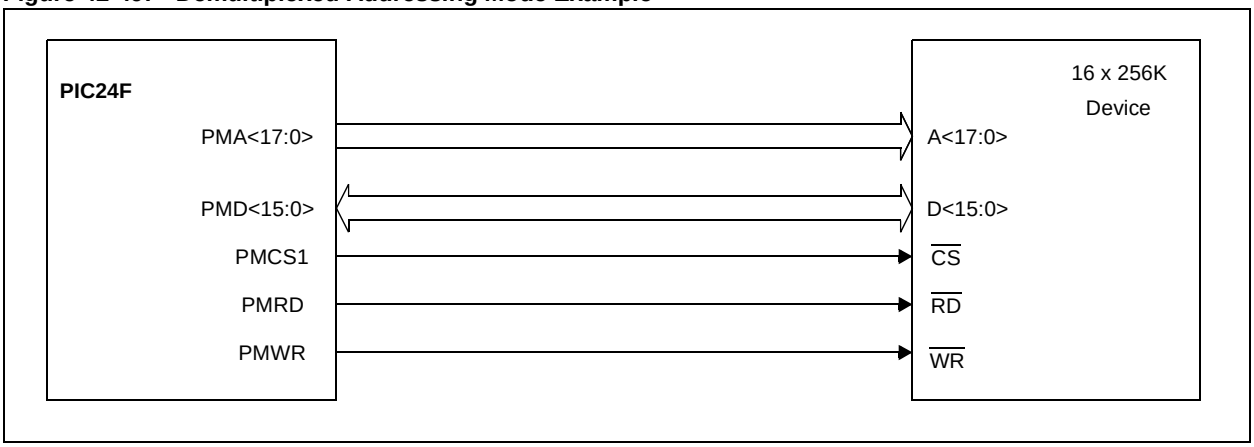
Example 42-5: Partially Multiplexed Addressing Mode Initialization Code

```
PMCON1bits.ADRMUX = 0b01;      // address is multiplexed with data using 1 address phases
PMCON1bits.MODE = 0b11;        // master mode
PMCON1bits.CSF = 0b00;         // PMCS1 pin used for chip select 1
                               // PMCS2 pin used for chip select 2
PMCON1bits.ALP = 1;            // set address latch strobes to high active level
PMCON1bits.ALMODE = 0;         // "smart" address strobes are not used
PMCON1bits.BUSKEEP = 0;        // bus keeper is not used

PMCS1BS = 0x2000;              // set CS1 start address to the start of the EPMP EDS space (0x200000),
                               // see this value in the device datasheet
PMCS2BS = 0x2800;              // set CS1 end address and CS2 start address to cover a 2x256
                               // KBytes region for CS1 (0x280000 EPMP EDS address)
                               // no need to set CS2 end address (RADDR) if CS2 is not used

PMCON3bits.PTWREN = 1;         // enable write strobe port
PMCON3bits.PTRDEN = 1;         // enable read strobe port
PMCON3bits.AWAITM = 0b00;      // set address latch pulses width to 1/2 Tcy
PMCON3bits.AWAITE = 0;         // set address hold time to 1/4 Tcy

PMCON4bits.PTEN0 = 1;          // enable PMA0/ALL port
PMCON4bits.PTEN1 = 1;          // enable PMA1/ALH port
PMCON3bits.PTEN16 = 1;         // enable PMA16 port
PMCON3bits.PTEN17 = 1;         // enable PMA17 port

PMCS1CFbits.CSDIS = 0;         // enable CS1
PMCS1CFbits.CSP = 0;           // CS1 active low
PMCS1CFbits.CSPTEN = 1;        // enable CS1 port
PMCS1CFbits.BEP = 0;           // byte enable active low
PMCS1CFbits.WRSP = 0;          // write strobe active low
PMCS1CFbits.RDSP = 0;          // read strobe active low
PMCS1CFbits.SM = 0;            // read and write strobes on separate lines
PMCS1CFbits.PTSZ = 0b10;       // data bus width is 16-bit

PMCS1MDbits.ACKM = 0b00;       // PMACK is not used
PMCS1MDbits.DWAITB = 0b01;     // data setup before read/write strobe is 1+1/4 Tcy
PMCS1MDbits.DWAITM = 0b0100;   // read/write strobe width 3+1/2Tcy for write
                               // 3+3/4 Tcy for read
PMCS1MDbits.DWAITB = 0b01;     // data hold after read/write strobe is 1+1/4 Tcy for write
                               // 1 Tcy for read

PMCS2CFbits.CSDIS = 1;         // disable CS2 functionality

PMCON1bits.PMPEN = 1;          // enable EPMP
```

42.7.3 Demultiplexed Address Example

Figure 42-49 and Example 42-6 illustrate the connection to 16-bit addressable device in Demultiplexed mode.

Figure 42-49: Demultiplexed Addressing Mode Example



Example 42-6: Demultiplexed Addressing Mode Initialization Code

```
PMCON1bits.ADRMUX = 0b00;      // address is demultiplexed
PMCON1bits.MODE = 0b11;        // master mode
PMCON1bits.CSF = 0b00;         // PMCS1 pin used for chip select 1
                               // PMCS2 pin used for chip select 2
PMCON1bits.BUSKEEP = 0;        // bus keeper is not used

PMCS1BS = 0x2000;              // set CS1 start address to the start of the EPMP EDS space (0x200000),
                               // see this value in the device datasheet
PMCS2BS = 0x2800;              // set CS1 end address and CS2 start address
                               // to cover a 2x256 KBytes region for CS1 (0x280000 EPMP EDS address)
                               // no need to set CS2 end address (RADDR) if CS2 is not used

PMCON3bits.PTWREN = 1;         // enable write strobe port
PMCON3bits.PTRDEN = 1;         // enable read strobe port
PMCON3bits.PTEN16 = 1;         // enable PMA16
PMCON3bits.PTEN17 = 1;         // enable PMA17

PMCON4 = 0xffff;               // enable PMA<15:0> ports

PMCS1CFbits.CSDIS = 0;         // enable CS1
PMCS1CFbits.CSP = 0;           // CS1 active low
PMCS1CFbits.CSPTEN = 1;        // enable CS1 port
PMCS1CFbits.BEP = 0;           // byte enable active low
PMCS1CFbits.WRSP = 0;          // write strobe active low
PMCS1CFbits.RDSP = 0;          // read strobe active low
PMCS1CFbits.SM = 0;            // read and write strobes on separate lines
PMCS1CFbits.PTSZ = 0b10;       // data bus width is 16-bit

PMCS1MDbits.ACKM = 0b00;       // PMACK is not used
PMCS1MDbits.DWAITB = 0b01;     // data setup before read/write strobe is 1+1/4 Tcy
PMCS1MDbits.DWAITM = 0b0100;   // read/write strobe width 3+1/2Tcy for write
                               // 3+3/4 Tcy for read
PMCS1MDbits.DWAITB = 0b01;     // data hold after read/write strobe is 1+1/4 Tcy for write
                               // 1 Tcy for read

PMCS2CFbits.CSDIS = 1;         // disable CS2 functionality

PMCON1bits.PMPEN = 1;          // enable EPMP
```

42.8 AC ELECTRICAL SPECIFICATIONS

Figure 42-50: Parallel Slave Port Timing Diagram

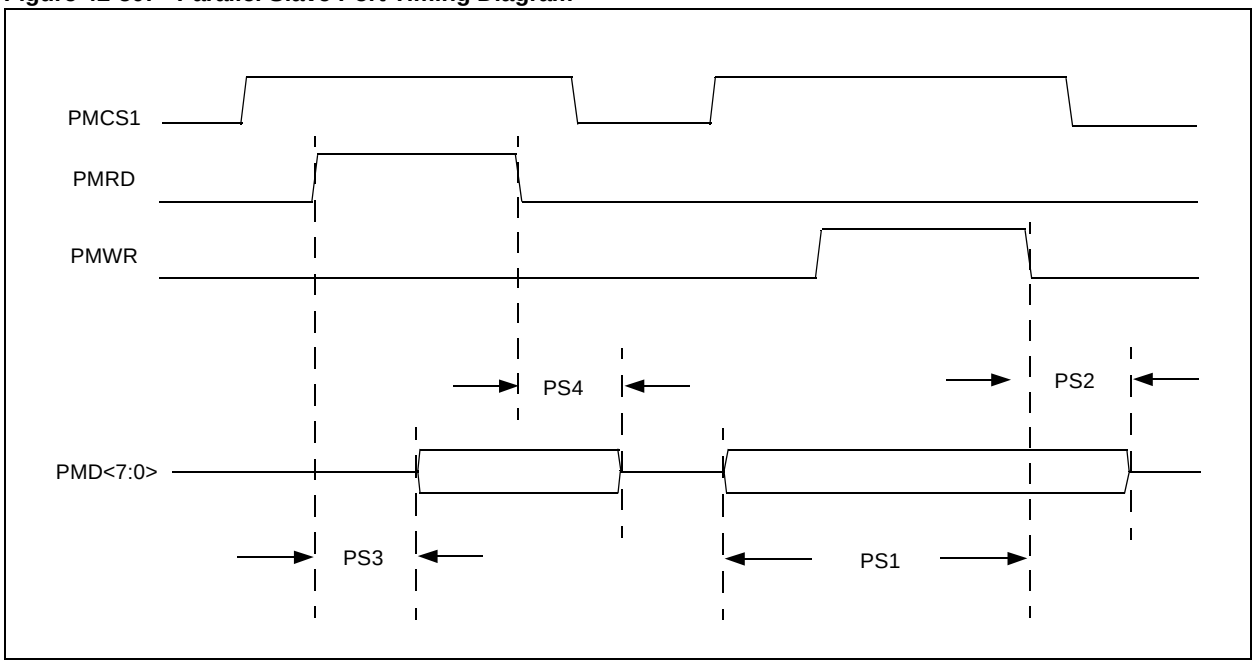
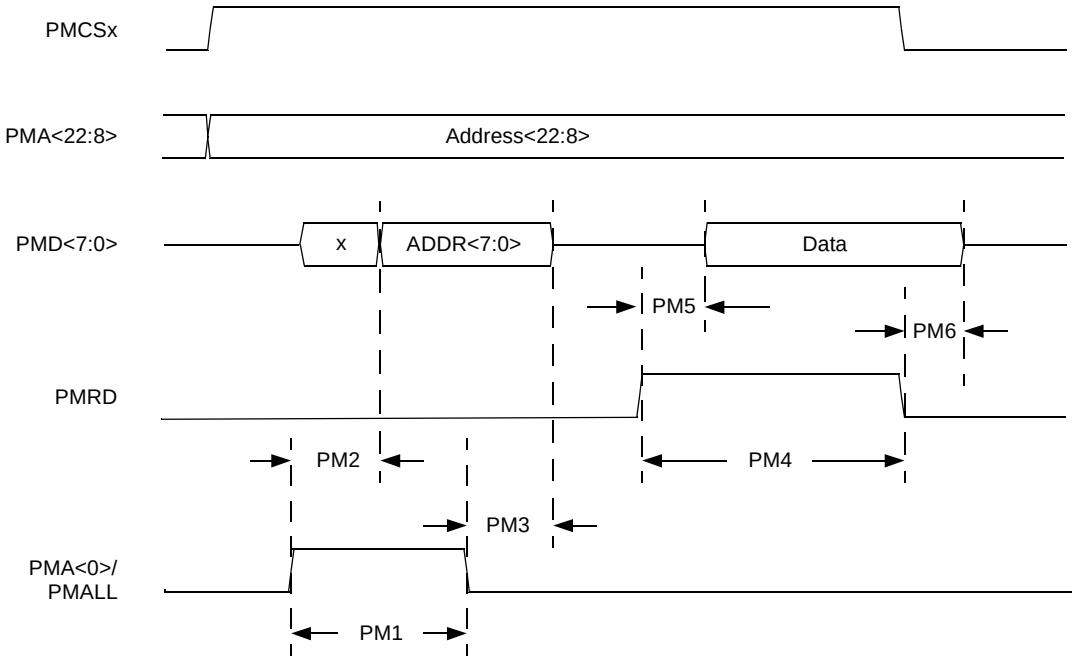


Table 42-7: Parallel Slave Port Timing

AC CHARACTERISTICS		Operating conditions: from 2.0V to 3.6V. Operating temperature: from -40°C to +85°C. (Unless otherwise stated)			
Param. No.	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**
PS1	Data Invalid before PMWR or PMCS1 Inactive (set-up time)	20	—	—	ns
PS2	PMWR or PMCS1 Inactive to Data In Invalid (hold time)	20	—	—	ns
PS3	PMRD and PMCS1 Active to Data Out Valid	—	—	80	ns
PS4	PMRD Active or PMCS1 Inactive to Data Out Invalid	10	—	30	ns

Figure 42-51: Enhanced Parallel Master Port Read Timing Diagram

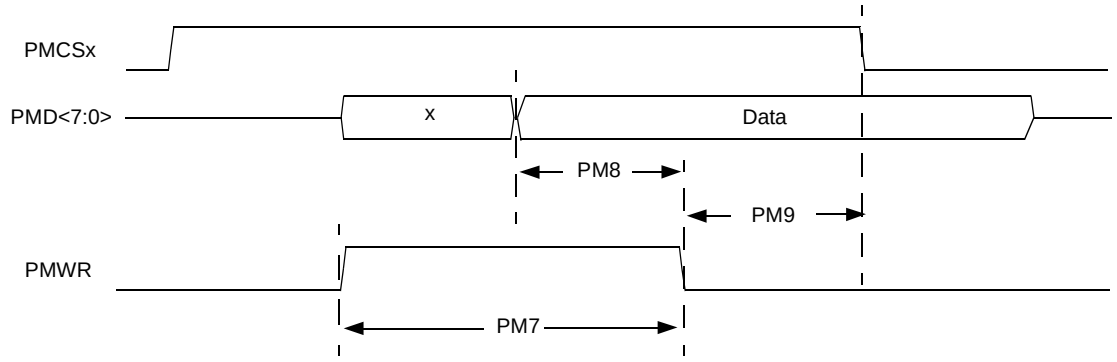


Note: This timing is valid for other data port widths and address multiplexing modes.

Table 42-8: Enhanced Parallel Master Port Read Timing

AC CHARACTERISTICS		Operating conditions: from 2.0V to 3.6V. Operating temperatures: from -40°C to +85°C. (Unless otherwise stated)			
Param. No.	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**
PM1	PMALL/PMALH/PMALU Pulse-Width	—	0.5 TCY	—	ns
PM2	Address Out Valid to PMALL/PMALH/PMALU Invalid (address set-up time)	0.25 TCY	—	—	ns
PM3	PMALL/PMALH/PMALU Invalid to Address Out Invalid (address hold time)	0.25 TCY	—	—	ns
PM4	PMRD Pulse-Width	—	0.75 TCY	—	ns
PM5	Data In to PMRD or PMENB Active state	—	—	0.75 TCY	ns
PM6	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	—	0.25 TCY	ns

Figure 42-52: Enhanced Parallel Master Port Write Timing Diagram



Note: This timing is valid for other data port widths.

Table 42-9: Enhanced Parallel Master Port Write Timing

AC CHARACTERISTICS		Operating conditions: from 2.0V to 3.6V. Operating temperature: from -40°C to +85°C. (Unless otherwise stated)			
Param. No.	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**
PM7	PMWR Pulse-Width	—	0.5 TCY	—	ns
PM8	Data Out Valid before PMWR or PMENB goes Inactive (data set-up time)	0.25 TCY	—	—	ns
PM9	PMWR or PMENB Invalid to Data Out Invalid (data hold time)	0.25 TCY	—	—	ns

42.9 REGISTER MAPS

Table 42-10 lists all EPMP module-related registers.

Table 42-10: Enhanced Parallel Master/Slave Port Register Map(1)

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON1	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	—	MODE1	MODE0	CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0	0000
PMCON2	BUSY	—	ERROR	TIMEOUT	AMREQ(2)	CURMST(2	MSTSEL1(2)	MSTSEL0(2)	RADDR23	RADDR22	RADDR21	RADDR20	RADDR19	RADDR18	RADDR17	RADDR16	0000
PMCON3	PTWREN	PTRDEN	PTBE1EN	PTBE0EN	—	AWAITM1	AWAITM0	AWAITE	—	PTEN22	PTEN21	PTEN20	PTEN19	PTEN18	PTEN17	PTEN16	0000
PMCON4	PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	0000
PMCS1CF	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS1BS	BASE23	BASE22	BASE21	BASE20	BASE19	BASE18	BASE17	BASE16	BASE15	—	—	—	BASE11	—	—	—	0200
PMCS1MD	ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMCS2CF	CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM	ACKP	PTSZ1	PTSZ0	—	—	—	—	—	0000
PMCS2BS	BASE23	BASE22	BASE21	BASE20	BASE19	BASE18	BASE17	BASE16	BASE15	—	—	—	BASE11	—	—	—	0600
PMCS2MD	ACKM1	ACKM0	AMWAIT2	AMWAIT1	AMWAIT0	—	—	—	DWAITB1	DWAITB0	DWAITM3	DWAITM2	DWAITM1	DWAITM0	DWAITE1	DWAITE0	0000
PMDIN1	Parallel Port Data In Register 1																0000
PMDIN2	Parallel Port Data In Register 2																0000
PMDOUT1	Parallel Port Data Out Register 1																0000
PMDOUT2	Parallel Port Data Out Register 2																0000
PMSTAT	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F
PADCFG1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RTSECSEL	PMPTTL	0000

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the Enhanced Parallel Master Port module.

Note 1: Refer to the product device data sheet for specific Core register map details.

2: Unimplemented in devices that do not use Alternate master mode operation. Refer to the specific device data sheet for more information.

42.10 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Enhanced Parallel Master Port are:

Title	Application Note #
No related application notes at this time.	

Note: Visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

42.11 REVISION HISTORY

Revision A (November 2009)

This is the initial released version of this document.

Revision B (March 2011)

Revises the footnotes in Register 42-2, Register 42-5 and Register 42-6 to reflect different implementations of the module in newer PIC24F devices.

Changes the introduction to **Section 42.5 “Alternate Master”** to reflect the absence of Alternate Master operation in some PIC24F devices.

Corrects code examples shown in Example 42-2, Example 42-3, Example 42-4, Example 42-5 and Example 42-6.

Other minor typographic fixes throughout the document.

NOTES:

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