Section 40. Reset with Programmable Brown-out Reset

HIGHLIGHTS

This section of the manual contains the following topics:

40.1 INTRODUCTION

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Pin Reset
- SWR: RESET Instruction
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode/Uninitialized W Register Reset

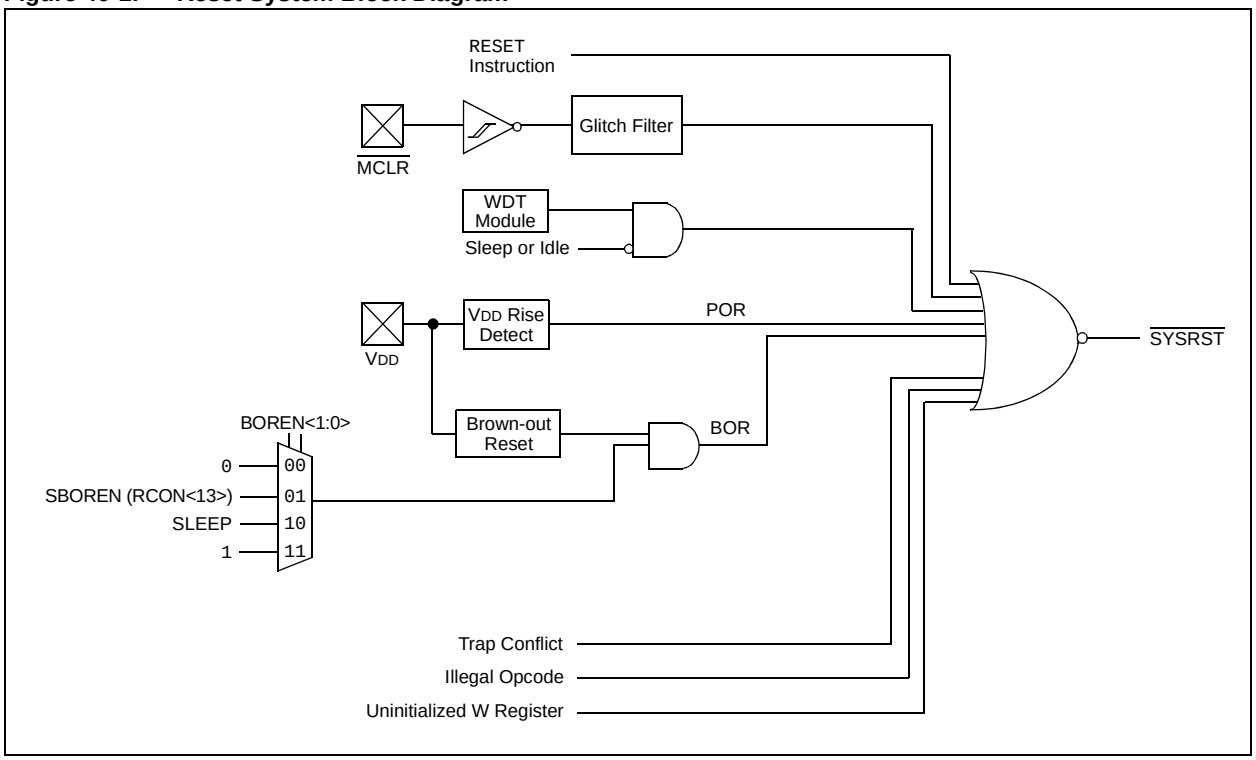
Figure 40-1 displays a simplified block diagram of the Reset module. Any active source of Reset will make the SYSRST signal active. Many registers associated with the CPU and peripherals are forced to a known "Reset state". Most registers are unaffected by a Reset; their status is unknown on Power-on Reset (POR) and unchanged by all other Resets.

Note:	Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Resets will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 40-1). A Power-on Reset will clear all bits, except for the BOR and POR bits (RCON<1:0>), which are set. Users may set or clear any of the bits at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset.

The RCON register also has other bits associated with the Watchdog Timer (WDT) and device power-saving states. For more information on the function of these bits, refer to **Section 40.11.1 "Using the RCON Status Bits"**.

Figure 40-1: Reset System Block Diagram



Register 40-1: RCON: Reset Control Register(1)

R/W-0	R/W-0	R/W-0	U-0	U-0	R/C-0	U-0	R/W-0
TRAPR	IOPUWR	SBOREN	—	—	DPSLP	—	PMSLP
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN(2)	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or an uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13 **SBOREN:** Software Enable/Disable of BOR bit
1 = BOR is turned on in software
0 = BOR is turned off in software

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **DPSLP:** Deep Sleep Mode Flag bit
1 = Deep Sleep has occurred
0 = Deep Sleep has not occurred

bit 9 **Unimplemented:** Read as '0'

bit 8 **PMSLP:** Program Memory Power During Sleep/Idle bit
1 = Program memory bias voltage remains powered during Sleep/Idle
0 = Program memory bias voltage is powered down during Sleep/Idle

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

Register 40-1: RCON: Reset Control Register(1) (Continued)

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred; the BOR is also set after a Power-on Reset
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

40.2 CLOCK SOURCE SELECTION AT RESET

If clock switching is enabled (OSWEN), the system clock source at device Reset is chosen, as displayed in Table 40-1. If clock switching is disabled, the system clock source is always selected according to the oscillator Configuration bits. Refer to **Section 6. "Oscillator"** for further details.

Table 40-1: Oscillator Selection vs. Type of Reset (Clock Switching Enabled)

Reset Type	Clock Source Selected Based on
POR	Oscillator Configuration Bits FNOSC<2:0>
BOR	
$\overline{\text{MCLR}}$	COSC Control bits OSCCON<14:12>
WDTR	
SWR	
TRAPR	
IOPUWR	

40.3 POWER-ON RESET (POR)

The POR monitors the core power supply for adequate voltage levels to ensure proper chip operation. There are two threshold voltages associated with a POR. The first voltage is the device threshold voltage, VPOR. The device threshold voltage is the voltage at which the POR module becomes operable. The second voltage associated with a POR event is the POR circuit threshold voltage. Once the correct threshold voltage is detected, a power-on event occurs and the POR module hibernates to minimize current consumption.

A power-on event generates an internal POR pulse when a VDD rise is detected. The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR pulse. In particular, VDD must fall below VPOR before a new POR is initiated. For more information on the VPOR and VDD rise rate specifications, refer to the **"Electrical Characteristics"** section of the specific device data sheet.

The POR pulse resets the POR timer and places the device in the Reset state. The POR also selects the device clock source identified by the oscillator Configuration bits.

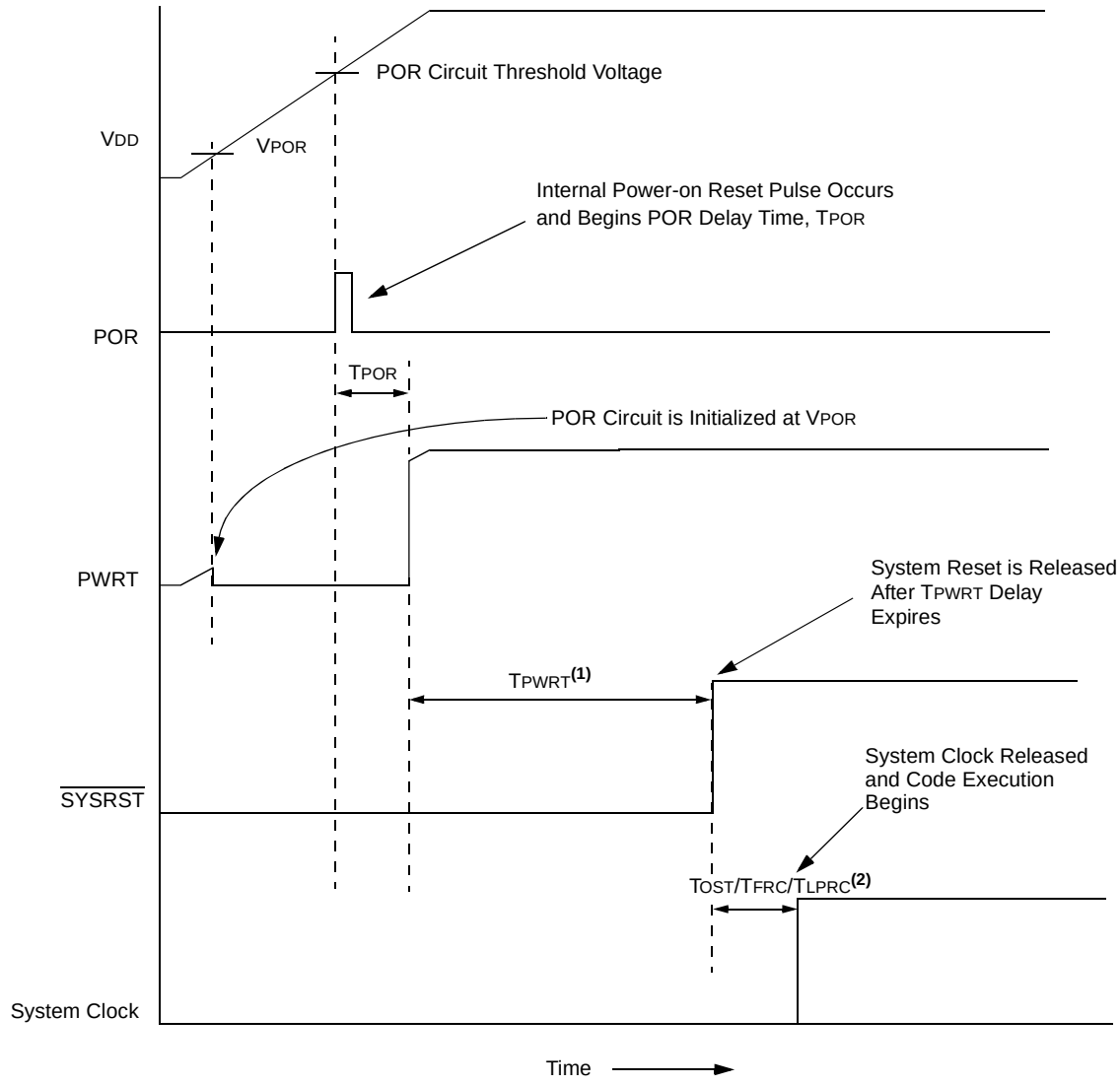
After the POR pulse is generated, the POR circuit inserts a small delay, the TPOR, which is nominally 5 μs and ensures that internal device bias circuits are stable. After the expiration of TPOR, a delay, TPWRT, is inserted if enabled in the Configuration Word.

TPWRT is applied any time the device resumes operation after a power-down if the Power-up Timer (PWRT) is enabled. The PWRT adds a fixed 64 ms nominal delay at device start-up. The PWRT is used to extend the duration of a power-up sequence to allow time for the VDD supply to stabilize before the core begins to run.

The power-on event will set the BOR and POR status bits (RCON<1:0>). Once all of the delays have expired, the system clock is released and code execution can begin.

Refer to **Section 40.14 "Electrical Specifications"** for more information on the values of the delay parameters.

Figure 40-2: POR Module Timing Sequence for Rising VDD



Note 1: TPWRT is inserted if the Power-up Timer is enabled.

2: The delay is the function of the oscillator used, the frequency selected and the VDD provided. This delay can be anywhere within the gray area shown in the figure (indicated by dotted arrow). Refer to Table 40-5 for details to determine which delay applies.

Note: When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device will not function correctly. The user must ensure that the delay between the time power is first applied and the time $\overline{\text{SYSRST}}$ becomes inactive is long enough to get all operating parameters within the specification.

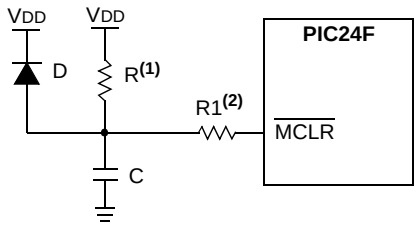
40.3.1 Using the POR Circuit

To take advantage of the POR circuit, just tie the MCLR pin directly to VDD. This will eliminate external RC components usually needed to create a POR delay. A minimum rise time for VDD is required. Refer to the **"Electrical Characteristics"** section of the specific device data sheet for more information.

Depending on the application, a resistor may be required between the MCLR pin and VDD. This resistor can be used to decouple the MCLR pin from a noisy power supply rail.

Figure 40-3 displays a possible POR circuit for a slow power supply ramp up. The external POR circuit is only required if the device would exit Reset before the device VDD is in the valid operating range. The diode, D, helps discharge the capacitor quickly when VDD powers down.

Figure 40-3: External Power-on Reset Circuit (for Slow VDD Rise Time)



Note 1: The value of R should be low enough so that the voltage drop across it does not violate the VIH specification of the MCLR pin.

2: R1 limits any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

40.4 MCLR RESET

Whenever the MCLR pin is driven low, the device asynchronously asserts SYSRST, provided the input pulse on MCLR is longer than a certain minimum width, SY10 (see **Section 40.14 "Electrical Specifications"**). When the MCLR pin is released, SYSRST is also released. The Reset vector fetch starts without delay, starting from the SYSRST release. The processor continues to use the existing clock source that was in use before the MCLR Reset occurred. The EXTR status bit (RCON<7>) is set to indicate the MCLR Reset.

40.5 SOFTWARE RESET INSTRUCTION (SWR)

Whenever the RESET instruction is executed, the device asserts SYSRST. This Reset state does not re-initialize the clock. The clock source that is in effect prior to the RESET instruction remains in effect. SYSRST is released at the next instruction cycle and the Reset vector fetch occurs without additional delay.

40.6 WATCHDOG TIMER RESET (WDTR)

Whenever a Watchdog Timer time-out occurs, the device asynchronously asserts SYSRST. The clock source remains unchanged. Note that a WDT time-out during Sleep or Idle mode will wake-up the processor, but NOT reset the processor. For more information, refer to **Section 9. "Watchdog Timer (WDT)"**.

40.7 BROWN-OUT RESET (BOR)

PIC24F devices implement a BOR circuit, which provides the users with several configuration and power-saving options. The BOR is configurable by the device Configuration bits, BORV<1:0> (FPOR<6:5>) and BOREN<1:0> (FPOR<1:0>). There is a total of four BOR configurations which are provided in Table 40-2.

Table 40-2: BOR Configurations

BOR Configuration BOREN<1:0>		Status of SBOREN (RCON<13>)	Brown-out Reset (BOR) Operation
0	0	Unavailable	Brown-out Reset disabled in hardware; SBOREN bit disabled.
0	1	Available	Brown-out Reset controlled with the SBOREN bit setting.
1	0	Unavailable	Brown-out Reset enabled only while device is active and disabled in Sleep; SBOREN bit disabled.
1	1	Unavailable	Brown-out Reset enabled in hardware; SBOREN bit disabled.

The BOR threshold is set by the BORV<1:0> bits. If BOR is enabled (any values of BOREN<1:0>, except '00'), any drop of V_{DD} below the set threshold point will reset the device. The chip will remain in Brown-out Reset until V_{DD} rises above the threshold.

If PWRT is enabled, it will be invoked after the V_{DD} rises above the threshold. It then will keep the chip in Reset for an additional time delay, T_{PWRT}, if the V_{DD} drops below the threshold while the PWRT is running. The chip goes back into a Brown-out Reset and the Power-up Timer will be initialized. Once the V_{DD} rises above the threshold, the PWRT will execute the additional time delay.

BOR and the PWRT are independently configured. Enabling the BOR Reset does not automatically enable the Power-up Timer (PWRT).

When BOREN<1:0> = 01, the BOR can be enabled or disabled by the user in the software. This is done with the control bit, SBOREN (RCON<13>). Setting SBOREN enables the BOR to function as previously described. Clearing the SBOREN disables the BOR entirely. The SBOREN bit operates only in this mode; otherwise it is read as '0'.

Placing the BOR under software control gives the user the additional flexibility of tailoring the application to its environment without having to reprogram the device to change BOR configuration. It also allows the user to tailor the incremental current that the BOR consumes. While the BOR current is typically very small, it may have some impact in low-power applications.

Note:	Even when the BOR is under software control, the BOR Reset voltage level is still set by the BORV<1:0> Configuration bits (see Table 40-3); it cannot be changed in software.

40.7.1 Detecting BOR

When the BOR is enabled, the BOR bit (RCON<1>) is always reset to '1' on any Brown-out Reset or Power-on Reset event. This makes it difficult to determine if a Brown-out Reset event has occurred just by reading the state of BOR alone. A more reliable method is to check the state of both POR and BOR. This assumes that the POR and BOR bits are reset to '0' in the software immediately after any Power-on Reset event. If the BOR bit is '1' while POR is '0', it can be reliably assumed that a Brown-out Reset event has occurred.

Note:	Even when the device exits from the Deep Sleep mode, both the POR and the BOR bits are set.

40.7.2 Disabling BOR in Sleep Mode

When BOREN<1:0> = 10, the BOR remains under hardware control and operates as previously described. However, whenever the device enters Sleep mode, the BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

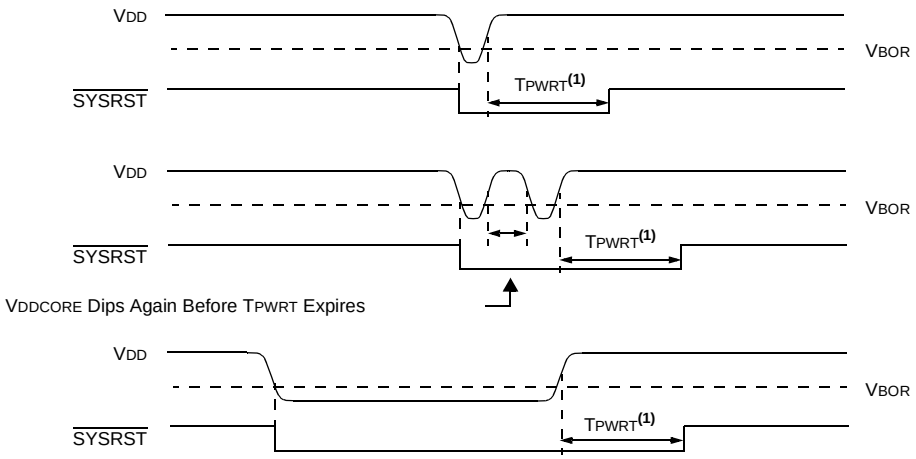
This mode allows for applications to recover from brown-out situations, while actively executing code, when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

40.7.3 Low-Power BOR (LPBOR)

Unlike the BOR module, the LPBOR operates on a single trip point. This module is intended to provide BOR/POR protection while the device is in Deep Sleep mode, though it can also be used outside of Deep Sleep mode if desired. Because it is designed for very low-current consumption, accuracy may vary.

- LPBOR re-arms the POR to ensure that the device will reset if VDD drops below the POR threshold. The LPBOR trip point is around 2.0V.
- LPBOR is selected in the configuration through the FPOR Configuration register (BORV<1:0>) = 00.

Figure 40-4: Brown-out Situations



Note 1: TPWRT will be inserted after BOR event if it is enabled.

40.8 TRAP CONFLICT RESET (TRAPR)

A Trap Conflict Reset (TRAPR) occurs when a hard and a soft trap occur at the same time. The TRAPR status bit (RCON<15>) is set on this event. Refer to **Section 8. "Interrupts"** for more information on traps.

40.9 ILLEGAL OPCODE RESET (IOPUWR)

A device Reset is generated if the device attempts to execute an illegal opcode value that was fetched from program memory. If a device Reset occurs as a result of an illegal opcode value, the IOPUWR status bit (RCON<14>) is set.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

40.10 UNINITIALIZED W REGISTER RESET

The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to. An attempt to use an uninitialized register as an Address Pointer causes a device Reset and sets the IOPUWR status bit (RCON<14>).

40.11 REGISTERS AND STATUS BIT VALUES

Status bits from the RCON register are set or cleared differently in different Reset situations, as indicated in Table 40-3.

Table 40-3: Status Bits, Their Significance and the Initialization Condition for RCON Register

Condition	Program Counter	TRAPR	IOPUWR	DPSLP	EXTR	SWR	WDTO	SLEEP	IDLE	BOR	POR	STKEPR
Power-on Reset	000000h	0	0	0	0	0	0	0	0	1	1	0
RESET Instruction	000000h	0	0	0	0	1	0	0	0	0	0	0
Brown-out Reset	000000h	0	0	0	0	0	0	0	0	1	0	0
$\overline{\text{MCLR}}$ during Run Mode	000000h	0	0	0	1	0	0	0	0	0	0	0
$\overline{\text{MCLR}}$ during Idle Mode	000000h	0	0	0	1	0	0	0	1	0	0	0
$\overline{\text{MCLR}}$ during Sleep Mode	000000h	0	0	0	1	0	0	1	0	0	0	0
$\overline{\text{MCLR}}$ during Deep Sleep Mode	000000h	0	0	1	1	0	0	0	0	0	0	0
WDT Time-out Reset during Run Mode	000000h	0	0	0	0	0	1	0	0	0	0	0
WDT Time-out Reset during Idle Mode	PC + 2	0	0	0	0	0	1	0	1	0	0	0
WDT Time-out Wake-up during Sleep Mode	PC + 2	0	0	0	0	0	1	1	0	0	0	0
Stack Overflow Reset	000000h	0	0	0	0	0	0	0	0	0	0	1
Stack Underflow Reset	000000h	0	0	0	0	0	0	0	0	0	0	1
Trap Event Reset	000000h	1	0	0	0	0	0	0	0	0	0	0
Illegal Opcode/ Uninitialized WREG	000000h	0	1	0	0	0	0	0	0	0	0	0
Interrupt Exit from Idle Mode	PC + 2(1)	0	0	0	0	0	0	0	1	0	0	0
Interrupt Exit from Sleep Mode	PC + 2(1)	0	0	0	0	0	0	1	0	0	0	0
Idle Mode (execute PWRSAV 1)	PC + 2	0	0	0	0	0	0	0	1	0	0	0
Sleep Mode (execute PWRSAV 0)	PC + 2	0	0	0	0	0	0	1	0	0	0	0
Deep Sleep Mode (set DSEN and execute PWRSAV 0)	000000h	0	0	1	0	0	0	0	0	1	1	0

Note 1: Program Counter (PC) is loaded with PC + 2 if the interrupt priority is less than, or equal to, the CPU interrupt priority level. PC is loaded with the hardware vector address if the interrupt priority is greater than the CPU interrupt priority level.

40.11.1 Using the RCON Status Bits

The user can read the RCON register after any device Reset to determine the cause of the Reset. Table 40-4 provides a summary of the Reset flag bit operation.

Note:	The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 40-4: Reset Flag Bit Operation

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap conflict event	POR
IOPWR (RCON<14>)	Illegal opcode or uninitialized W register access	POR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET instruction	POR
WDTO (RCON<4>)	WDT time-out	PWRSAV instruction, POR
IDLE (RCON<2>)	PWRSAV #IDLE instruction	POR, CLRWDT instruction
SLEEP (RCON<3>)	PWRSAV #SLEEP instruction	POR, CLRWDT instruction
DPSLP (RCON<10>)	Set DSEN and execute PWRSAV #SLEEP instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

40.12 DEVICE RESET TO CODE EXECUTION START TIME

The delay between the end of a Reset event and when the device actually begins to execute code is determined by two main factors: the type of Reset and the system clock source coming out of the Reset. The code execution start time for various types of device Resets is summarized in Table 40-5. Individual delays are characterized in **Section 40.14 "Electrical Specifications"**.

Table 40-5: Code Execution Start Time for Various Device Resets

Reset Type	Clock Source	$\overline{\text{SYSRST}}$ Delay	System Clock Delay	Notes
POR(6)	EC	TPOR + TPWRT	—	**1, 2**
	FRC, FRCDIV	TPOR + TPWRT	TFRC	**1, 2, 3**
	LPRC	TPOR + TPWRT	TLPRC	**1, 2, 3**
	ECPLL	TPOR + TPWRT	TLOCK	**1, 2, 4**
	FRCPLL	TPOR + TPWRT	TFRC + TLOCK	**1, 2, 3, 4**
	XT, HS, SOSC	TPOR+ TPWRT	TOST	**1, 2, 5**
	XTPLL, HSPLL	TPOR + TPWRT	TOST + TLOCK	**1, 2, 4, 5**
BOR	EC	TPWRT	—	**2**
	FRC, FRCDIV	TPWRT	TFRC	**2, 3**
	LPRC	TPWRT	TLPRC	**2, 3**
	ECPLL	TPWRT	TLOCK	**2, 4**
	FRCPLL	TPWRT	TFRC + TLOCK	**2, 3, 4**
	XT, HS, SOSC	TPWRT	TOST	**2, 5**
	XTPLL, HSPLL	TPWRT	TFRC + TLOCK	**2, 3, 4**
All others	Any Clock	—	—	**None**

Note 1: TPOR = Power-on Reset delay.

2: TPWRT = 64 ms nominal if POR<PWRTEN> is enabled; otherwise, no TPWRT.

3: TFRC and TLPRC = RC oscillator start-up times.

4: TLOCK = PLL lock time.

5: TOST = Oscillator Start-up Timer (OST). A 10-bit counter waits 1024 oscillator periods before releasing oscillator clock to the system.

6: If Two-Speed Start-up is enabled, regardless of the primary oscillator selected, the device starts with FRC, and in such cases, FRC start-up time is valid.

Note:	Nominal timing values are indicated in **Section 40.14 "Electrical Specifications"**. Refer to the "**Electrical Characteristics**" section of the product data sheet for detailed operating frequency and timing specification values.

For POR, the system Reset signal, $\overline{\text{SYSRST}}$, is released after the POR delay time (TPOR) and the TPWRT delay time expires. For BOR, $\overline{\text{SYSRST}}$ is released after the TPWRT delay time expires if the Power-up Timer is enabled in the Configuration Word. For all other Resets, the system Reset signal, $\overline{\text{SYSRST}}$, is released without additional delay after the Reset condition is removed.

The time that the device actually begins to execute code also depends on the system oscillator delays, which include the Oscillator Start-up Timer delay (TOST), Fast Internal Oscillator delay (TFRC), Low-Power Internal Oscillator delay (TLPRC) and the PLL Lock time (TLOCK). The OST and PLL lock times run parallel to the applicable code execution delay times.

40.12.1 POR and Long Oscillator Start-up Times

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has NOT expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

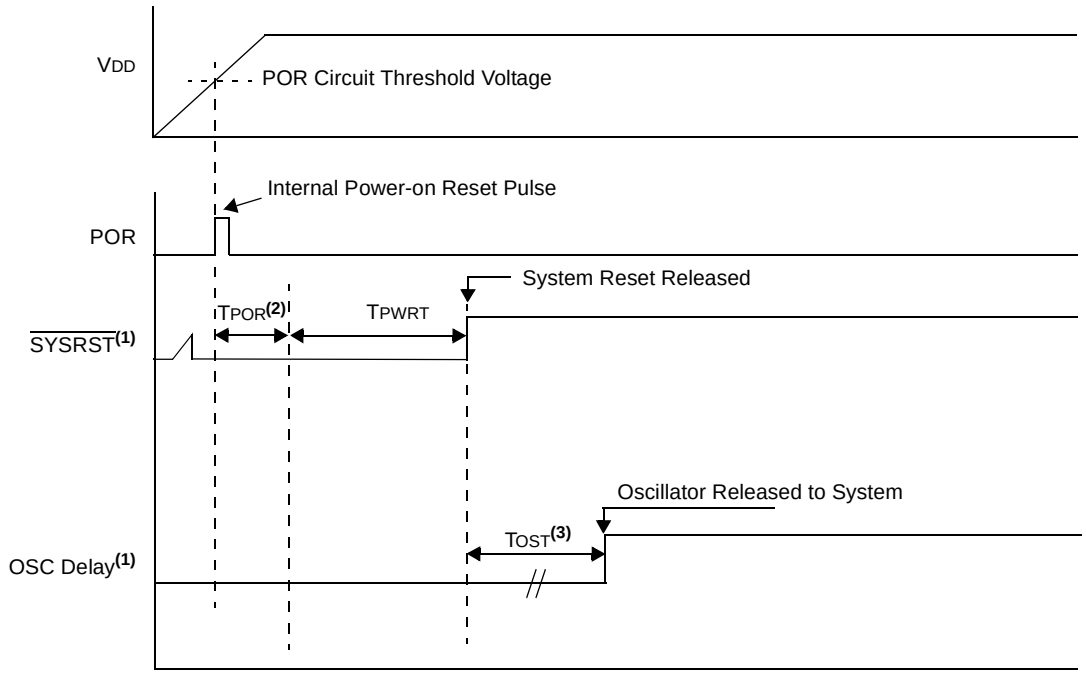
The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

40.12.2 Examples of Device Start-up Timelines

Figure 40-5 through Figure 40-8 depict graphical timelines of the delays associated with device Reset for several operating scenarios. The individual delays are characterized in **Section 40.14 "Electrical Specifications"**.

Figure 40-5 displays the delay timeline when a crystal oscillator is used as the system clock. The internal POR pulse occurs at the VPOR threshold. TPOR and TPWRT delays occur after the internal POR pulse.

Figure 40-5: Device Reset Delay, Crystal (XT/HS/SOSC) Clock Source



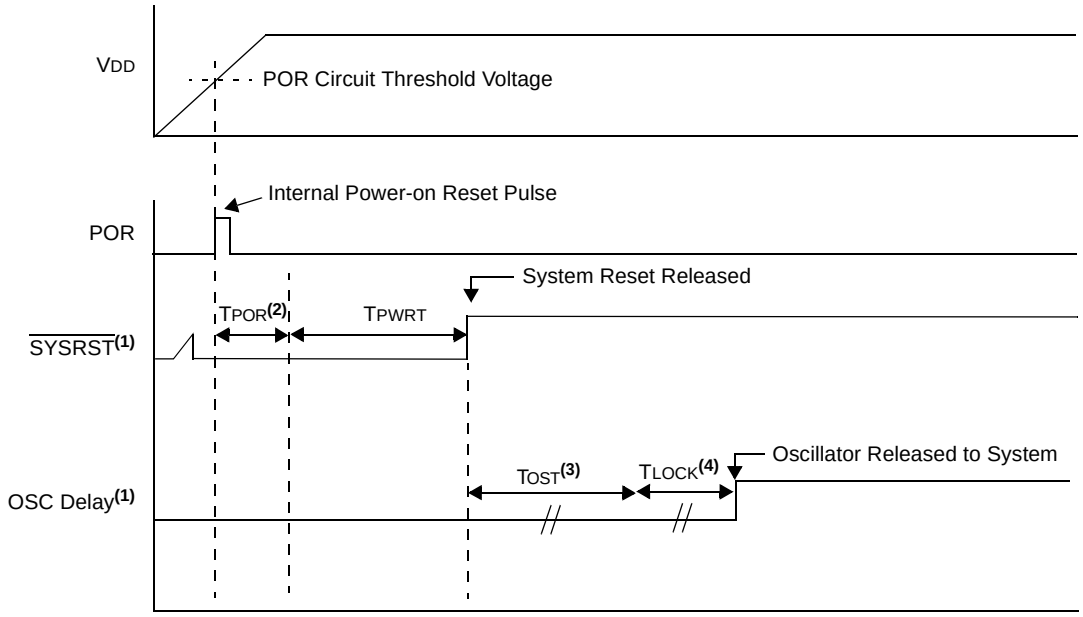
Note 1: Delay times shown are not drawn to scale.

2: TPOR = Power-on Reset delay.

3: TOST = Oscillator Start-up Timer (OST). A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system. Refer to product data sheet for TLPRC and TFRC specifications.

The Reset timeline displayed in Figure 40-6 is similar to that displayed in Figure 40-5, except that the PLL has been enabled, which increases the oscillator stabilization time.

Figure 40-6: Device Reset Delay, Crystal (XT/HS/SOSC) + PLL Clock Source



Note 1: Delay times shown are not drawn to scale.

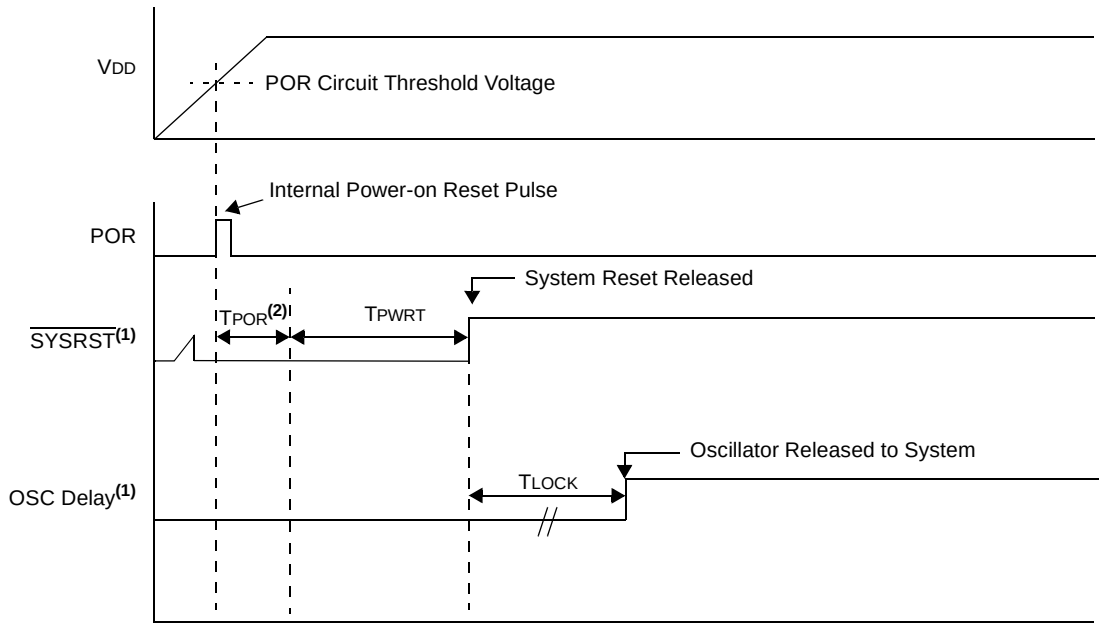
2: TPOR = Power-on Reset delay.

3: TOST = Oscillator Start-up Timer (OST). A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system. Refer to product data sheet for TLPRC and TFRC specifications.

4: TLOCK not inserted when PLL is disabled.

The Reset timeline in Figure 40-7 displays an example of when the ECPLL clock source is used as the system clock. This example is similar to the one provided in Figure 40-6, except that the Oscillator Start-up Timer delay, TOST, does not occur.

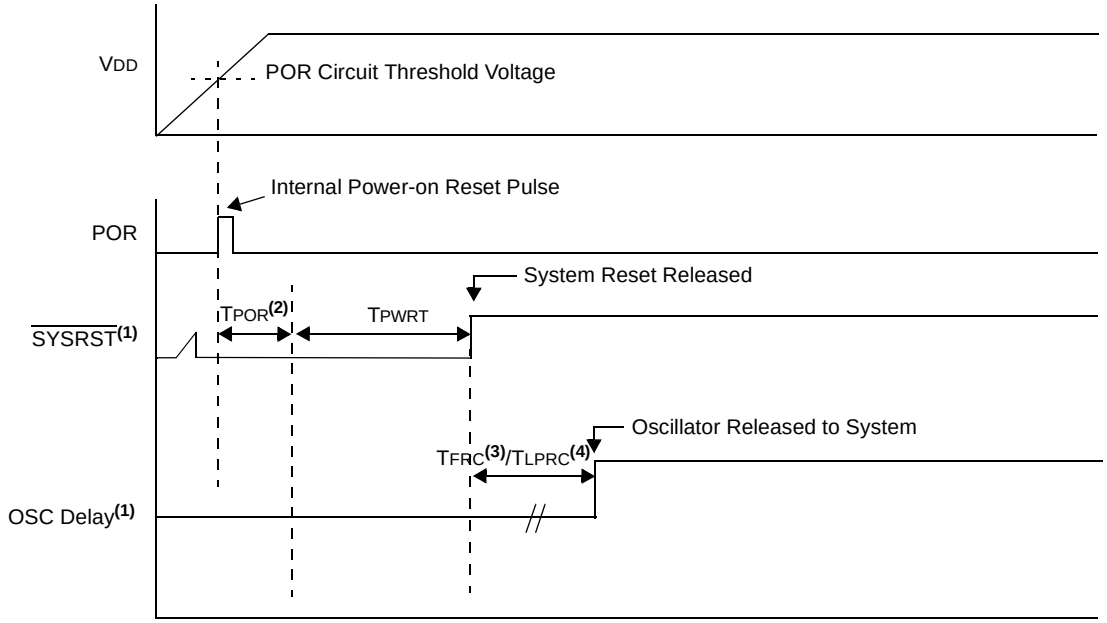
Figure 40-7: Device Reset Delay, EC or ECPLL Clock



Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.

The Reset timeline displayed in Figure 40-8 provides an example of using the internal FRC or LPRC clock sources, or if Two-Speed Start-up is enabled.

Figure 40-8: Device Reset Delay, FRC or LPRC Clock or with Two-Speed Start-up Enabled



Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.
3: TFRC = FRC oscillator start-up time. Refer to device data sheets for values.
4: TLPRC = LPRC oscillator start-up time. Refer to device data sheets for values.

40.13 SPECIAL FUNCTION REGISTER (SFR) RESET STATES

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function, and their Reset values are specified in the corresponding section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of two registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the oscillator Configuration bits in the FOSC Configuration register (see Table 40-1).

40.14 ELECTRICAL SPECIFICATIONS

Figure 40-9: Brown-out Reset Characteristics

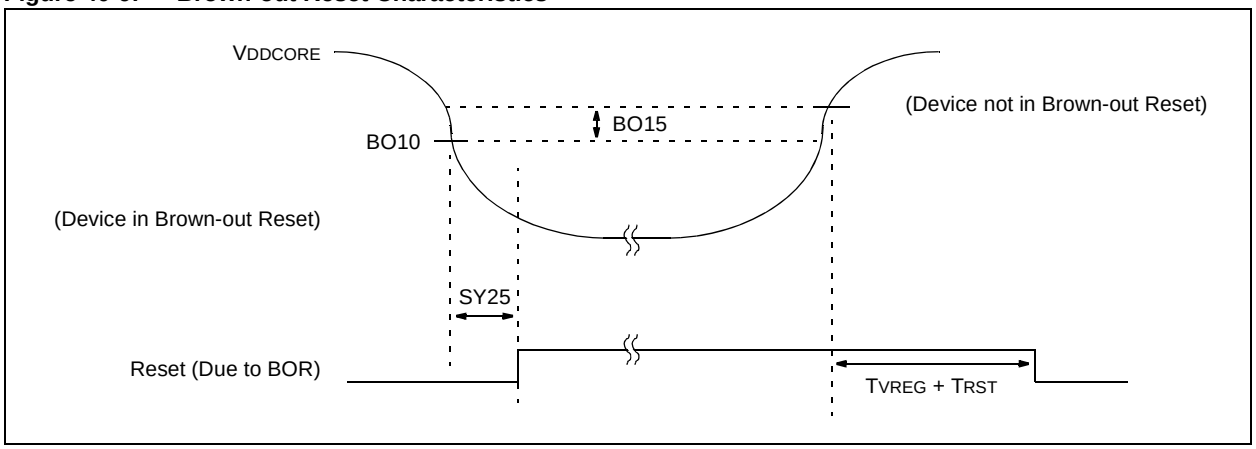


Figure 40-10: Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing Characteristics

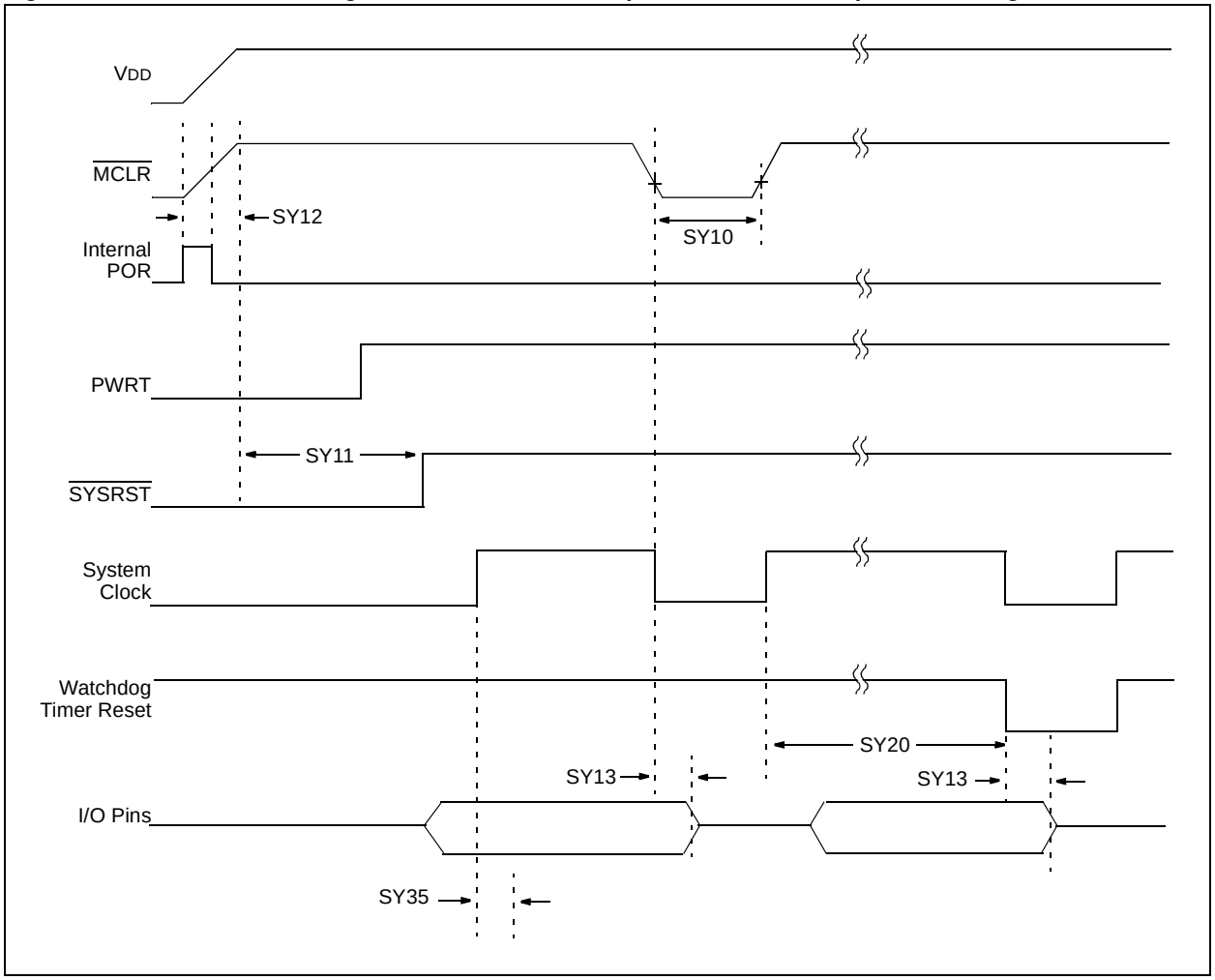


Table 40-6: Electrical Characteristics: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
BO10	VBOR	BOR Voltage on VDD Transition, High-to-Low, BORV<1:0> = 00	—	2	—	V	VDD = 3.3V
		BORV<1:0> = 01	—	3	—	V	
		BORV<1:0> = 10	—	2.7	—	V	
		BORV<1:0> = 11	—	1.8	—	V	
BO15	VBHYS	BOR Hysteresis	—	5	—	mV	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

Table 40-7: Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer and Brown-out Reset Timing Requirements

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SY10	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	µs	
SY11	TPWRT	Power-up Timer Period	—	64	—	ms	
SY12	TPOR	Power-on Reset Delay	1	5	10	µs	
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	100	ns	
SY20	TWDT	Watchdog Timer Time-out Period	0.85	1.0	1.15	ms	1:32 prescaler
			3.4	4.0	4.6	ms	1:128 prescaler
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	µs	VDD ≤ VBOR

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

40.15 DESIGN TIPS

Question 1: ***How do I use the RCON register?***

Answer: The initialization code after a Reset should examine RCON and confirm the source of the Reset. In some applications, this information can be used to take appropriate action to correct the problem that caused the Reset to occur. All Reset status bits in the RCON register should be cleared after reading them to ensure the RCON value provides meaningful results after the next device Reset.

Question 2: ***I initialized a W register with a 16-bit address; why does the device appear to reset when I attempt to use the register as an address?***

Answer: Because all data addresses are 16-bit values, the uninitialized W register logic only recognizes that a register has been initialized correctly if it was subjected to a word load. Two-byte moves to a W register, even if successive, will not work, resulting in a device Reset if the W register is used as an Address Pointer in an operation.

40.16 REGISTER MAPS

A summary of the registers associated with the PIC24F Oscillator module is provided in Table 40-8.

Table 40-8: Reset Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	TRAPR	IOPUWR	SBOREN	—	—	DPSLP	—	PMSLP	EXTR	SWR	SWDTEN(1)	WDTO	SLEEP	IDLE	BOR	POR	0003

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for the fully implemented registers.
Note 1: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

40.17 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Reset with Programmable Brown-out Reset are:

Title	Application Note #
Power-up Trouble Shooting	AN607
Power-up Considerations	AN522

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

40.18 REVISION HISTORY

Revision A (January 2009)

This is the initial released revision of this document.

NOTES: