Section 36. High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)

HIGHLIGHTS

This section of the manual contains the following topics:

36.1 INTRODUCTION

At their highest level of functionality, PIC24F devices integrate several features that affect the entire device as a whole. They add convenience and flexibility of design for the user, and allow the devices to be incorporated into a wider range of designs. These include:

- Flexible Configuration Options – Allowing users to select a wide range of basic microcontroller operating options, and changing them if needed during run time.
- Device Identification – Allowing electronic confirmation of a device part number and revision level in the target application.
- On-Chip Voltage Monitoring – Allowing the device to be used over a range of application voltage levels and having safe shutdown before the non-operable voltage is reached.

36.2 DEVICE CONFIGURATION

The basic behavior and operation of PIC24F family devices are set by the device Configuration bits. These allow the user to select a wide range of options and optimize the microcontroller's operation to the application's requirements.

In PIC24F family devices, device Configuration bits are mapped to the device's program memory space starting at location F80000h. This is beyond the user program memory space and belongs to the configuration memory space (800000h-FFFFFFh).

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various configuration options. To prevent inadvertent configuration changes during code execution, all programmable device Configuration bits are write-once.

Table 36-1 provides a list of the available Configuration bit options.

Note:	All the bits that are described here are not available on all devices. Also, additional bits may be available.

For more information on the location of device Configuration Words and Configuration bit mapping of a particular device, refer to the specific device data sheet.

36.2.1 Configuration Words

Table 36-1: PIC24F Device Configuration Bits(1)

Configuration Bit	Function
BOREN	Enables Brown-out Reset.
BORV	Selects the Brown-out Reset voltage.
BSS0	Code-protects the boot segment.
BWRP	Enables write protection for boot segment.
BSZ	Selects the boot segment size.
$\overline{\text{DEBUG}}$	Enables background debugger operation with external device control.
DSWDTEN	Enables the Deep Sleep Watchdog Timer.
DSWCKSEL	Selects the Deep Sleep Watchdog Timer clock source.
DSWDTPS	Selects the Deep Sleep Watchdog Timer postscaler.
DSZPBOR	Enables Deep Sleep zero-power BOR.
FCKSM	Configures device clock switching and Fail-Safe Clock Monitor (2 bits, 3 configuration options).
FICD	Selects the ICD pins.
FNOSC	Selects initial (default) device oscillator (3 bits, up to 8 configuration options).
FWDTEN	Enables Watchdog Timer.
FWPSA	Selects WDT prescaler.
GSS0	Enables code protection for the program memory space.
GWRP	Enables write/erase protection for program memory.
I2CxSEL	Selects standard or alternate I/O pin mapping of SCLx and SDAx.
ICS	Selects the ICSP™ port used with ICD (2 bits, up to 4 options).
MCLRE	Disables $\overline{\text{MCLR}}$ pin and makes it an I/P only pin.
IESO	Enables Two-Speed Start-up.
OSCIOFCN	Selects function of OSC2 pin (I/O port or CLKO) in certain external oscillator modes.
POSCFREQ	Selects primary oscillator frequency range.
POSCMD	Selects primary (external) oscillator configuration (2 bits, 4 configurations).
PWRTEN	Enables Power-up Timer.
RTCCKSEL	Selects the RTCC clock source.
SOSCSEL	Selects secondary oscillator, either low or moderate power.
WDTPS	Selects WDT postscaler (4 bits, up to 16 configuration options).
WINDIS	Selects Windowed Operation mode for Watchdog Timer.

Note 1: Refer to the specific product data sheet for device configuration bit details.

36.3 DEVICE IDENTIFICATION

PIC24F family devices have two read-only registers that provide device-specific identification information. These are located near the end of the device configuration space, starting at FF0000h. The Device ID registers are 24 bits wide and the upper 8 bits are unimplemented. Both registers can be read using table read instructions.

The DEVID register at FF0000h identifies the Microchip microcontroller architectural family and the specific part number. The DEVREV register at FF0002h identifies the particular silicon revision for that device. Refer to the product data sheet for details on the device ID format.

For any given family of PIC24F family devices, the corresponding device data sheet provides a list of values for DEVID and the corresponding part numbers for that family. The association of the value of DEVREV to a silicon revision level is different for each part number. The translation of a DEVREV value to a revision level can be found in part-specific literature, such as device silicon errata, or through Microchip's development tools, such as MPLAB® IDE. For assistance with interpreting values of DEVREV, contact Microchip technical support or your local Microchip representative.

36.4 SUPPLY VOLTAGE (V_{DD}) MONITORING FEATURES

36.4.1 Power-on Reset (POR)

On powering the device, the device enters the Power-on Reset state. On coming out of the POR state, the device takes a $T_{STARTUP}$ time delay to start operations.

If the Power-up Timer (PWRT) is enabled, the PWRT adds a fixed delay of 64 ms nominal delay after the $T_{STARTUP}$ delay. The Power-up Timer can be enabled or disabled by setting or clearing the FPOR<PWRTEN> bit.

36.4.2 Brown-out Reset (BOR)

The PIC24F family devices have configurable brown-out circuitry. The circuitry can be configured to generate the device Reset when V_{DD} falls below the set trip point. There are three selectable trip points that can be selected by the FPOR<BORV1:BORV0> bits. The circuitry is enabled by default; it can be disabled by clearing the Configuration bits, FPOR<BOREN1:BOREN0>. If the BOR circuitry is disabled by clearing FPOR<BOREN1:BOREN0>, it can be enabled or disabled by software by setting or clearing the bit, RCON<SBOREN>.

When the BOR circuitry is enabled and the voltage falls below the set voltage, the Reset circuitry will generate a BOR. This event is captured by the BOR flag bit (RCON<1>).

For the available BOR trip points, refer to the particular device data sheet.

36.4.3 High/Low-Voltage Detection (HLVD)

The PIC24F family devices have a programmable High/Low-Voltage Detection circuit (HLVD). The circuitry can be programmed to generate an interrupt on crossing the range of the VDD level in the selected direction.

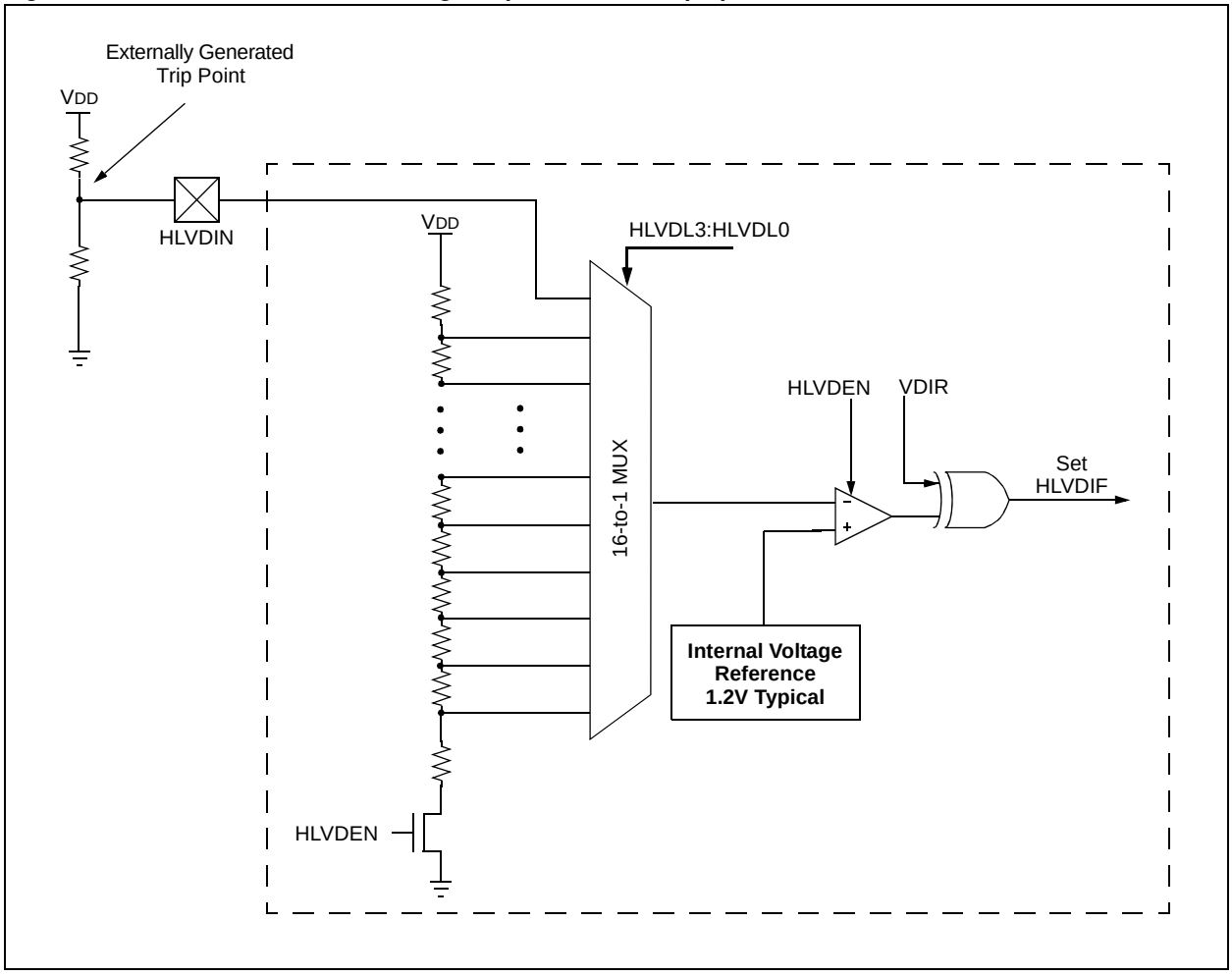
36.4.3.1 OPERATION

When the HLVD module is enabled, a comparator uses an internally generated reference voltage as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The “trip point” voltage is the voltage level at which the device detects a high or low-voltage event, depending on the configuration of the module. When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the HLVDIF bit.

The trip point voltage is software programmable to any one of 16 values. The trip point is selected by programming the HLVDCON <HLVDL3:HLVDL0> bits.

The HLVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits, HLVDL3:HLVDL0, are set to ‘1111’. In this state, the comparator input is multiplexed from the external input pin, HLVDIN. This gives users flexibility because it allows them to configure the HLVD interrupt to occur at any voltage in the valid operating range.

Figure 36-1: HLVD Module Block Diagram (with External Input)



36.4.3.2 CONFIGURING THE HLVD MODULE

There are 15 selectable trip ranges that can be selected by configuring HLVDCON<HLVDL3:HLVDL0>. The circuitry can be enabled/disabled by the bit, HLVDCON<HLVDEN>. When the HLVD module is enabled and VDD crosses the selected trip voltage range in the selected direction, an interrupt will be generated and the HLVD flag will be set (IFS4<HLVDIF>).

If the trip ranges provided are not suitable for the application, one can configure HLVDCON<HLVDL3:HLVDL0> to 0b1111 to use an external reference voltage. If the external reference voltage crosses 1.2V nominal on the HLVDIN pin, an interrupt will be generated. The VDIR (HLVDCON<7>) can be used to select either a falling or rising VDD trigger.

Register 36-1: HLVDCON: High/Low-Voltage Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
HLVDEN	—	HLSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIR	BGVST	IRVST	—	HLVDL3(1)	HLVDL2(1)	HLVDL1(1)	HLVDL0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **HLVDEN:** HLVD Power Enable bit
1 = HLVD enabled
0 = HLVD disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **HLSIDL:** HLVD Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **VDIR:** Voltage Change Direction Select bit
1 = Event occurs when voltage equals or exceeds trip point (HLVDL3:HLVDL0)
0 = Event occurs when voltage equals or falls below trip point (HLVDL3:HLVDL0)

bit 6 **BGVST:** Band Gap Voltage Stable Flag bit
1 = Indicates that the band gap voltage is stable
0 = Indicates that the band gap voltage is unstable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
1 = Indicates that the internal reference voltage is stable and the voltage detect logic generates the interrupt flag at the specified voltage range
0 = Indicates that the internal reference voltage is unstable and the voltage detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **HLVDL3:HLVDL0:** Voltage Detection Limit bits(1)
1111 = External analog input is used (input comes from the HLVDIN pin)
1110 = Maximum range
.
.
0000 = Minimum range

Note 1: For the available trip points, refer to the device data sheet.

36.4.3.3 HLVD SETUP

The following steps are needed to set up the HLVD module:

1. Write the value to the HLVDL3:HLVDL0 bits that selects the desired HLVD trip point.
2. Set the VDIR bit to detect high voltage (VDIR = 1) or low voltage (VDIR = 0).
3. Enable the HLVD module by setting the HLVDEN bit.
4. Clear the HLVD Interrupt Flag (HLVDIF), which may have been set from a previous interrupt.
5. Enable the HLVD interrupt if interrupts are desired by setting the HLVDIE bit. An interrupt will not be generated until the IRVST bit is set.

36.4.3.4 CURRENT CONSUMPTION

When the module is enabled, the HLVD comparator and voltage divider (if HLVD is not set to 0b1111) are enabled and will consume static current. The total current consumption, when enabled, is specified in the electrical specifications section of the specific device data sheet.

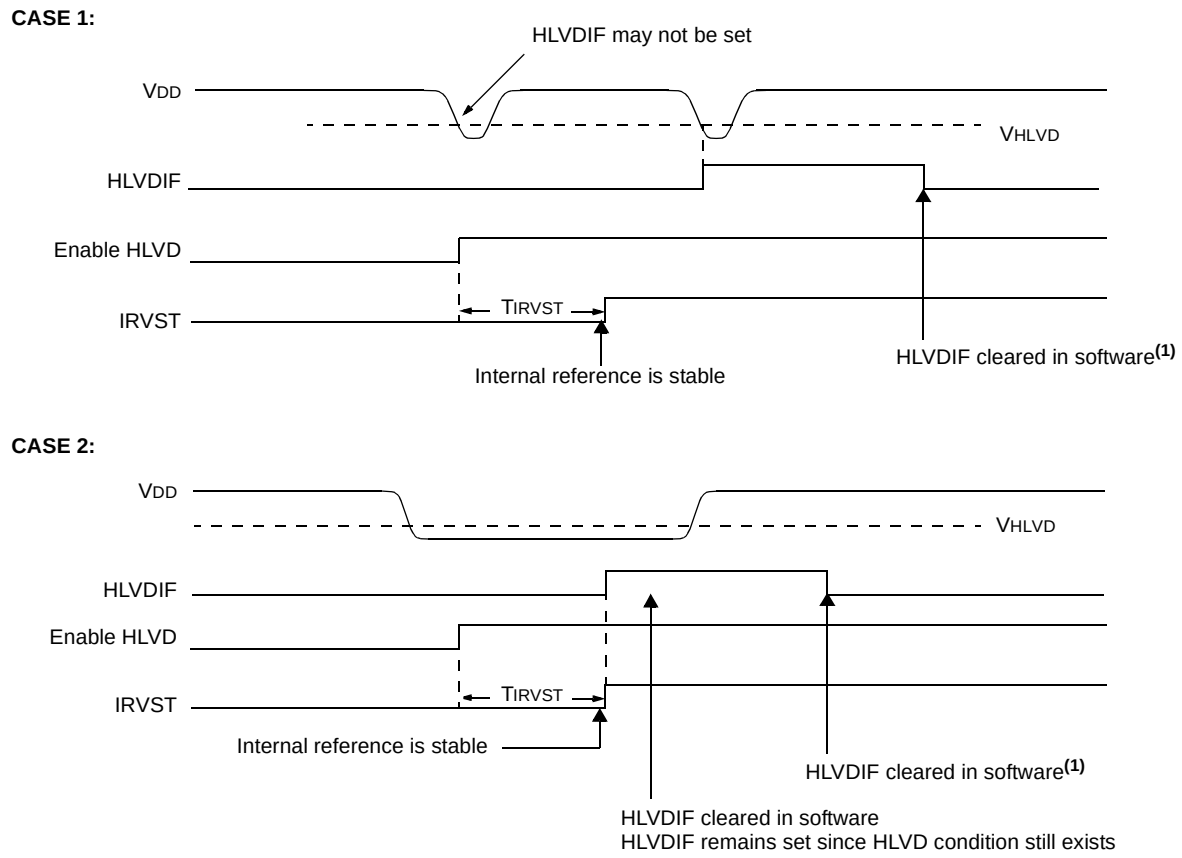
Depending on the application, the HLVD module does not need to be operating constantly. To decrease the current requirements, the HLVD circuitry can be enabled for short periods by software where the voltage is checked. This will significantly reduce current consumption.

36.4.3.5 HLVD START-UP TIME

If the HLVD is disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TIRVST, is specified in the electrical specifications section of the specific device data sheet. The IRVST (HLVDCON<5>) will set to indicate the reference voltage is stable and the HLVD module is ready.

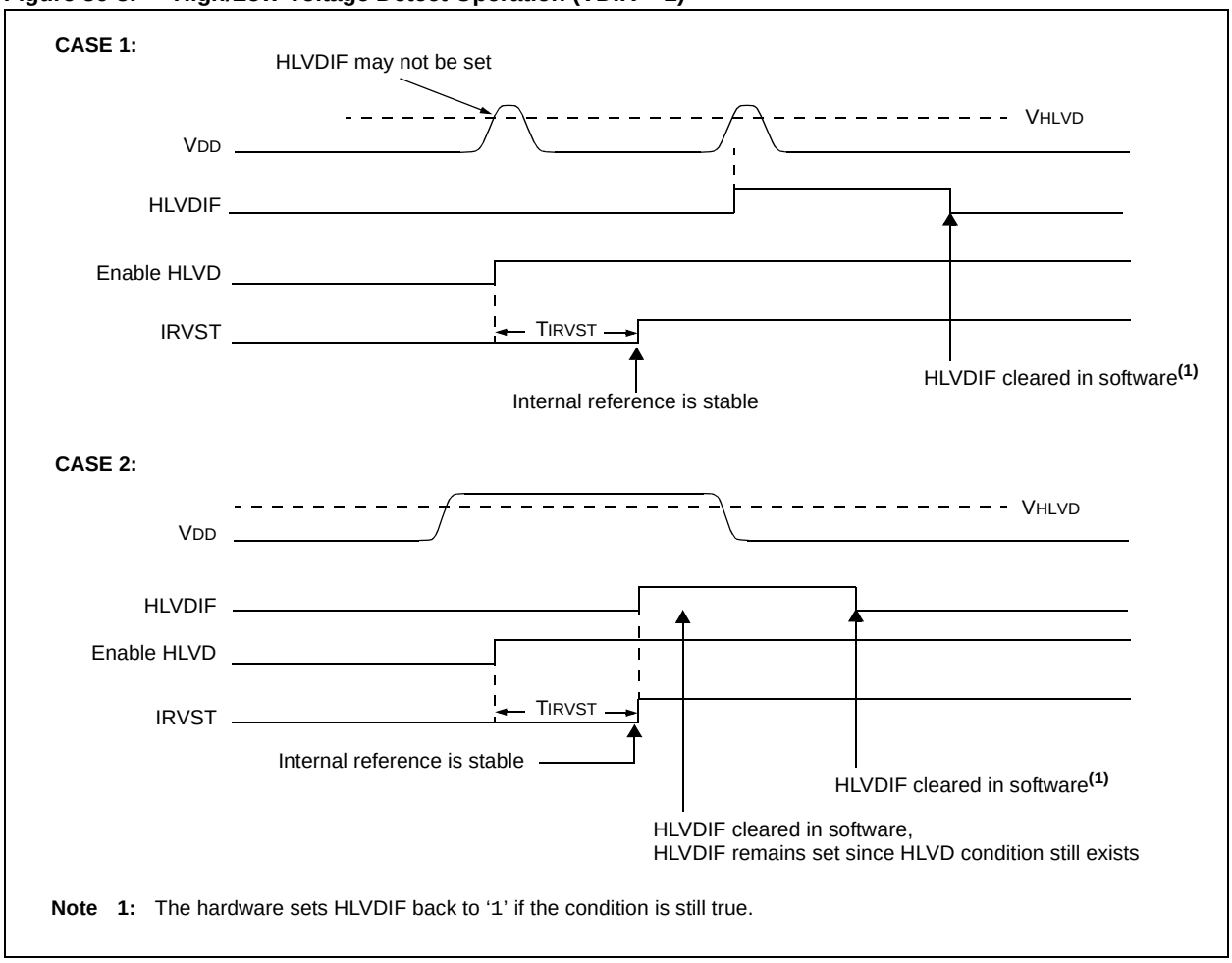
The HLVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval. Refer to Figure 36-2 or Figure 36-3.

Figure 36-2: High/Low-Voltage Detect Operation (VDIR = 0)



Note 1: The hardware sets HLVDIF back to '1' if the condition is still true.

Figure 36-3: High/Low-Voltage Detect Operation (VDIR = 1)



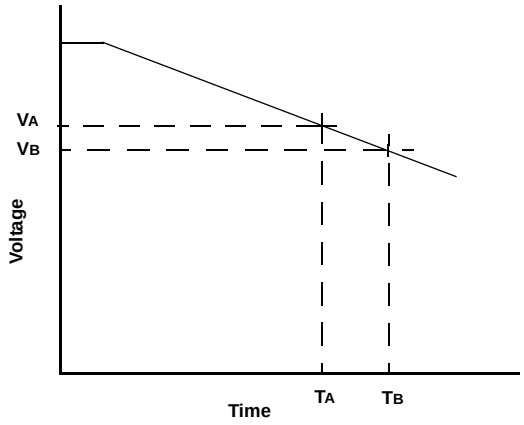
Note 1: The hardware sets HLVDIF back to '1' if the condition is still true.

36.4.3.6 APPLICATIONS

In many applications, the ability to detect a drop below or rise above a particular threshold is desirable. For example, the HLVD module could be periodically enabled to detect Universal Serial Bus (USB) attach or detach. This assumes the device is powered by a lower voltage source than the USB when detached. An attach would indicate a high-voltage detect from, for example, 3.3V to 5V (the voltage on USB) and vice versa for a detach. This feature could save a design a few extra components and an attach signal (input pin).

For general battery applications, Figure 36-4 displays a possible voltage curve. Over time, the device voltage decreases. When the device voltage reaches voltage, VA, the HLVD logic generates an interrupt at time, TA. The interrupt could cause the execution of an Interrupt Service Routine (ISR), which would allow the application to perform “housekeeping tasks” and perform a controlled shutdown before the device voltage exits the valid operating range at TB. The HLVD, thus, would give the application a time window represented by the difference between TA and TB to safely exit.

Figure 36-4: Typical Low-Voltage Detect Application



Legend: VA = HLVD trip point
VB = Minimum valid device operating voltage

36.4.3.7 OPERATION DURING SLEEP

When enabled, the HLVD circuitry continues to operate during Sleep. If the device voltage crosses the trip point, the HLVDIF bit will be set and the device will wake-up from Sleep. Device execution will continue from the interrupt vector address if interrupts have been globally enabled.

36.4.3.8 EFFECTS OF A RESET

A device Reset forces all registers to their Reset state. This forces the HLVD module to be turned off.

36.5 REGISTER MAPS

A summary of the registers associated with the PIC24F High-Level Integration with Programmable High/Low-Voltage Detect (HLVD) is provided in Table 36-2.

Table 36-2: HLVDCON SFR Memory Map

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
HLVDCON	HLVDEN	—	HLSIDL	—	—	—	—	—	VDIR	BGVST	IRVST	—	HLVDL3	HLVDL2	HLVDL2	HLVDL0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexidecimal.
Note 1: Refer to the device data sheet for specific core register map details.

36.6 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the High-Level Integration with Programmable High/Low-Voltage Detect (HLVD) of PIC24F Devices are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

36.7 REVISION HISTORY

Revision A (October 2008)

This is the initial released revision of this document.

NOTES: