GENERAL INSTRUMENT | **PIC16C5x SERIES**

ADVANCE INFORMATION

EPROM-Based 8-Bit CMOS Microcontrollers

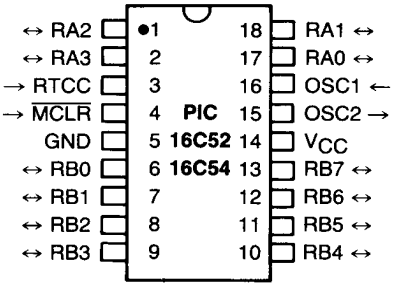
FEATURES

- Low-Cost PIC® 8-Bit Microcontroller Family
- Designed with Fully Static CMOS EPROM Technology
  - — User Programmable: Prototypes and
- Low-Volume Production
- Factory Programmable: High-Volume Production
- Ultra Wide Performance Ranges:
  - — Frequency: 25kHz – 20MHz (200ns Instruction Rate)
  - — Voltage: 2.5V – 6.0V Single Supply
  - — Current: <1μA Standby Mode
    - 35μA (125μs Instruction Rate)
    - 2.5mA (2μs Instruction Rate)
    - 30mA (200ns Instruction Rate)
- Low-Cost RC Oscillator or Crystal Oscillator
- Small 18-pin or 28-pin DIP and Surface Mount Packaging
- Powerful "Single Word" Instruction Set
- Security EPROM Fuse for Code Protection
- Free Running Watchdog Timer
- Oscillator Start-Up Timer
- 8-Bit Real-Time Clock Counter (RTCC) with Optional 8-Bit Programmable Prescaler
- 2-Level Stack for Subroutine Nesting
- Efficient EPROM Program Memory Organizations: 256 × 12 and 512 × 12 bits.
- 32 Bytes of RAM
- 8-Bit ALU
- 12 or 20 Bidirectional I/O Lines
- Available in Three Temperature Ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: −40°C to +85°C
  - — Automotive: −40°C to +110°C
- Low Cost PC-Based Software Development System

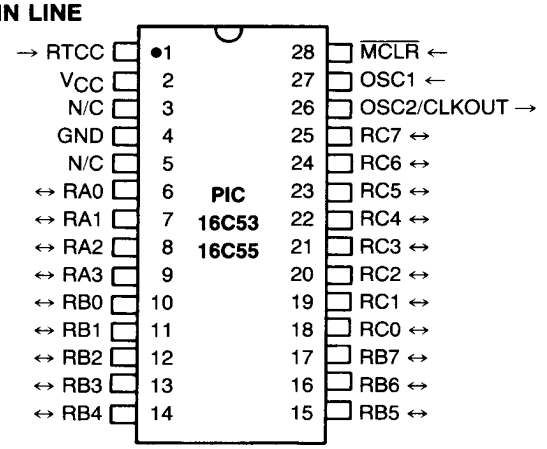
PIN CONFIGURATIONS

Top View

18 LEAD DUAL IN LINE



28 LEAD DUAL IN LINE



DESCRIPTION

The General Instrument Microelectronics PIC16C52, PIC16C53, PIC16C54 and PIC16C55 are single-chip microcontrollers designed in GIM's CMOS EPROM technology. Their architecture is based on GIM's PIC165x NMOS 8-bit microcontroller series, but is modified and upgraded to enhance overall operation and performance. The PIC16C5x series is pin compatible to the PIC1652/54/55 and uses the same instruction set plus 6 new instructions (TRIS F5, TRIS F6, TRIS F7, OPTION, SLEEP, CLRWDT).

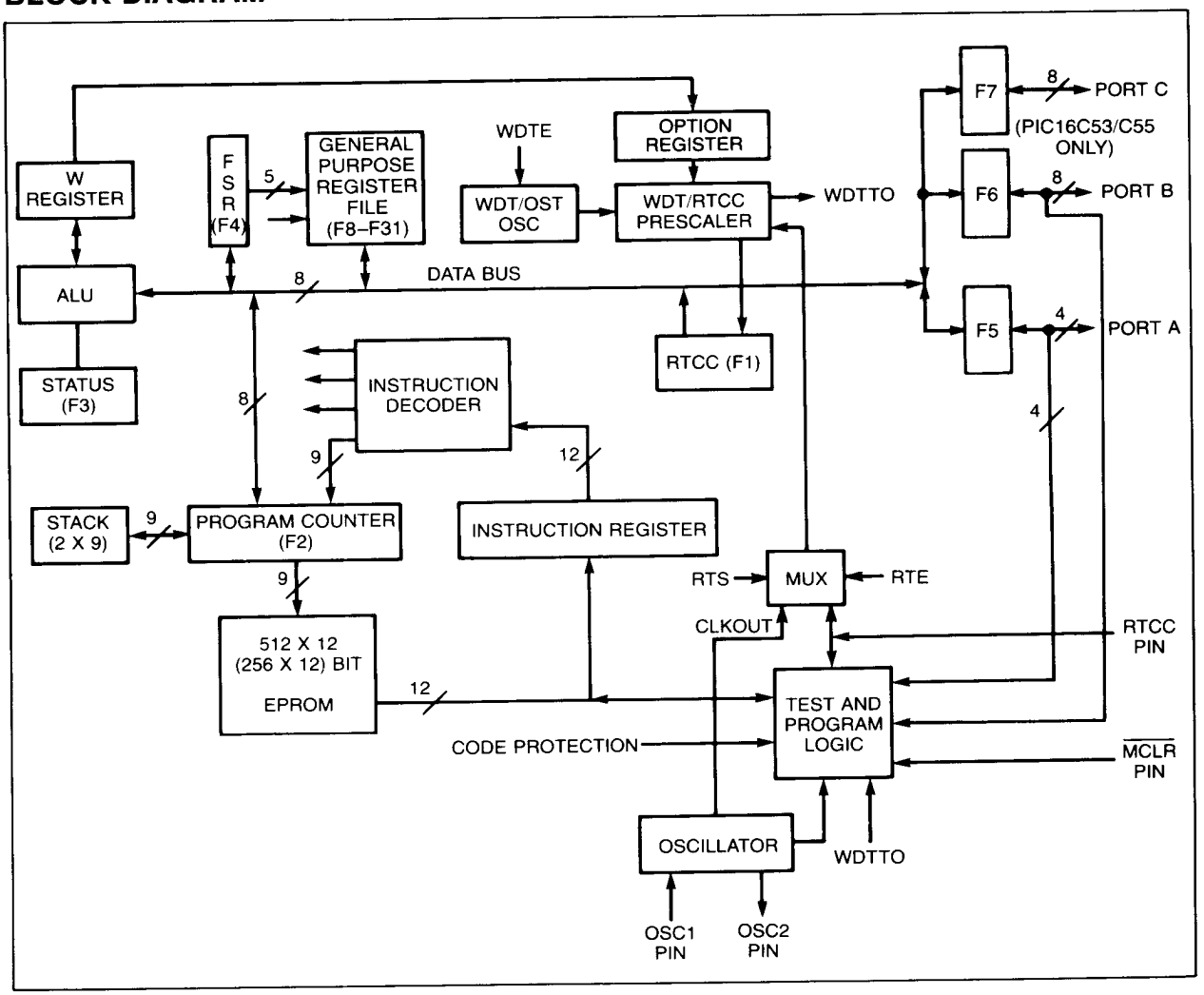
PIC is a registered trademark of General Instrument Microelectronics

User programmable CMOS EPROM technology offers a reduction in development costs and turn-around time for prototype evaluation when compared to factory mask programmable NMOS ROM versions of the PIC family.

Because of these features users can quickly and economically design a PIC16C5x microcontroller into a system in several ways — as a prototype evaluation, as a low volume production run, or as a pilot production run.

For higher volumes requiring factory programming, General Instrument Microelectronics offers quick-turn production delivery schedules.

BLOCK DIAGRAM



PIC16C5x FAMILY OVERVIEW

PART #	EPROM CONFIGURATION	I/O PINS	PIN COUNT	OSCILLATOR FREQUENCY RANGE	OSCILLATOR TYPE
PIC16C52XT	256 x 12	12	18	0.4–4 MHz	XTAL, EXT
PIC16C52RC	256 x 12	12	18	0.4–4 MHz	RC, EXT
PIC16C52LP	256 x 12	12	18	25–500 kHz	XTAL, EXT
PIC16C52HS	256 x 12	12	18	4.0–20 MHz	XTAL, EXT
PIC16C53XT	256 x 12	20	28	0.4–4 MHz	XTAL, EXT
PIC16C53RC	256 x 12	20	28	0.4–4 MHz	RC, EXT
PIC16C53LP	256 x 12	20	28	25–500 kHz	XTAL, EXT
PIC16C53HS	256 x 12	20	28	4.0–20 MHz	XTAL, EXT
PIC16C54XT	512 x 12	12	18	0.4–4 MHz	XTAL, EXT
PIC16C54RC	512 x 12	12	18	0.4–4 MHz	RC, EXT
PIC16C54LP	512 x 12	12	18	25–500 kHz	XTAL, EXT
PIC16C54HS	512 x 12	12	18	4.0–20 MHz	XTAL, EXT
PIC16C55XT	512 x 12	20	28	0.4–4 MHz	XTAL, EXT
PIC16C55RC	512 x 12	20	28	0.4–4 MHz	RC, EXT
PIC16C55LP	512 x 12	20	28	25–500 kHz	XTAL, ET
PIC16C55HS	512 x 12	20	28	4.0–20 MHz	XTAL, EXT

PACKAGING

The 18-pin devices, PIC16C52/54, will be available in 18-lead dual-in-line plastic and windowed ceramic packages.

The 28-pin devices, PIC16C53/55, will be available in 28-lead dual-in-line plastic and windowed ceramic packages. PLCC packages will also be available.

ARCHITECTURAL DESCRIPTION

The PIC16C5x microcontrollers are low-power, high-speed CMOS devices containing RAM, I/O, and a central processing unit as well as a customer-defined program memory (EPROM) on a single chip. The firmware architecture is based on a register file concept with separated data and instruction buses (modified Harvard architecture). The data bus and memory are 8 bits wide while the program bus and memory have a width of 12 bits. This concept allows simple yet powerful commands designed to emphasize bit, byte and register operations. Overlapping instruction fetch and execution cycles allow for high-speed operation, meaning that, while one instruction is executing, the following instruction is already being read from the program memory. The 8-bit data bus connects two basic functional elements: the register file composed of 32 addressable 8-bit registers, including the I/O ports; and an 8-bit-wide arithmetic logic unit. An 8-bit-wide data path allows transfers of constant and literal values from the program memory to the W register. The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the real-time clock counter (RTCC), the program counter (PC), the status register, the I/O registers (ports), and the file select register. The general purpose registers are used for data and control information under command of the instructions. The arithmetic logic unit contains one temporary working register (W register) and gating to perform Boolean functions between data held in the W register and any file register. The program memory consists of a 512-x-12-bit-wide EPROM (256-x-12 for the PIC16C52/53) containing the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the program counter that automatically increments to execute in-line programs. Program control operations can be performed by bit test and skip instructions; call instructions; jump instructions; or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy-to-use subroutine nesting.

PIN FUNCTIONS

SIGNAL NAME	DEFINITION
OSC1 (Input) OSC2 (Output)	These pins are the time base inputs to which a crystal, ceramic resonator, RC combination, or an external single phase clock can be connected. The frequency of oscillation is 4X the instruction cycle frequency. (OSC2 functions as CLKOUT output with RC oscillator) (Fclkout = Fosc/4)
RTCC (Input)	External real-time clock counter input. One bit in the OPTION register determines the trigger edge of this input. RTE = 1 (default) trigger on falling edge. RTE = 0 trigger on rising edge. This pin will be disregarded if the RTS bit in the OPTION register is cleared (RTS=0). An optional 8 bit prescaler, which is user definable by the OPTION register, can divide the RTCC input signal in the range from 1:2 up to 1:256.
RA0–RA3 (Input/Output)	4 user-programmable I/O lines (F5).
RB0–RB7 (Input/Output)	8 user-programmable I/O lines (F6).
RC0–RC7 (Input/Output)	8 user-programmable I/O lines (F7) (PIC16C53/55 only). All inputs and outputs are under direct control of the program. The instruction TRIS (f) determines which line is putting out data or is in the high impedance mode for reading in data.
$\overline{MCLR}$	Master clear. Schmitt trigger input with internal pull-up resistor. Initializes the PC to 1FFh (0FFh for PIC16C52/53) and puts all I/O lines into the high impedance mode. The watchdog timer is cleared and the OPTION register is set to all "ones." $\overline{MCLR}$ should be left unconnected (OSC start up time = 10 ms) or connected to an external RC network for longer start up times. The on-chip start-up timer (OST) is enabled as soon as V_{CC} has reached a level > 2.0V and holds the device in the master clear mode for about 10 ms.
V_{CC}	Power supply.
GND	Ground.
N/C	No Connect (PIC16C53/55 only).

REGISTER FILE ARRANGEMENT

FILE	FUNCTION
F0	Not a physically implemented register. F0 calls for the contents of the file select register (low order 5 bits) to be used to select a file register. F0 is useful as an indirect address pointer. For example, W + F0 → W will add the contents of the register pointed to by the FSR (F4) to W and place the result in W (instruction ADDWF F0,W).
F1	Real-time clock counter register. This register can be loaded and read by the program. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input RTCC if the RTE bit in the option register is "1." A 8-bit prescaler can be assigned by the OPTION register. (Note: RTCC and watchdog timer share one common prescaler. If it is assigned to the RTCC, the WDT has a fixed period of 10ms.) If the RTS bit of the OPTION register is cleared to "0," the signal on the RTCC pin is disregarded and the RTCC register is incremented by the internal CLKOUT signal, which is fosc/4.
F2	Program counter. The PC is automatically incremented during each instruction cycle and can be read and written (MOVF PC and MOVWF PC) under program control. Although it is 9 bits wide, only the low-order 8 bits are accessable by the program. The MSB is automatically set to "0" if a CALL or any other instruction is executed that overwrites the autoincrement function of the PC (exception: GOTO k).
F3	Status word register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction (except TO and PD). (7) (6) (5) (4) (3) (2) (1) (0) 1 1 1 TO PD Z DC C
	C (Carry): For ADDWF and SUBWF instructions, this bit is set if there is a carry out from the most significant bit of the calculation. For ROTATE (RRF, RLF) instructions, this bit is loaded with either the high- or low-order bit of the addressed register file.
	DC (Digit Carry): For ADDWF and SUBWF instructions, this bit is set if there is a carry out from the 4th low order bit of the calculation.
	Z (Zero): Set if the result of an arithmetic or logic operation is zero.
	PD (Power Down): Set to "1" during "power on." This bit is reset to "0" under program control by the SLEEP instruction and can be set by the CLRWDT instruction (see PD and TO detail below).
	TO (Time Out): Set to "1" during power up and by the CLRWDT command under program control. This bit is reset to "0" by a WDT time out. Thus, the program can determine if the processor was "powered up" or reset by a WDT time outs. (see PD and TO detail below).
	Bits 5–7: These bits are defined as logic "ones."
F4	File select register (FSR). Only the low-order 5 bits are used. The FSR is used in generating effective file register addresses under program control (indirect addressing as described with F0). When accessed as a directly addressed file, the upper 3 bits are read as "ones."
F5	I/O register A (PORT A). Only the low-order 4 bits (RA0–RA3) are used. RA4–RA7 are defined as "zeros."
F6	I/O register B (PORT B).
F7	I/O register C (PORT C) (PIC 16C53/55 only). General purpose register (PIC16C52/54).
F8–31	General purpose registers.

PD and TO Status Bits Detail
Bits 3 and 4 of the status register file F3 can be used by the program to determine the processor history if the program counter is set to 1FF (hex) by a low-to-high transition of the $\overline{MCLR}$ input or a WDT time out.

FUNCTION	PD	TO	<PC>
Power up	1	1	1FFh
SLEEP	0	1	XXX*
$\overline{MCLR}$ wake up	0	1	1FF
WDT wake up	0	0	1FF
WDT time out	1	0	1FF
CLRWDT	1	1	XXX*

*XXX = current instruction address.

The PD status flag is not automatically set to one after the instruction or a WDT timeout has occurred. This means that the PD bit stays zero even after wake up by pulling $\overline{MCLR}$ low or a watchdog timer time out has occurred until it is set to one under program control (CLRWDT).

However, a SLEEP command will be recognized and executed regardless of whether PD is zero or one.

The TO bit stays zero after a WDT time out until a CLRWDT command has been executed. However, the next WDT time out will be recognized again, regardless of the status of the TO flag.

For all other instructions except SLEEP and CLRWDT, TO and PD are read-only bits.

SPECIAL PURPOSE REGISTERS

REGISTER	FUNCTION
W	Working register. Holds second operand in two-byte instructions and/or supports the internal data transfer.
OPTION (Write Only)	Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. 0 1 2 3 4 5 PS0 PS1 PS2 PA RTS RTE
	PA: prescaler assignment (0 = WDT, 1 = RTCC)
	Prescaler value PS2 PS1 PS0 Rate 0 0 0 1:2 0 0 1 1:4 0 1 0 1:8 0 1 1 1:16 1 0 0 1:32 1 0 1 1:64 1 1 0 1:128 1 1 1 1:256
	RTS: RTCC signal source 0 int.CLKOUT 1 RTCC pin
	RTE: RTCC signal edge 0 rising edge 1 falling edge
	NOTE: A $\overline{MCLR}$ reset will set all bits in the OPTION register to one.

BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code that specifies the instruction type and one or more operands specifying the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator that selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight- or nine-bit constant or literal value.

For an oscillator frequency of 20MHz the instruction execution time is 200 ns, unless a conditional test is true or the program counter is changed as a result of an instruction (e.g. GOTO k or MOVWF F2). In these cases, the instruction execution time is 400 ns.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11–6)	(5)	(4–0)
OP CODE	d	f (FILE #)

For d = 0, f → W (PICAL (GIM PIC assembler software) accepts d=0 or d=W in the mnemonic)
d = 1, f → f (if d is omitted, assembler assigns d = 1)

INSTRUCTION-BINARY	(HEX)	NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED	NOTES
0000 0000 0000	000	No operation	NOP		—	None	
0000 001f f f f f	02f	Move W to f	MOVMF	f	W → f	None	1
0000 0100 0000	040	Clear W	CLRW	—	0 → W	Z	
0000 011f f f f f	06f	Clear f	CLRF	f	0 → f	Z	
0000 10df f f f f	08f	Subtract W from f	SUBWF	f, d	f − W → d [f + $\overline{W}$ + 1 → d]	C, DC, Z	1, 2
0000 11df f f f f	0Cf	Decrement f	DECF	f, d	f − 1 → d	Z	2
0001 00df f f f f	10f	Inclusive OR W and f	IORWF	f, d	W v f → d	Z	2
0001 01df f f f f	14f	AND W and f	ANDWF	f, d	W·f → d	Z	2
0001 10df f f f f	18f	Exclusive OR W and f	XORWF	f, d	W ⊕ f → d	Z	2
0001 11df f f f f	1Cf	Add W and f	ADDWF	f, d	W + f → d	C, DC, Z	1, 2
0010 00df f f f f	20f	Move f	MOVF	f, d	f → d	Z	2
0010 01df f f f f	24f	Complement f	COMF	f, d	$\overline{f}$ → d	Z	2
0010 10df f f f f	28f	Increment f	INCF	f, d	f + 1 → d	Z	2
0010 11df f f f f	2Cf	Decrement f, skip if zero	DECFSZ	f, d	f − 1 → d, skip if zero	None	2
0011 00df f f f f	30f	Rotate right f	RRF	f, d	f(n) → d(n−1), f(0) → C, C → d(7)	C	2
0011 01df f f f f	34f	Rotate left f	RLF	f, d	f(n) → d(n+1), f(7) → C, C → d(0)	C	2
0011 10df f f f f	38f	Swap halves f	SWAPF	f, d	f(0−3) ↔ f(4−7) → d	None	2
0011 11df f f f f	3Cf	Increment f, skip if zero	INCFSZ	f, d	f + 1 → d, skip if zero	None	2

BIT-ORIENTED FILE REGISTER OPERATIONS

(11–6)	(7–5)	(4–0)
OP CODE	b (BIT #)	f (FILE #)

INSTRUCTION-BINARY	(HEX)	NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED	NOTES
0100 bbbf f f f f	4bf	Bit clear f	BCF	f, b	0 → f(b)	None	2
0101 bbbf f f f f	5bf	Bit set f	BSF	f, b	1 → f(b)	None	2
0110 bbbf f f f f	6bf	Bit test, f, skip if clear	BTFSC	f, b	Bit test f(b): skip if clear	None	
0111 bbbf f f f f	7bf	Bit test f, skip if set	BTFSS	f, b	Bit test f(b): skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11–8)	(7–0)
OP CODE	k (LITERAL)

INSTRUCTION-BINARY	(HEX)	NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED	NOTES
0000 0000 0010	002	Load OPTION register	OPTION	—	W → OPTION register	None	
0000 0000 0011	003	Go into standby mode	SLEEP	—	Stop oscillator I/O ports = High Z	PD	
0000 0000 0100	004	Clear watchdog timer	CLRWDT	—	0 → WDT	TO, PD	
0000 0000 0 f f f	00f	Tristate port f	TRIS	f	W → Tristate status f	None	3
1000 kkkk kkkk	8kk	Return, place literal in W	RETLW	k	k → W, Stack → PC	None	
1001 kkkk kkkk	9kk	Call subroutine	CALL	k	PC + 1→ Stack, k → PC	None	1
101k kkkk kkkk	Akk	Go To address (k is 9 bit)	GOTO	k	k → PC (9 bits)	None	
1100 kkkk kkkk	Ckk	Move literal to W	MOVLW	k	k → W	None	
1101 kkkk kkkk	Dkk	Incl. OR literal and W	IORLW	k	k v W → W	Z	
1110 kkkk kkkk	Ekk	AND literal and W	ANDLW	k	k·W → W	Z	
1111 kkkk kkkk	Fkk	Excl. OR literal and W	XORLW	k	k ⊕ W → W	Z	

Notes 1, 2, 3 (see next page).

NOTES:

1. The 9th bit of the program counter is zero for a CALL and a MOVWF F2 or ADDWF F2. Therefore, subroutines and jump tables must be located in program memory locations 000–0FF (hex). However, subroutines can be called from anywhere in the program memory since the stack is 9 bits wide.

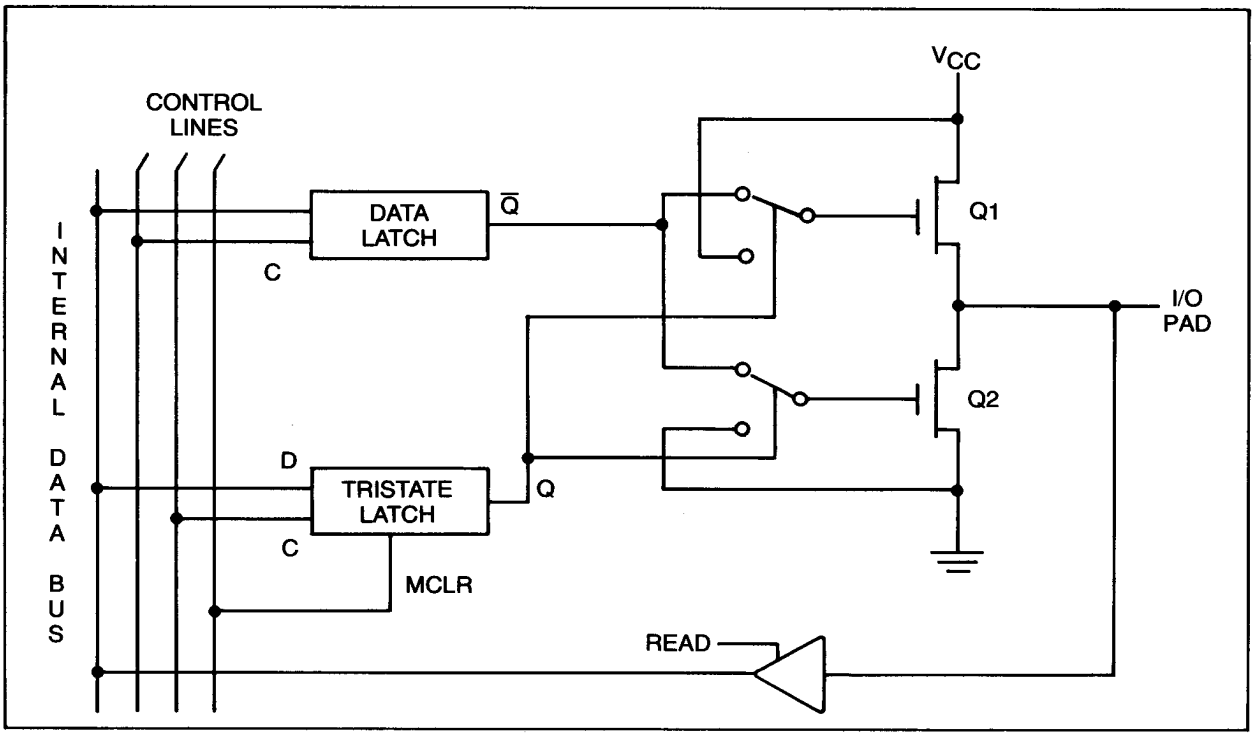
2. When an I/O register is modified as a function of itself, the value used will be that value present on the pins themselves. For example, an output pin latched high but driven low by an external device will be relatched in the low state.

3. The instruction "TRIS f," where f = 5 or 6 (PIC16C52/54) or f = 5, 6 or 7 (PIC16C53/55), causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffer.

I/O INTERFACING

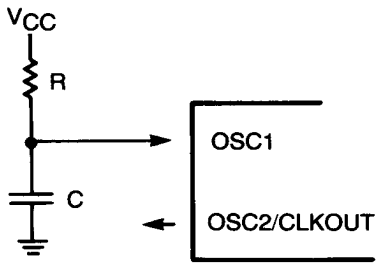
The equivalent circuit for an I/O port bit is shown in Figure 1 below as it would interface with either the input of a TTL device (PIC is outputting) or the output of a tristate TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O port, the port must first be set to the high impedance state under program control (TRIS command). This turns off Q1 and Q2, allowing the TTL tristate device to drive the pin.

TYPICAL INTERFACE BIDIRECTIONAL I/O LINE (Figure 1) (shown in active output state)

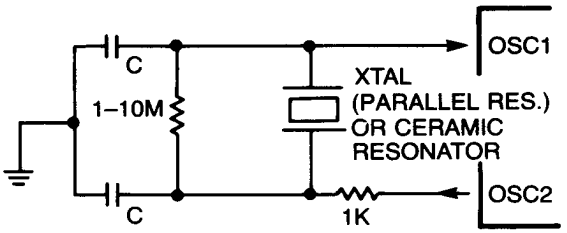


TYPICAL OSCILLATOR CIRCUITS (Figure 2)

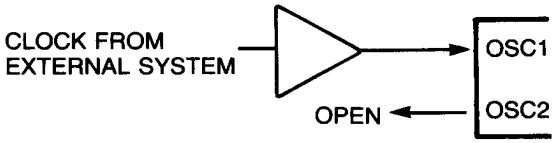
RC operation



Crystal operation (or ceramic resonator)



External clock input operation



Watchdog timer (WDT)/ Oscillator start-up timer (OST)

A free running on-chip oscillator with a basic time period of 10 ms performs two particular functions:

1. Watchdog timer
   An EPROM fuse (WDTE bit) is available to control the watchdog timer. If the WDTE (watchdog timer enable) bit is zero, the WDT must be periodically cleared within the selected time-out period under software control (CLRWDT command). Otherwise, the WDT will expire and reset the entire processor logic by generating a $\overline{MCLR}$ signal. This is the case even if the processor is in power down mode. The PD and TO bits of the status register F3 can be used by the program to check whether a power-up, wake-up, or time-out condition occurred. The optional 8-bit RTCC/WDT prescaler can be assigned to the watchdog timer allowing a user-definable time-out period between 20 ms and 2.56 seconds. In this case the RTCC input ratio is 1:1.

2. Oscillator start-up timer (OST)
   The WDT/OST timer is triggered if the voltage level on the $\overline{MCLR}$ input changes from low to high. The threshold voltage is typically 2.0 volts. If triggered, it inhibits the normal processor operation for about 10 ms, allowing the oscillator circuitry sufficient time to start up. The TO bit of the status register F3 is not reset by an OST time out. The WDTE bit does not influence the OST function.

Power down mode

The power down mode can be entered by a special software command "SLEEP." In this mode, the oscillator is stopped and the I/O pins are tristated (with inputs clamped to V_{CC}). However, the watch dog timer may be running if it is enabled by the appropriate EPROM fuse (WDTE). The PIC16C52/53/54/55 can be awakened either by pulsing $\overline{MCLR}$ low or by a watchdog timer time out (if WDTE = 0). In both cases the oscillator start-up timer is triggered and the normal processor operation will not start until the OST has expired (10 ms). Thus, the OSC circuitry has enough time to establish normal operation. No external R/C combination on the $\overline{MCLR}$ pin is required for that purpose. If there is an external R/C combination, care must be taken as the capacitor will not be discharged completely and an extension of the OST time period is not possible. The PD bit in the STATUS register, which is set to "one" during power on only, will be cleared by the "SLEEP" command. Since the PD is not changed by $\overline{MCLR}$ it can be used to determine if the processor was powered up or awakened from the stand by mode.

Code protection bit (security bit)

The code protection bit (CP) is a special EPROM fuse. If CP is blown (= zero), the contents of the program EPROM cannot be read by the verify command. A verify cycle results in an output of four bits on port A which does not allow instruction recognition. This feature offers unique protection against unauthorized copying of the program itself. The configuration EPROM is not affected by these bits and can be read to allow part identification, even if the code protection bits are activated.

EPROM programming and testing

The EPROM programming is controlled by the signals on $\overline{MCLR}$ (V_{PP}), OSC1 input (program pulse), RTCC (program/verify selection), Port A and Port B (data). See Table 1 for the valid combinations of these signals.

The 12-bit-wide program EPROM is programmed in one step. Also, the data-low byte must be provided on Port B and the data-high byte on Port A. The RTCC pin must be held at a low level to select the programming mode; however, a programming voltage of 12.5V is provided on the $\overline{MCLR}$ pin. The programming pulse has to be provided by a high-to-low transition on the OSC1 input. The EPROM address is provided by the program counter.

TABLE 1: TEST, PROGRAM AND OPERATION MODES

FUNCTION	$\overline{MCLR}$	RTCC	OSC1	OSC2	PORT A	PORT B
Reset	L	X			Hi-Z	Hi-Z
Standby	H	X			Hi-Z	Hi-Z
Normal operation	H	X			I/O	I/O
Program	12.5V	L		X	data high	data low
Verify	12.5V	H		CLKOUT	data high	data low
TEST 1 (factory use only!)	12.5V	12.5V		CLKOUT		
INCPC (increment PC)	12.5V	12.5V		CLKOUT	0	0
TEST 2 (factory use only!)	L	12.5V				
TEST 3 (factory use only!)	H	12.5V				

X = don't care, but within the V_{IL} and V_{IH} limits
L = logic low level (V_{IL})
H = logic high level (V_{IH})

General Instrument Microelectronics will make special programming equipment available for development, prototyping and low-volume production.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature under bias . . . −55 to +125°C
Storage temperature . . . . . −65 to +150°C
Voltage on any pin with respect to V_{SS} . . . . . −0.3V to V_{CC} +0.3V
Max. voltage on V_{CC} with respect to V_{SS} . . . +9.5V
Max. voltage on $\overline{MCLR}$ and RTCC with respect to V_{SS} . . . . . +13V
Total power dissipation (Note 1) 300mW

* **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Operating temperature 0° to +70°C (commercial)
−40 to +85°C (industrial)

CHARACTERISTICS	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Supply Voltage	V_{CC3} V_{CC2} V_{CC1}	2.5 4.0 4.75		6.0 6.0 6.0	V V V	Fosc = 32kHz Fosc = 2MHz Fosc = 20MHz
Supply Current (Note 2)	I_{CC1}			30	mA	20MHz, V_{CC} = 6.0V, T = 0°C to +70°C external square wave
	I_{CC2}			2.5	mA	2MHz, V_{CC} = 5.0V, external square wave
	I_{CC3}			35	μA	32kHz, V_{CC} = 3V
power down	I_{CC4}		<10		μA	WDT enabled, V_{CC} = 2.5V
	I_{CC5}		<1		μA	WDT disabled, V_{CC} = 2.5V
Input Low Voltage	V_{IL} V_{ILMC}	V_{SS}		.2 V_{CC} 1.5	V V	 $\overline{MCLR}$ input
Input High Voltage	V_{IH} V_{IHMC} V_{IHRTCC}	2.0 2.0 2.0		V_{CC} V_{CC} V_{CC}	V V V	V_{CC} = 5V ±10% $\overline{MCLR}$ input (Note 3) RTCC input (Note 3)
Output High Voltage	V_{OH}	V_{CC} − 0.5			V	I_{OH} = 0.4mA, V_{CC} = 4.5V I_{OH} = 0.1mA, V_{CC} = 3.0V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA, V_{CC} = 4.5V I_{OL} = 0.2mA, V_{CC} = 3.0V
Input Leakage Current	I_{IL}			±1	μA	$V_{SS} < V_{pin} < V_{CC}$
Output Sink Current (I/O ports)	I_{OL}			12	mA	Note 1, V_{OL} = TBD
Output Source Current	I_{OH}			−5	mA	Note 1, V_{OH} = TBD

Typical data for T = +25°C

Notes:

1. Total power dissipation should not exceed 300mW for the package. Power dissipation is calculated as follows:

$$P_{dis} = V_{CC} \times I_{CC} + \Sigma(V_{CC} - V_{IL}) \times I_{IL} + \Sigma(V_{CC} - V_{OH}) \times I_{OH} + \Sigma(V_{OL} \times I_{OL})$$

2. The supply current is a function of the operating voltage and frequency and can be estimated with the following formula:

(frequency F > 500kHz)

$$I_{CCX} = \frac{I_{CC2}}{2} * F * \frac{U}{5} \text{ [mA]}$$

with I_{CC2} = supply current (in mA) at 2MHz, 5 volts.
F = oscillator frequency in MHz
U = supply voltage in volts

It should be emphasized that above formulas are approximations only. Other factors, such as bus loading, oscillator type, bus rate, and temperature, also influence the current consumption.

3. Instantaneous voltages on RTCC and $\overline{MCLR}$ inputs must not exceed V_{CC} + 1V. Exceeding this specification might force the device into test mode and normal operation cannot be guaranteed.

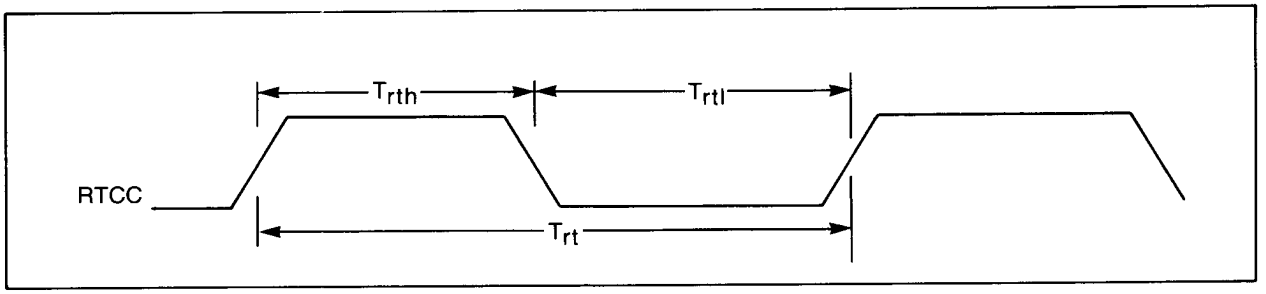
AC CHARACTERISTICS

Standard Conditions (unless otherwise noted)

CHARACTERISTIC	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Instruction Cycle Time PIC16C5xHS	T_{cy1}	0.2		1	μs	4.0 – 20MHz osc frequency (Note 1) (T = 0°C to +70°C) 4.75V < V_{CC} < 6.0V
PIC16C5xXT/RC	T_{cy2}	1		10	μs	0.400 – 4.0MHz osc frequency (Note 1) 4.0V < V_{CC} < 6.0V
PIC16C5xLP	T_{cy3}	10		160	μs	0.025 – 0.400MHz osc frequency (Note 1) 3.0V < V_{CC} < 6.0V
External Clock	T_{cy4}	Note 2		DC	μs	DC – 20MHz osc frequency (Note 1) V_{CC}/frequency ranges as above
RTCC Input Period High Pulse Width Low Pulse Width	T_{rt} T_{rth} T_{rtl}	$T_{cyx}+0.05$ 1/2 T_{cyx} 1/2 T_{cyx}			μs	external RTCC input

Notes:
1. Instruction cycle period (T_{cyx}) equals 4X the input oscillator time base period.
2. Minimum instruction cycle time equals T_{cy1}, T_{cy2}, or T_{cy3}, depending on selected version.

RTCC TIMING (Figure 3)

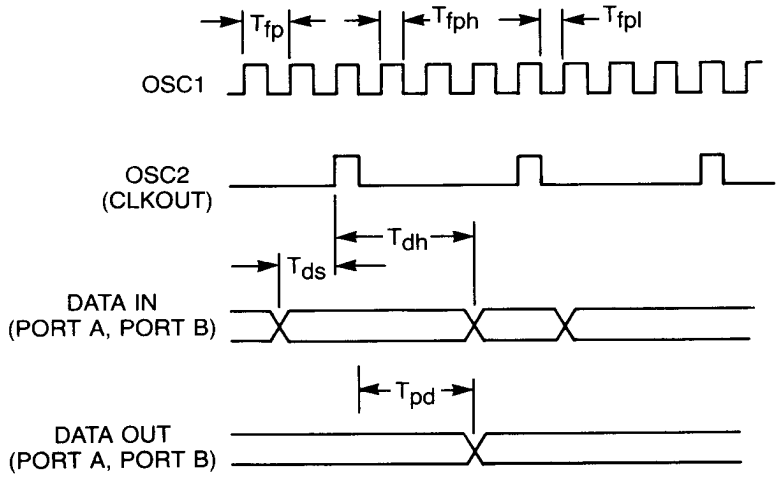


PROGRAMMING TIMING

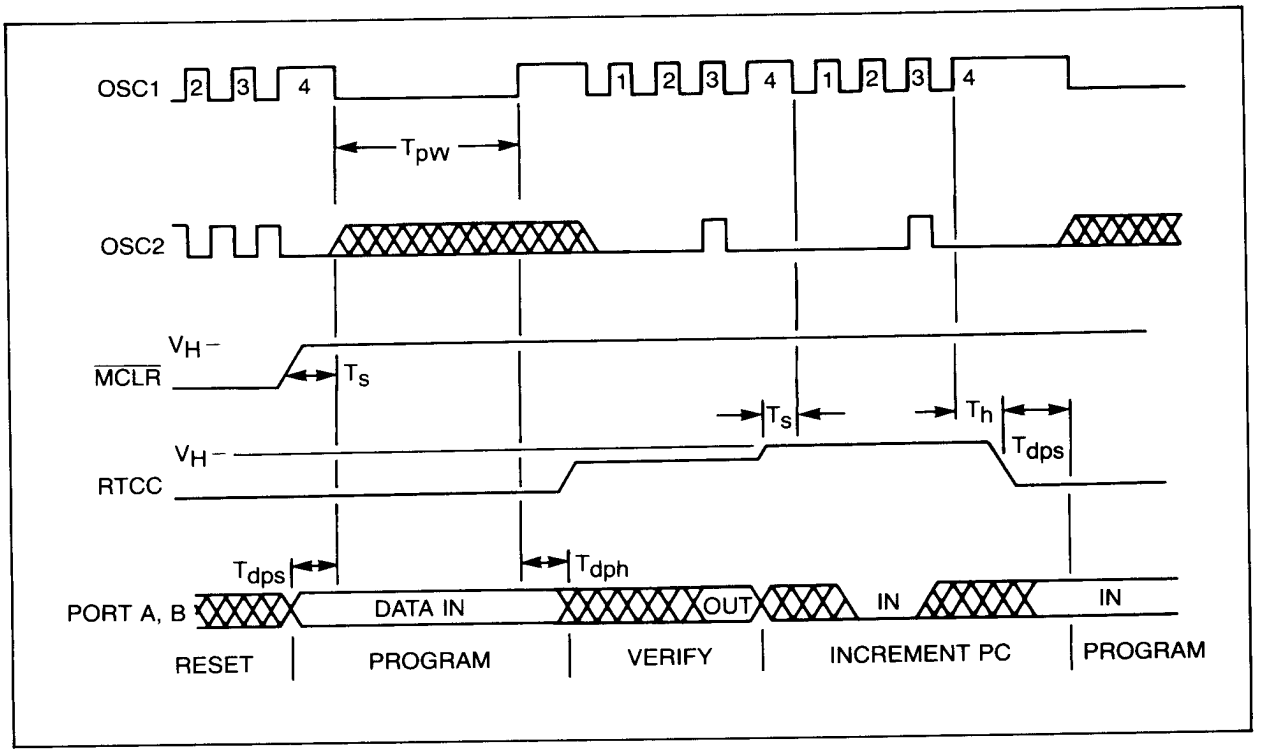
Temperature range: +10°C to +50°C

CHARACTERISTIC	SYM	MIN	TYP	MAX	UNIT	CONDITIONS
OSC1 Input Time Period OSC1 Input High Time OSC1 Input Low Time	T_{fp} T_{fph} T_{fpl}			160 80 80	μs μs μs	
OSC1 Programming Pulse Width	T_{pw}	0.1	1	20	ms	
Data in Setup Time (Port A and B) Data in Hold Time (Port A and B) Data Out Delay Time (Port B, verify)	t_{ds} t_{dh} t_{pd}	TBD TBD		 TBD		
High Voltage Setup Time High Voltage Hold Time	T_s T_h	TBD TBD				
Program Mode Setup Time	T_{ps}	TBD				
Program Data Setup Time Program Data Hold Time	T_{dps} T_{dph}	TBD TBD				

TIMING DIAGRAM VERIFY, INCPC (Figure 4)



TIMING DIAGRAM PROGRAM, VERIFY, INCPC (Figure 5)



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