

## EXTENDED TEMPERATURE RANGE

PIC series microcomputers are available in two temperature ranges. The preceding data sheets describe the commercial grade device, 0°C to 70°C centigrade. An industrial/automotive temperature range version is available. The -40° to 85° centigrade option is specified with the addition of a suffix, I, to the part number.

The specifications for these devices differ from their commercial grade counterparts in a few electrical parameters, typically interface voltage/current levels. Refer to the data sheets for details.

## OPEN DRAIN OPTIONS

### **PIC1650A, PIC1670**

#### **Open-Drain I/O Ports**

Any or all of the I/O lines may be specified by the customer to be open drain, that is, the internal pull-up device will be removed. This enables the outputs to be pulled up to +10.0V maximum with an external pull-up resistor, allowing easy interface to external devices requiring a logic one level greater than  $V_{DD}$  of the PIC. In the logic one state, the leakage current of the I/O port is  $\pm 5\mu A$ , maximum.

The customer shall specify on the "PIC Series Order Form" the pin number and port name (e.g., "RB3") of each port required to be open drain.

### **PIC1655A, PIC1656**

#### **Open Drain I/O, Input and Output Ports**

Any or all of the I/O, input only or output only lines may be specified by the customer to be open drain, that is, the internal pull-up device will be removed. This enables the outputs to be pulled up to +10.0V maximum with an external pull-up resistor, allowing easy interface to external devices requiring a logic one

level greater than  $V_{DD}$  of the PIC. In the logic one state, the leakage current of the I/O port is  $\pm 5\mu A$ , maximum.

The customer shall specify on the "PIC Series Order Form" the pin number and port name (e.g., "RB3") of each port required to be open drain.

### **PIC16C55**

#### **Input-only, Output-only and I/O Ports**

Any or all of the input-only and I/O lines may be specified to have an internal pull-up resistor inserted via a mask option. This allows easy interface to an external transistor or switch without the need for an external pull-up resistor. Furthermore, any or all of the output-only or I/O pull-down transistors can be specified to be removed via a mask option. This facilitates interfacing with external circuitry which has signal swings below  $V_{SS}$ . In this case the maximum voltage permitted to be applied to the pin is -12V with respect to  $V_{DD}$ .

### **PIC1654**

#### **Optional Internal Connection to RTCC**

A mask option will allow an internal clock signal whose period is equal to the instruction execution time to drive the real time clock/counter register. In this mode, transitions in the RTCC pin will be disregarded.

### **PIC1655XT**

#### **Prescaler Division Ratio**

A mask option will allow the division ratio of the RTCC prescaler to be selected as 1, 2, 4, 8 or 16. Consult the data sheet for the details.

## 8 Bit Microcomputer

### FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained oscillator for crystal, ceramic resonator or RC network
- Access to RAM registers inherent in instruction
- Wide power supply operating range (2.5V to 6.0V)
- Low power dissipation
- 4 inputs, 8 outputs, 8 bi-directional I/O lines
- 2 level stack for subroutine nesting
- Software compatible with other PIC series microcomputers

### DESCRIPTION

The PIC16C55 microcomputer is a CMOS device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

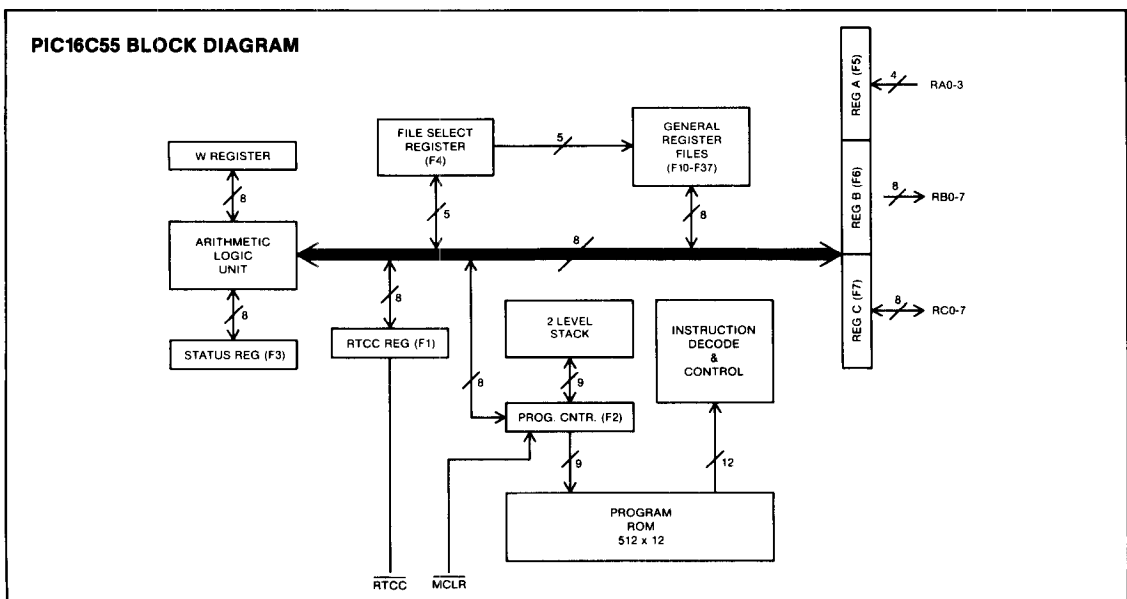
The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to power tools, telecommunications systems, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use

instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC16C55 is fabricated with complementary MOS technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or crystal or ceramic resonator, for greater accuracy) to establish the frequency.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC16C63. The PIC16C63 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PIC Field Demo System is available containing a PIC16C63 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.



**ARCHITECTURAL DESCRIPTION**

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register,

and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

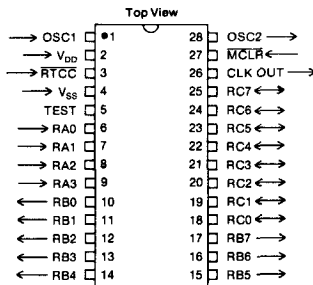
The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

**PIN FUNCTIONS**

Signal	Function
OSC1 (Input), OSC2 (output)	Oscillator pins. These pins are used to derive the internal clock for the chip. A crystal, ceramic resonator or RC network may be used in conjunction with OSC1 and OSC2. Additionally, OSC1 may be driven by an external oscillator.
RTCC (Input)	Real Time Clock Counter. File 1 increments on falling edges applied to this pin. This register can be loaded and read by the program.
RA0-3 (Input)	Dedicated input lines read under control of the program. The 4 MSB's are always read as logic zeroes.
RB0-7 (output)	Dedicated output lines, user programmable under direct control of the program.
RC0-7 (input/output)	User programmable input/output lines. These are controlled by the program to be inputs and/or outputs.
MCLR (Input)	Master Clear. Used to initialize the internal ROM program to address 777 octal and set output status latches into the high impedance state.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be connected to V <sub>SS</sub> or left open circuit for normal operation.
V <sub>DD</sub>	Power supply.
V <sub>SS</sub>	Ground

MICROCOMPUTER

**PIN CONFIGURATION**  
28 LEAD DUAL IN LINE



**REGISTER FILE ARRANGEMENT**

File (Octal)	Function																
<b>F0</b>	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.																
<b>F1</b>	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$ . However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.																
<b>F2</b>	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.																
<b>F3</b>	Status Word Register. When F3 is the destination register, the status flags are overwritten. <div style="text-align: center; margin: 10px 0;"> <table border="1" style="margin: auto;"> <tr> <td style="padding: 2px 10px;">(7)</td> <td style="padding: 2px 10px;">(6)</td> <td style="padding: 2px 10px;">(5)</td> <td style="padding: 2px 10px;">(4)</td> <td style="padding: 2px 10px;">(3)</td> <td style="padding: 2px 10px;">(2)</td> <td style="padding: 2px 10px;">(1)</td> <td style="padding: 2px 10px;">(0)</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">Z</td> <td style="text-align: center;">DC</td> <td style="text-align: center;">C</td> </tr> </table> </div> <p>C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.  For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.</p> <p>DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.</p> <p>Z (Zero): Set if the result of an arithmetic operation is zero.</p> <p>Bits: 3-7 These bits are defined as logic ones.</p>	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)	1	1	1	1	1	Z	DC	C
(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)										
1	1	1	1	1	Z	DC	C										
<b>F4</b>	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.																
<b>F5</b>	Input Register A (A0-A3). (A4-A7 defined as zeroes). Output operations to this register are not defined.																
<b>F6</b>	Output Register B (B0-B7). When an instruction involving a read is executed on this port (all instructions except literal and control operations, NOP, MOVWF, CLRWF and CLRF) the data will be read from the latch (not from the pins).																
<b>F7</b>	I/O Register C (C0-C7). For use as an input port, the output latch should be tristated. The input port is non-latching so an input must be present until read by an instruction. When an instruction involving a read is executed on this port (as in F6), the data will be read from the pins, whether or not it is tristated (i.e., selected as an input or an output).																
<b>F10-F37</b>	General Purpose Registers.																

## Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the

PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 5 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 10 μsec.

### BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PIC16C accepts d = 0 or d = W in the mnemonic)  
 d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP — —	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF f W→f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW — 0→W	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF f 0→f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF f, d f - W→d [f+W+1→d]	f - W→d [f+W+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECf f, d f - 1→d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF f, d WVf→d	WVf→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF f, d W∩f→d	W∩f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF f, d W⊕f→d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF f, d W+f→d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF f, d f→d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF f, d f→d	f→d	Z
001 010 dff fff (1200)	Increment f	INCF f, d f+1→d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ f, d f - 1→d, skip if Zero	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF f, d f(n)→d(n-1), f(0)→C, C→d(7)	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF f, d f(n)→d(n+1), f(7)→C, C→d(0)	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF f, d f(0-3)↔f(4-7)→d	f(0-3)↔f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ f, d f+1→d, skip if zero	f+1→d, skip if zero	None

### BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF f, b 0→f(b)	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF f, b 1→f(b)	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSZ f, b Bit Test f(b): skip if clear	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSZ f, b Bit Test f(b): skip if set	Bit Test f(b): skip if set	None

### LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Operation	Status Affected
000 000 000 010 (0002)	Return	RETURN —	Stack→PC	None
000 000 0ff fff (0000)	Tristate port f	TRIS f	W→Tristate status f [f=F6 or F7]	None
100 0kk kkk kkk (4000)	Return and place Literal in W	RETlw k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW k	kVW→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW k	k∩W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW k	k⊕W→W	Z

#### NOTES:

- The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
- When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.
- TRIS f (where f=6 or 7) causes the contents of W to be written to the tristate latches of the specified file. A one forces the pin to tristate the output buffer to a high impedance state.

## SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equiv-

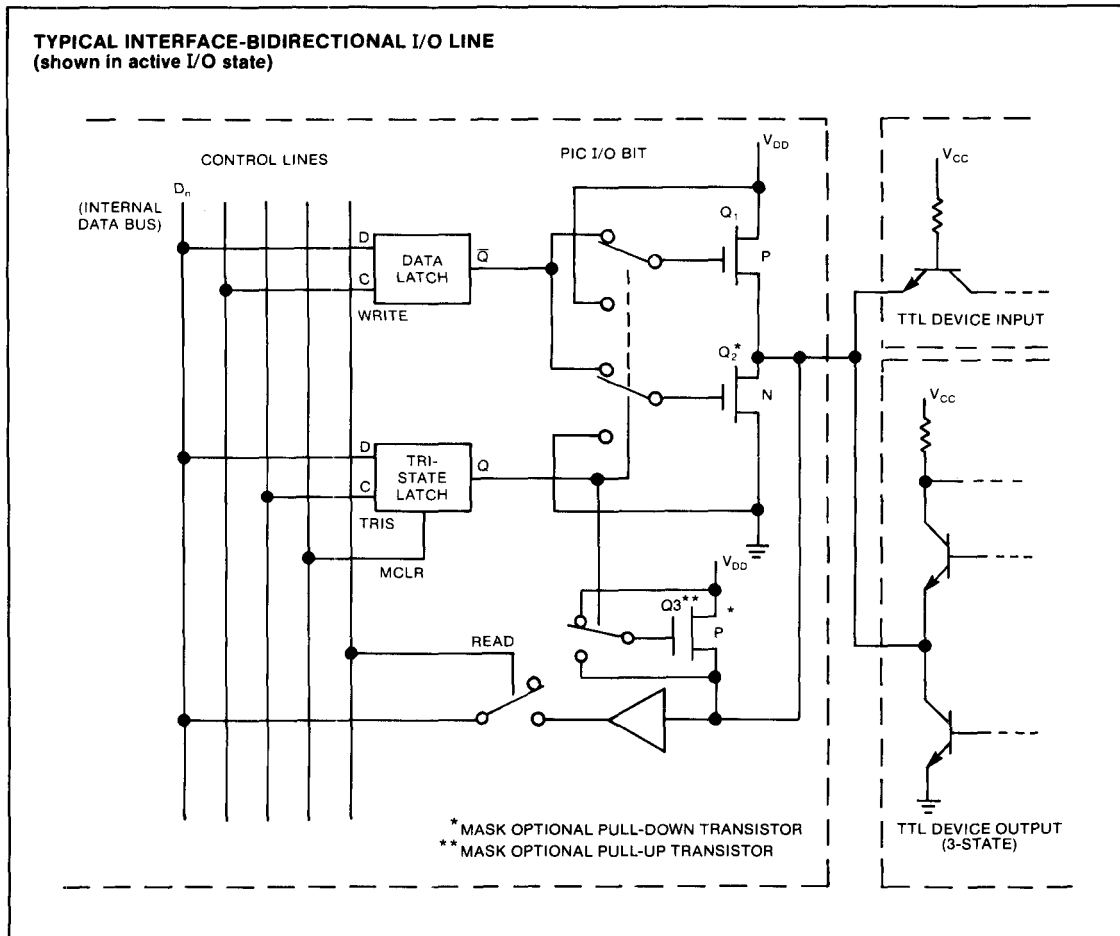
alent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140)	Negate File	NEGF f,d	COMF f, 1	
001 010 dff fff (1200)			INCF f, d	Z
011 000 000 011 (3003)	Add Carry to File	ADDCF f, d	BTFSC 3,0	
001 010 dff fff (1200)			INCF f, d	Z
011 000 000 011 (3003)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0	
000 011 dff fff (0300)			DECF f, d	Z
011 000 100 011 (3043)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1	
001 010 dff fff (1200)			INCF f,d	Z
011 000 100 011 (3043)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1	
000 011 dff fff (0300)			DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003)	Branch on Carry	BC k	BTFSC 3,0	
101 kkk kkk kkk (5000)			GOTO k	—
011 100 000 011 (3403)	Branch on No Carry	BNC k	BTFSS 3,0	
101 kkk kkk kkk (5000)			GOTO k	—
011 100 100 011 (3043)	Branch on Digit Carry	BDC k	BTFSC 3,1	
101 kkk kkk kkk (5000)			GOTO k	—
011 001 000 011 (3443)	Branch on No Digit Carry	BNDC k	BTFSS 3,1	
101 kkk kkk kkk (5000)			GOTO k	—
011 101 000 011 (3103)	Branch on Zero	BZ k	BTFSC 3,2	
101 kkk kkk kkk (5000)			GOTO k	—
011 101 000 011 (3503)	Branch on No Zero	BNZ k	BTFSS 3,2	
101 kkk kkk kkk (5000)			GOTO k	—

## I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of a tri-state TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a

PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port must first be set to the high impedance state under program control. This turns off  $Q_1$  and  $Q_2$  and turns on  $Q_3$  (if present), allowing the TTL tri-state device to drive the pin.



## Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation. (Note that for an output only port the latch, not the pin is read.)

### Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. For use as an input port the output must be set to the high impedance state via the tri-state latch. Thus the external device inputs to the PIC circuit by forcing the input line high or low. If the input lines are not tri-stated then refer to PIC1650A

programming cautions. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result.

### Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVf, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if  $t_{pd}$  (See I/O Timing Diagram) is greater than  $1/5t_{cy}$  (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

**ELECTRICAL CHARACTERISTICS****Maximum Ratings\***

Ambient Temperature Under Bias	125°C
Storage Temperature	-55°C to +150°C
Voltage on any Pin with Respect to $V_{SS}$ (Note 1)	-0.3V to $V_{DD} + 0.3V$
Voltage on $V_{DD}$ with Respect to $V_{SS}$	-0.3V to +6.5V
Power Dissipation (Note 5)	300mW

**Standard Conditions** (unless otherwise stated):

**DC CHARACTERISTICS**

Operating Temperature  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$

\* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Supply Voltage	$V_{DD}$	2.5	—	6.0	V	
Supply Current	$I_{DD}$	—	—	2 5	mA mA	$V_{DD} = 4V$ $V_{DD} = 6V$ } All I/O pins tri-state, $t_{CY} = 4 \mu\text{sec}$
Input Low Voltage	$V_{IL}$	$V_{SS}$	—	$0.2V_{DD}$	V	
Input High Voltage	$V_{IH}$	$0.8V_{DD}$	—	—	V	
Output High Voltage (RB0-7, RC0-7)	$V_{OH}$	$V_{DD} - 0.4$ $V_{DD} - 0.4$	—	—	V V	$I_{SOURCE} = 0.2\text{mA}$ , $V_{DD} = 4.75V$ $I_{SOURCE} = 80\mu\text{A}$ , $V_{DD} = 2.5V$
Output Low Voltage (RB0-7, RC0-7) (Note 1)	$V_{OL}$	—	—	0.4	V	$I_{SINK} = 0.2\text{mA}$ , $V_{DD} = 2.5V$ $I_{SINK} = 1.6\text{mA}$ , $V_{DD} = 4.75V$
Input Low Current (RA0-3, RC0-7) (Note 2)	$I_{IL}$	—	—	250	$\mu\text{A}$	$V_{DD} = 6V$ , $V_{IN} = 0.4V$
Input High Current (RA0-3, RC0-7) (Note 2)	$I_{IH}$	2	—	—	$\mu\text{A}$	$V_{IN} = V_{DD} - 0.4V$
Leakage Current (Note 3)	$I_{LC}$	-1	—	1	$\mu\text{A}$	$V_{SS} \leq V_{PIN} \leq V_{DD}$

†Typical data is at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.0V$ .

**NOTES:**

- The output pull-down transistor can be removed via a mask option to facilitate interfacing with external circuitry which has signal swings below  $V_{SS}$ . If this is the case, the maximum voltage permitted to be applied to the pin is -12V with respect to  $V_{DD}$ .
- Current is being sourced by the internal pull-up resistors which are available as a mask option on ports RA0-3 and RC0-7. (RC0-7 have their pull-ups turned off when selected as outputs.)
- This applies to ports RA0-3 and RC0-7 without the mask optional internal pull-up resistors, port RB0-7 and RC0-7 in the high impedance state,  $\overline{RTCC}$ ,  $\overline{MCLR}$  and OSC 1.
- Total output sink current for all output pins (including CLK OUT) must not exceed 50mA. Total output source current must not exceed 20mA. Maximum output sink or source current for each individual output must not exceed 10mA.
- Total power dissipation should not exceed 300mW for the package. Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} [I_{DD} - \sum (I_{IN} + I_{OH})] + \sum (V_{DD} - V_{IN}) (I_{IN}) + \sum (V_{DD} - V_{OH}) (I_{OH}) + \sum (V_{OL}) (I_{OL})$$



**Standard Conditions** (unless otherwise stated):

**AC CHARACTERISTICS**

Operating Temperature  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 2.5 - 6.0\text{V}$  except as noted.

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Oscillator Frequency	$f_{OSC}$	25	—	1000	KHz	$V_{DD} = 2.5\text{V}$
	$f_{OSC}$	25	—	1250	kHz	$V_{DD} = 3.2\text{V}$
	$f_{OSC}$	25	—	1650	kHz	$V_{DD} = 5.0\text{V}$
	$f_{OSC}$	25	—	1800	kHz	$V_{DD} = 6.0\text{V}$
<b>CLOCK OUT</b>						
Period (Instruction Cycle Time)	$t_{CY}$	—	$5/f_{OSC}$	—	$\mu\text{s}$	(Note 1)
Pulse Width	$t_{CLKH}$	—	$1/f_{OSC}$	—	$\mu\text{s}$	
Rise/Fall Time	$t_r/t_f$	—	—	200	ns	1 TTL Load + 60pF $V_{DD} = 5\text{V}$
<b>RTCC Input</b>						
Period	$t_{RT}$	$t_{CY} + 0.2\mu\text{s}$	—	—	—	(Notes 2 and 3)
Pulse Width (High or Low Level)	$t_{pw}$	500	—	—	ns	
<b>I/O Ports</b>						
Data Input Setup Time	$t_s$	—	—	$1/5 t_{CY} - 300$	ns	
Data Input Hold Time	$t_h$	0	—	—	ns	
Data Output Propagation Delay	$t_{pd}$	—	—	1.6	$\mu\text{s}$	60pF + 2.2K to $0.8V_{DD}$

†Typical data is at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$

**NOTES:**

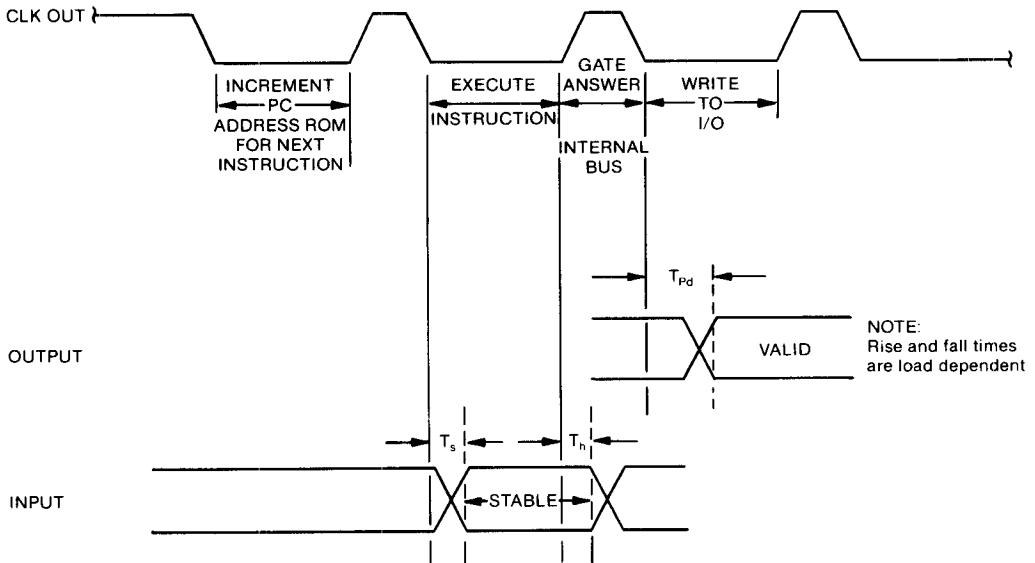
1. Instruction cycle period ( $t_{CY}$ ) equals five times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the  $\overline{\text{RTCC}}$  input, CLK OUT may be directly tied to the  $\overline{\text{RTCC}}$  input.
3. The maximum frequency which may be input to the  $\overline{\text{RTCC}}$  pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT(min)}} = \frac{1}{t_{CY(min)} + 0.2\mu\text{s}}$$

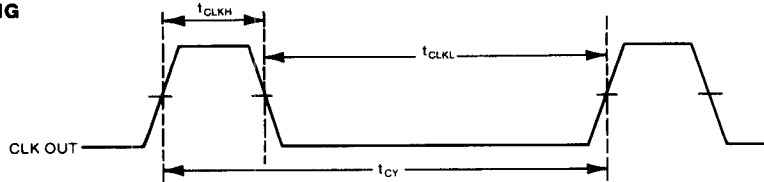
For example:

$$\text{if } t_{CY} = 4\mu\text{s}, f_{(max)} = \frac{1}{4.2\mu\text{s}} = 238\text{KHz.}$$

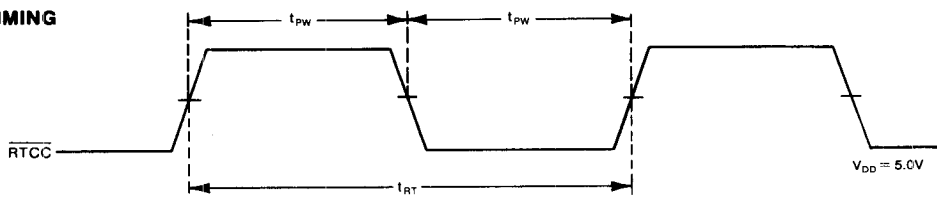
I/O TIMING



CLK OUT TIMING



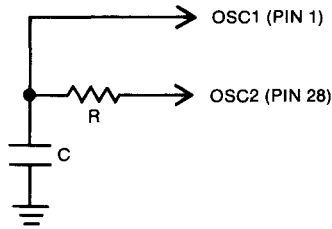
RTCC TIMING



MICROCOMPUTER

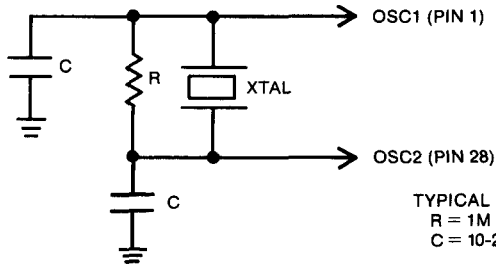
PIC16C55 OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION



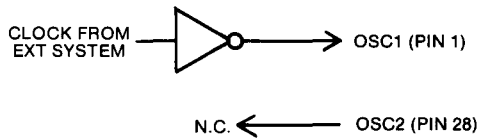
$10K \leq R \leq 1M$ .  
 TYPICAL VALUES  
 $R \geq 10K$   
 $C \geq 100pf$

CRYSTAL INPUT OPERATION



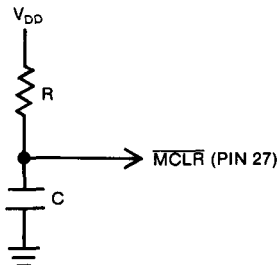
TYPICAL VALUES  
 $R = 1M$   
 $C = 10-20pF$

EXTERNAL CLOCK INPUT OPERATION



MICROCOMPUTER

MASTER CLEAR



TYPICAL VALUES  
 $R = 1M$   
 $C = 0.1\mu F$

Master Clear may require up to a 75ms delay before activation after power is applied to the  $V_{DD}$  pin for a 1MHz crystal to start up. To achieve this an external RC configuration as shown can be used (assuming  $V_{DD}$  is applied as a step function). The RC oscillator option, shown above, should start up in less time.