Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz for PIC1650A and PIC1655A (4MHz for PIC1656) the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1 f f f f f (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1 f f f f f (0140)	Clear f	CLRF	f	0→f	Z
000 010 d f f f f f (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 d f f f f f (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 d f f f f f (0400)	Inclusive OR W and f	IORWF	f, d	WVf→d	Z
000 101 d f f f f f (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 d f f f f f (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 d f f f f f (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 d f f f f f (1000)	Move f	MOVF	f, d	f→d	Z
001 001 d f f f f f (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 d f f f f f (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 d f f f f f (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 d f f f f f (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 d f f f f f (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 d f f f f f (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇆f(4-7)→d	None
001 111 d f f f f f (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb b f f f f f (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb b f f f f f (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb b f f f f f (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb b f f f f f (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 010 (0002)	Return from Interrupt	RETURN	—	Stack→PC	None
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	kVW→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377_8. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

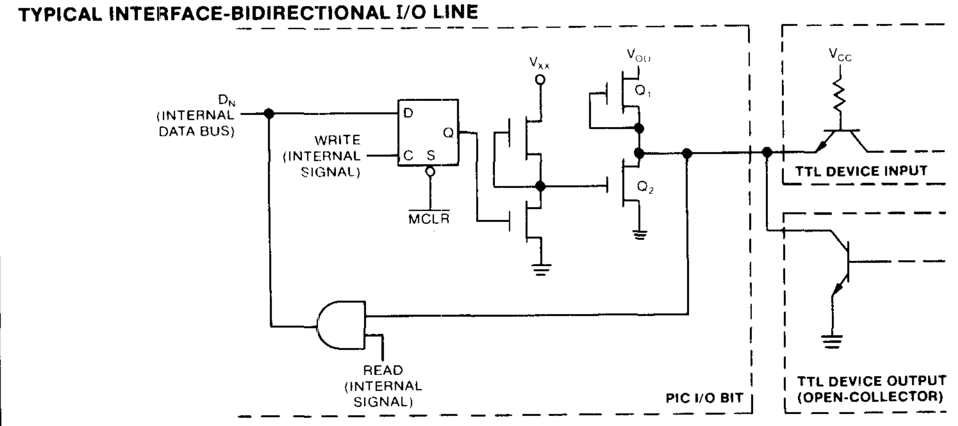
Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

MICROCOMPUTER

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

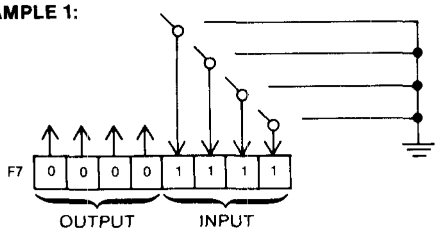
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. *Any input must be present until read by an input instruction.* The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



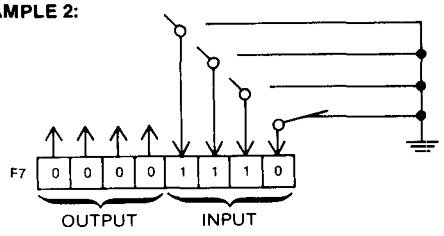
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature Under Bias	125°C
Storage Temperature	−55°C to +150°C
Voltage on any Pin with Respect to V_{SS}	−0.3V to +10.0V
Power Dissipation	1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS/PIC1664

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	All I/O pins @ V_{DD}
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RT}$ & OSC1)	V_{IH}	2.4	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RT}$ & OSC1 in PIC1650A/55A mode)	V_{ILH}	V_{DD}−1	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	$I_{OH} = -100\mu A$ (Note 4)
		3.5	—	V_{DD}	V	$I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	$I_{OL} = 1.6mA$, $V_{XX} = 4.5V$
		—	—	0.90	V	$I_{OL} = 5.0mA$, $V_{XX} = 4.5V$
		—	—	0.90	V	$I_{OL} = 5.0mA$, $V_{XX} = 8.0V$
		—	—	1.20	V	$I_{OL} = 10.0mA$, $V_{XX} = 8.0V$
		—	—	2.0	V	$I_{OL} = 20.0mA$, $V_{XX} = 8.0V$ (Note 5)
Output Low Voltage A0-A8 CLK OUT HALT ACK	V_{OL2}	—	—	0.45	V	$I_{OL} = 1.6mA$ (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{DD}$ (note 6)
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	$V_{IL} = 0.4V$ internal pullup
Input High Current (all I/O ports)	I_{IH1}	−0.1	−0.4	−1.4	mA	$V_{IH} = 2.4V$
Input High Current (HALT)	I_{IH2}	—	50	200	μA	$V_{IH} = 2.4V$ internal pulldown
OSC Input (PIC1650/55 MODE) External Input Impedance High	R_{OSCH}	120	800	3500	Ω	$V_{OSC} = V_{DD} = 5V$. (Applies to external OSC drive only.)
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	$V_{OSC} = 0.4V$
OSC Input (PIC1656 MODE) OSC1 External Input Low Voltage	V_{IL} (OSC1)	−0.2	—	0.8	V	
OSC1 External Input High Voltage	V_{IH} (OSC1)	V_{DD}−1	—	—	V	

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. Also applies to OSC1 pin in PIC1656 mode.

Standard Conditions (unless otherwise stated):
AC CHARACTERISTICS
Operating Temperature $T_A = 0°C$ to $+70°C$

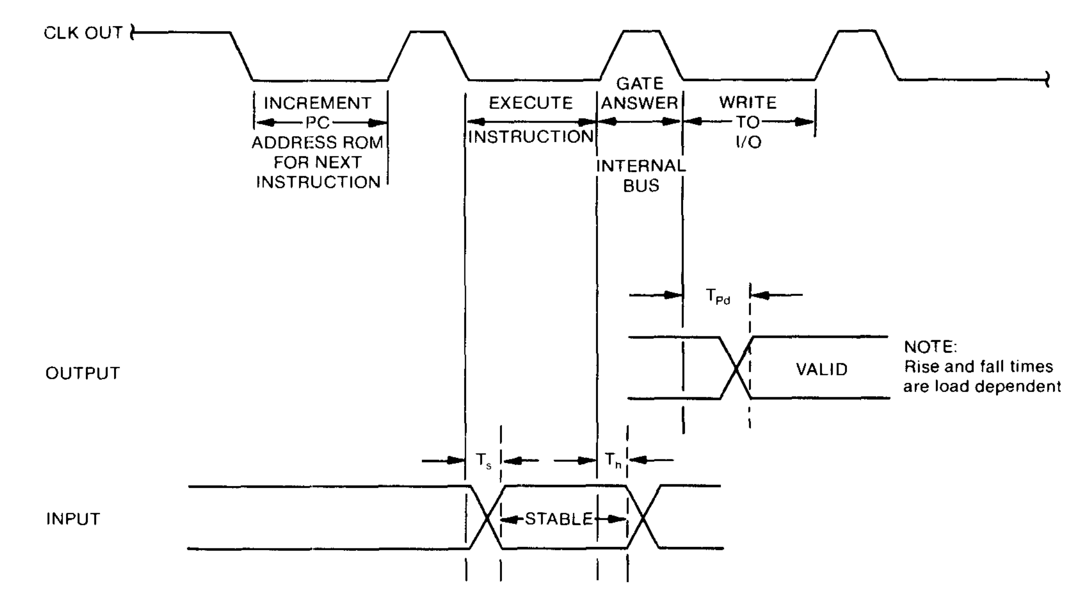
Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz — 1.0MHz external time base 1650A/1655A mode 0.8MHz —4.0MHz external time base 1656 mode (Note 1)
RT Input						
Period	t_{RT}	t_{CY}+0.2μs	—	—	—	
High Pulse Width	t_{RTH}	½t_{RT}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{RT}	—	—	—	(Notes 2 and 3)
I/O Ports						
Data Input Setup Time	t_S	—	—	¼t_{CY}—125	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	600	1000	ns	Capacitive load = 50pF
HALT ACK Output Propogation Delay	t_{HA}	—	200	—	ns	
A_0-A_8 Output Propogation Delay	t_{AD}	—	350	—	ns	
D_0-D_{11} Input Set-up Time	t_{DS}	0	—	—	ns	
D_0-D_{11} Input Hold Time	t_{DH}	200	—	—	ns	

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

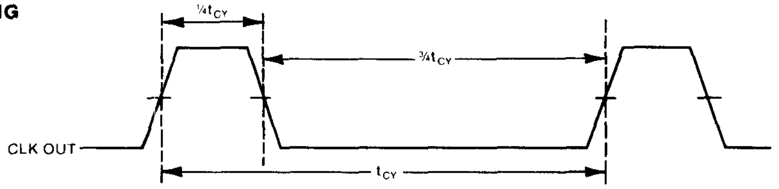
NOTES:
1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period for 1650A/1656A operation or sixteen times oscillator time base period for 1656 operation.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the RTCC input, CLK OUT may be directly tied to the $\overline{RT}/\overline{RTCC}$ input without any loss of counts.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows:
$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$
For example:
if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

MICROCOMPUTER

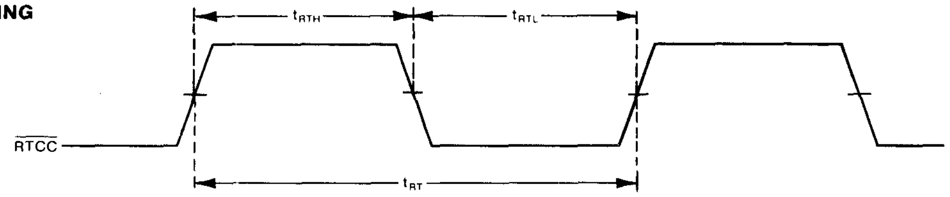
I/O TIMING



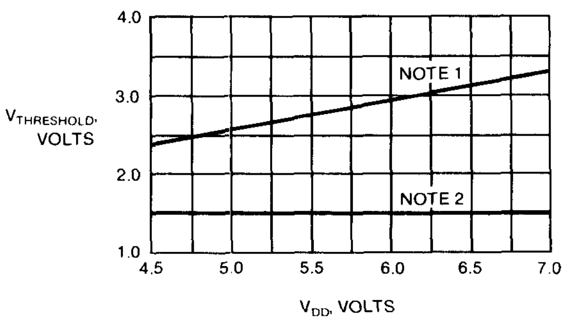
CLK OUT TIMING



$\overline{RT}$ TIMING



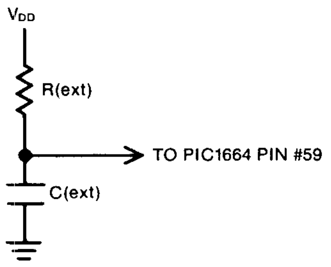
SCHMITT TRIGGER CHARACTERISTICS ($\overline{RTCC}$, $\overline{MCLR}$ and OSC PINS) $T_A = 25°C$ (TYPICAL)

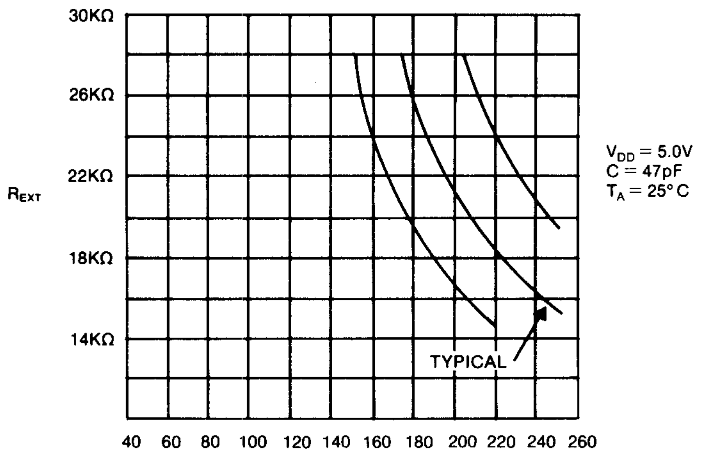


NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

PIC1664 OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION

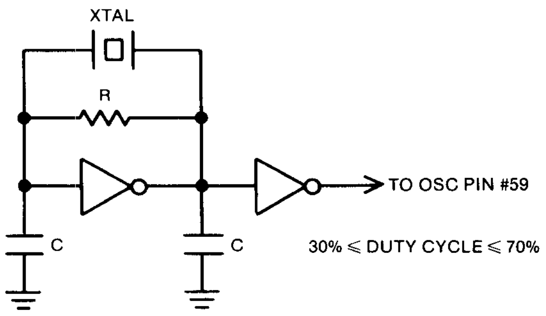




INSTRUCTION CYCLE TIME (kHz)
Oscillator Frequency With Typical Unit To Unit Variance

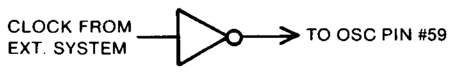
Unit to Unit Variation at $V_{DD} = 5.0V$, $T_A = 25°C$ is ±25%
Variation from $V_{DD} = 4.5V - 7.0V$ referenced to 5V is −3%, +9%
Variation from $T_A = 0°C - 70°C$ referenced to 25°C is +3%, −5%

BUFFERED CRYSTAL INPUT OPERATION



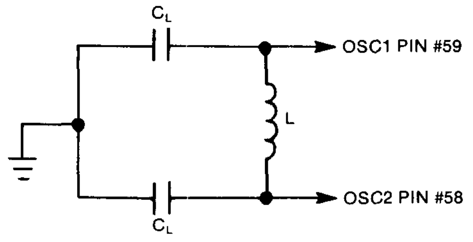
The buffer must be capable of driving 120Ω, min. (800Ω, typ.) to 2.0V. However, it is recommended that the pull-down transistor on the OSC pin be removed (an option) if OSC is to be driven externally.

EXTERNAL CLOCK INPUT OPERATION



PIC1664 OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

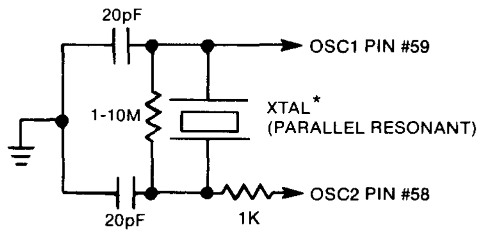
LC INPUT OPERATION



$$f_{OSC} \approx \frac{1}{2\pi\sqrt{L\,(C_L + C_{INT})}},$$
where $C_{INT} = 10pF$.

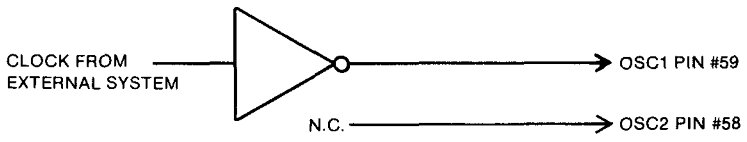
Typical values for 4MHz operation:
$L = 70\mu H$
$C_L = 10pF$

CRYSTAL INPUT OPERATION

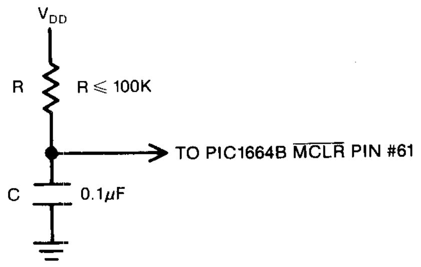


* or ceramic resonator

EXTERNAL CLOCK INPUT OPERATION

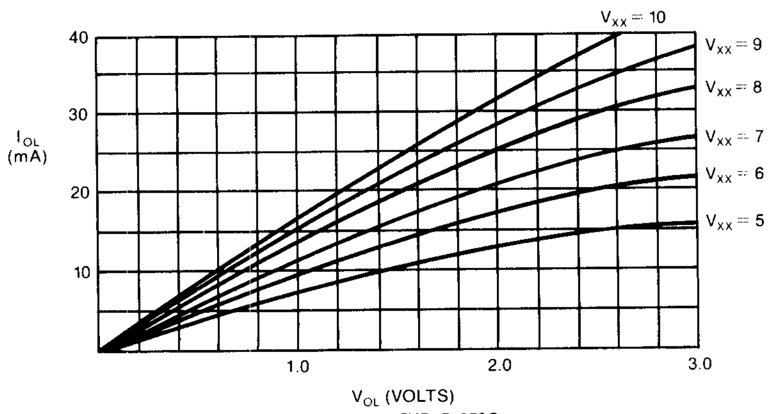


MASTER CLEAR (TYPICAL CIRCUIT)



Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin, for the oscillator to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

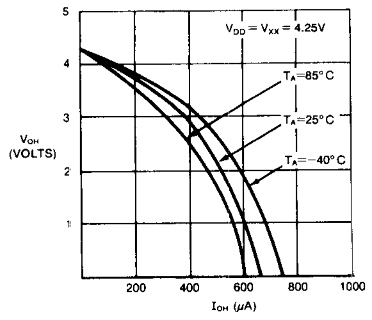
OUTPUT SINK CURRENT GRAPH



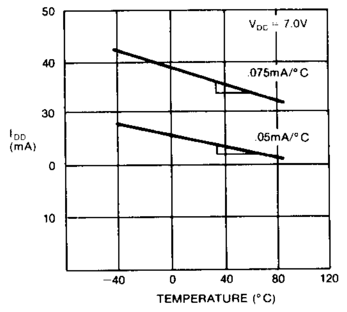
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

V_{OH} VS I_{OH} (I/O PORTS) (TYPICAL)



POWER SUPPLY CURRENT VS TEMPERATURE (TYPICAL LIMITS)



PIC1650A/PIC1655A EMULATION CAUTIONS

When emulating a PIC1650A or PIC1655A using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1650A/PIC16655A mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{\text{MCLR}}$ to force all I/O registers high.
2. The OSC1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the PIC1650A and the 28 pin socket for the PIC1655A module plugs.

E. Make sure that during an actual application that the $\overline{\text{MCLR}}$ input swings from a low to high level a minimum of 1 msec after the supply voltage is applied.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1664.

G. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1650A and PIC1655A.

PIC1656 EMULATION CAUTIONS

When emulating a PIC1656 using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1656 mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a low state.

1. This causes the $\overline{\text{MCLR}}$ to force F5 register high and F6 and F7 low.
2. The OSC1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes enabled and the $\overline{\text{RT}}$ always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are used for interrupt servicing.

B. All three levels of stack can be used within the program. If interrupts are used, allow one level of the stack for interrupt servicing.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application that the $\overline{\text{MCLR}}$ input swings from a low to high level a minimum of 1 msec after the supply voltage is applied.

F. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1656.

8 Bit Development Microcomputer

FEATURES

- PIC microcomputer with ROM removed
- Useful for engineering prototyping of PIC applications
- PIC ROM address & data lines brought out to pins
- HALT pin for single stepping or stopping program execution
- MODE pin for selection of PIC1650A/1655A or PIC1656 emulation
- User programmable via external memory
- 32 8-bit RAM registers
- Arithmetic Logic Unit
- User defined TTL-compatible Input and Output lines
- Real Time Clock/Counter
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)

DESCRIPTION

The PIC1664 development microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit on a single chip.

The PIC1664 MOS/LSI is functionally identical to the PIC microcomputers except that the ROM is removed and the ROM address and data lines are brought out, requiring a 64-pin package. The addition of a HALT pin gives the user the ability to stop as well as single-step the chip. The logic level applied to a MODE pin determines whether the PIC1664 emulates a PIC1650A/1655A or a PIC1656.

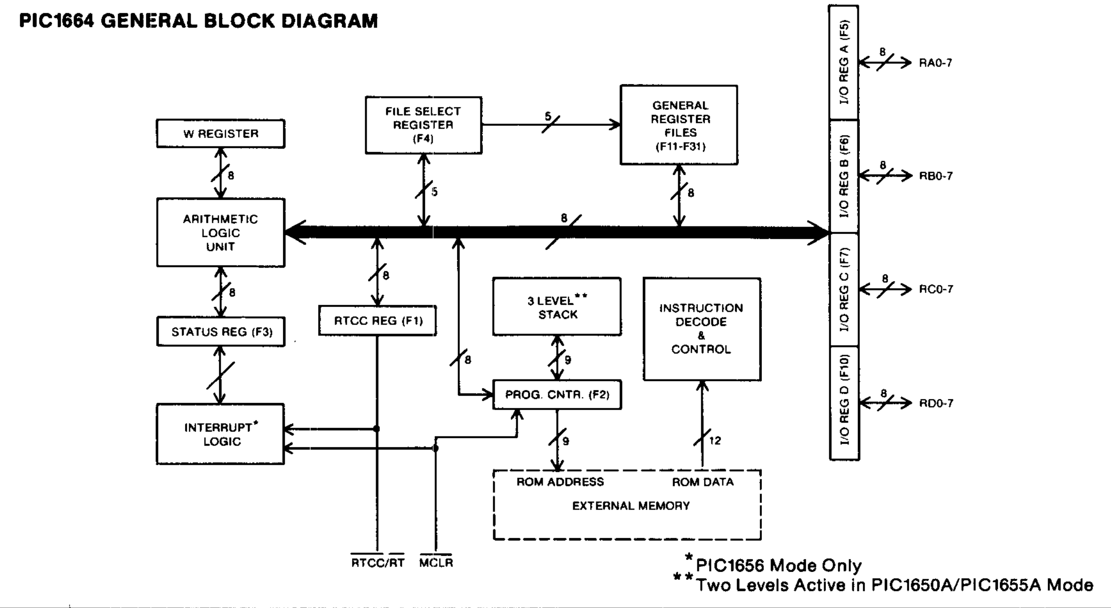
The external ROM can contain a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications.

The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC Series is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Application notes and sample programs are used to develop programs which can then be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PFD Field Demo Systems are available containing a PIC1664 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with stand-alone emulation and debugging operation or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM.

PIC1664 GENERAL BLOCK DIAGRAM



*PIC1656 Mode Only
**Two Levels Active in PIC1650A/PIC1655A Mode

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1664 microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC1664 is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined external ROM composed of 512 program words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general register. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the MCLR input on power up initializes the external ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
MODE (Input)	Mode input. Used to set the PIC1664 to emulate the PIC1650A/PIC1655A (logic "one") or the PIC1656 (logic "zero"). The mode must be selected before $\overline{\text{MCLR}}$ is brought high.
OSC1 (Input) **OSC2 (output)**	Oscillator pins. When the MODE switch selects PIC1650A/1655A operation OSC1 becomes a single input clock using either RC control or a buffered crystal. When the PIC1664 is in the PIC1656 mode both OSC1 and OSC2 are used as a two input clock using either crystal, ceramic resonator or LC network.
$\overline{\text{RT}}$ (Input)	Real Time Clock input. This pin increments the Real Time Clock Counter Register 1 on high to low transitions applied to this input. This pin has different modes of operation depending on the MODE input as well as the contents of F3, the Status Register. In PIC1650A/1655A mode this pin emulates the $\overline{\text{RTCC}}$ pin. In the PIC1656 mode this pin emulates the $\overline{\text{RT}}$ pin.
RA0-7, RB0-7, RC0-7, RD0-7 (Input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program. During emulation of the PIC1655A or PIC1656, Register D will become internal general purpose File Register 10; I/O lines RD0-7 will be undefined and must be left unconnected.
$\overline{\text{MCLR}}$ (Input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O registers high (for PIC1650A/1655A) or I/O registers F6 and F7 low and F5 high (for PIC1656). Also clears bits 3-7 of status register (F3) (for PIC1656). This pin should be held low at least 1-10ms after the power supply is valid for the oscillator to start up. $\overline{\text{MCLR}}$ has no internal pullup resistor.
V_{DD}	Primary Power supply input.
V_{XX}	Output buffer power supply input. Used to increase current sinking capability when emulating the PIC1650A and PIC1655A. When emulating the PIC1656 this pin must be connected to V_{DD}.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing. The OSC frequency is divided by 4 for PIC1650A/1655A mode or by 16 for the PIC1656 mode.
HALT (Input)	Halt. When high this input suspends execution of the next instruction. No data is lost and after HALT is brought low execution proceeds exactly as if no HALT signal had been applied.
HALT ACK (output)	Halt Acknowledge. This output is high when the PIC1664 is halted either due to an active HALT input or execution of the HALT instruction (0001_8). In the first case HALT ACK is brought back low when the PIC1664 begins execution when the HALT input is brought low; and in the second case it is brought low using $\overline{\text{MCLR}}$ or by first raising and then lowering the HALT input.
D0-D11 (Input)	Data Input. These twelve lines accept twelve bit PIC instruction codes generated by an external source D0 is the LSB of the instruction.
A0-A8 (output)	Address Output. These nine lines represent the address of the next instruction to be executed by the PIC1664. A0 is the LSB of the address.

MODE PIN OPERATION

The mode pin is used to select either PIC1650A/1655A emulation or PIC1656 emulation.

With the MODE pin set high, the PIC1664 is set to emulate the PIC1650A/1655A. Specifically:

1. $\overline{\text{MCLR}}$ will force all I/O registers high.
2. OSC1 becomes a single clock input. The PIC1664 will execute instructions at one fourth the OSC frequency.
3. The interrupt system is disabled and the RTCC always counts on trailing edges.
4. Bits 3-7 of F3 are ones.

When the MODE input is low, the PIC1664 will emulate the PIC1656 circuit. Specifically:

1. MCLR will force I/O registers F6 and F7 low and F5 high.
2. OSC1 and OSC2 become a two input clock supporting crystals, ceramic resonators, or RC networks. The PIC1664 will execute instructions at one sixteenth the OSC frequency.
3. The interrupt system is connected and the interrupt/RTCC operation is as described in the PIC1656 data sheet.
4. Bits 3-7 of F3 are used for interrupt service.

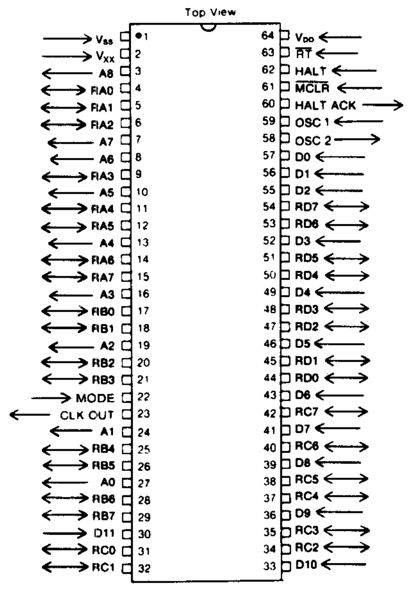
To insure proper chip operation, the Mode pin should be preset before $\overline{\text{MCLR}}$ is brought high at initialization. "Dynamic-type" switching of this pin during processor operation will result in undefined conditions and must be avoided.

PROGRAMMING CAUTIONS

The PIC1664 is designed as a development circuit for emulating the operation of the PIC1650A, PIC1655A and PIC1656. While all circuits in the PIC series have the same basic architecture and instruction set, there are differences which require attention on the part of the user to insure that all conditions are met for proper operation of the PIC1664 with respect to the target PIC circuit (either PIC1650A, PIC1655A, or PIC1656). The following check-list should be used to achieve proper emulation.

1. The MODE pin must be properly set (high for PIC1650A/PIC1655A or low for PIC1656).
2. With the MODE pin high OSC1 is a single clock input. A low on the MODE pin enables the two input clock.
3. For PIC1650A and PIC1655A emulation, bits 3-7 of F3 (the status register) should be considered undefined.
4. For PIC1655A and PIC1656 emulation bits 4-7 of F5 (the input only file) should be tied to V_{SS} (ground) as these bits are always read as low inputs.
5. For PIC1655A and PIC1656 emulation the pins corresponding to $F10_8$ (I/O port RD on the PIC1650A) should be left unconnected. In this way $F10_8$ will operate as an internal register as is appropriate for the PIC1655A and PIC1656.
6. The I/O Programming Caution on page 3-11 describing the I/O variations between the PIC1650A and the PIC1655A/PIC1656 must be carefully followed. The PIC1664 contains all bidirectional input/output ports as required for PIC1650A emulation. The I/O structure variation used in PIC1655A and PIC1656 require careful adherence to the cautions listed in the following pages.
7. The RETURN (0002_8) instruction is not supported by the PIC1650A and PIC1655A and should not be used when emulating these parts. The HALT instruction (0001_8) is not recognized by any PIC circuit other than the PIC1664.
8. For PIC1656 emulation the V_{XX} pin must be tied directly to V_{DD} as there is no V_{XX} pin on the PIC1656.

PIN CONFIGURATION
64 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to the contents of W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RT}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
CNT	RTCR	IR	RTCE	IE	Z	DC	C

BIT 0: Carry (C) bit	For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant. For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.
BIT 1: Digit Carry (DC) bit	For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.
BIT 2: Zero (Z) bit	Set if the result of an arithmetic operation is zero.
BITS: 3-7	Interrupt Service Flags (Cleared on $\overline{MCLR}$). BIT 3: Interrupt Enable (IE) status bit. When set to a one, this bit enables the external interrupt to occur when and if the interrupt request (IR) status bit (bit 5) is also set. When reset to a zero, the external interrupt is disabled. BIT 4: Real Time Clock Enable (RTCE) status bit. When set to a one, this bit enables the real-time clock/counter interrupt to occur when and if the real-time clock interrupt request (RTCR) status bit (bit 6) is also set. When reset to a zero, the interrupt is disabled. BIT 5: Interrupt Request (IR) status bit. This bit is set by a high-to-low transition on the $\overline{RT}$ pin, generating an interrupt request. If and when the interrupt enable (IE) bit (bit 3) is also set, an interrupt will occur. This causes the current PC address to be pushed onto the stack and the processor to execute the instruction at location 760_8. The IR bit is then immediately cleared. Note that the IR bit can be set regardless of the state of the IE bit, thus requesting an interrupt which can be serviced or not at the programmer's option. BIT 6: Real Time Clock/Counter Interrupt Request (RTCR) status bit. This bit is set when the RTCC register (File 1) transitions from a full count (377_8) to a zero count (000_8). If and when the RTCE bit is also set, an interrupt will occur. This causes the current PC address to be pushed onto the stack and the processor to execute the instruction at location 740_8. The RTCR bit is then immediately cleared. Note that the RTCR bit can be set regardless of the state of the RTCE bit, thus requesting an interrupt which can be serviced or not, at the programmer's option. NOTE: Although the processor cannot be interrupted during an interrupt (i.e., until the RETFI instruction is executed), (an) other interrupt(s) can be requested (status bits 5 and/or 6 can be set). This will cause the processor to reinterrupt immediately upon its return from the current interrupt assuming the interrupt(s) is (are) enabled. (Pending external interrupts have priority over pending real-time clock/counter interrupts.) BIT 7: Count Select (CNT) status bit. When CNT bit is set to a one, the RTCC register will increment on each high-to-low transition at the $\overline{RT}$ pin. If the CNT bit is sent to a zero, the RTCC register will increment at the internal clock rate (1/16 of the frequency at the OSC pins).

File (Octal)	Function
F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3). A4-A7 defined as zeroes.
F6	Output Register B (B0-B7)
F7	I/O Register (C0-C7)
F10-F37	General Purpose Registers