8 Bit Microcomputer

FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70° C and −40° to 85° C
- 4 sets of 8 user defined TTL-compatible Input/Output lines
- 2 level stack for subroutine nesting

DESCRIPTION

The PIC1650A microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

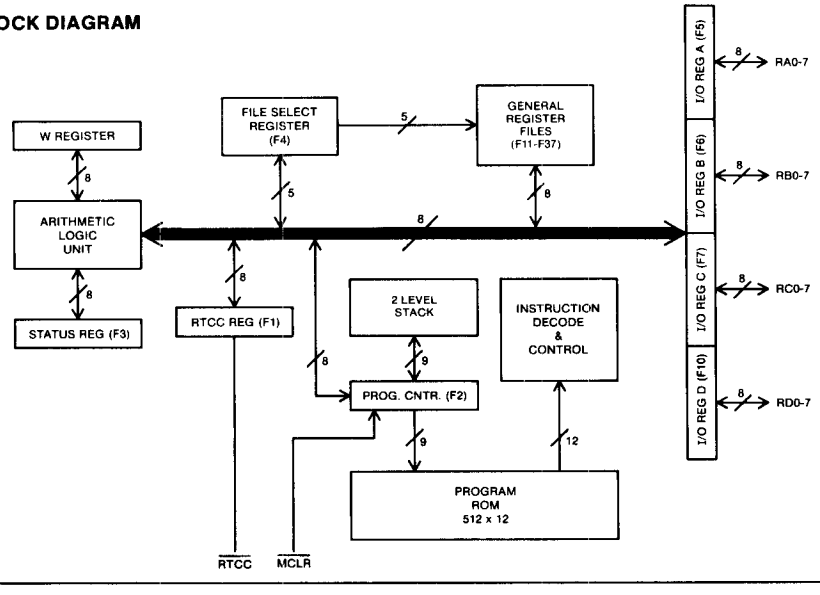
The PIC1650A is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664. The PIC1664 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD1000 Field Demo System is available containing a PIC1664 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

MICROCOMPUTER

PIC1650A BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

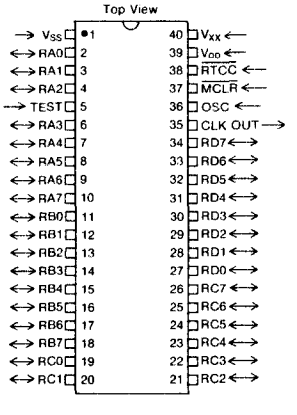
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
$\overline{RTCC}$ (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The RTCC register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O register high. Should be held low at least 1-10ms past the time when the power supply is valid for the oscillator to start up. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power. Used to enhance output current sinking capability.
V_{SS}	Ground

PIN CONFIGURATION
40 LEAD DUAL IN LINE



MICROCOMPUTER

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A7)
F6	I/O Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10	I/O Register D (D0-D7)
F11-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

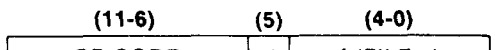
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

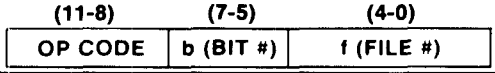
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

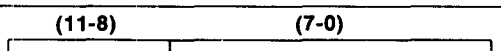
Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇌f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

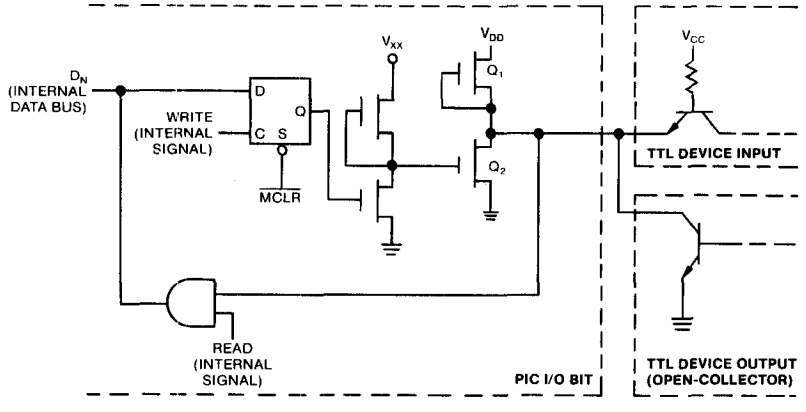
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	 Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	 Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	 Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	 Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	 Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	 —
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	 —
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	 —
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	 —
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	 —
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	 —

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

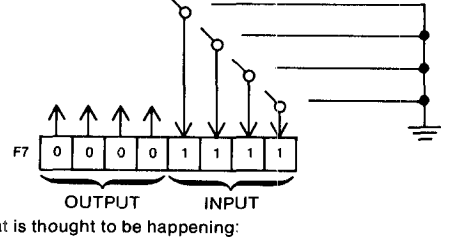
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



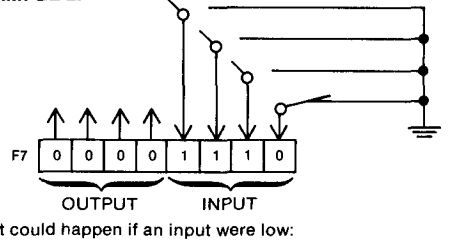
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +10.0V
Power Dissipation 1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS/PIC1650A

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	All I/O pins @ V_{DD}
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD}−1	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4 3.5	— —	V_{DD} V_{DD}	V V	I_{OH} = −100μA (Note 4) I_{OH} = 0
Output Low Voltage (I/O only)	V_{OL1}	— — — — —	— — — — —	0.45 0.90 0.90 1.20 2.0	V V V V V	I_{OL} = 1.6mA, V_{XX} = 4.5V I_{OL} = 5.0mA, V_{XX} = 4.5V I_{OL} = 5.0mA, V_{XX} = 8.0V I_{OL} = 10.0mA, V_{XX} = 8.0V I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.4	mA	V_{IH} = 2.4V

†Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

DC CHARACTERISTICS/PIC1650AI

Operating Temperature $T_A = -40°C$ to $+85°C$

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	60	mA	All I/O pins @ V_{DD}
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.7	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD}−1	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	$I_{OH} = -100\mu A$ (Note 4) $I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL1}	— — — — —	— — — — —	0.45 0.90 0.90 1.20 2.0	V V V V V	$I_{OL} = 1.6mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 10.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 20.0mA$, $V_{XX} = 8.0V$ (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	$I_{OL} = 1.6mA$ (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.8	mA	$V_{IL} = 0.4V$ internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.8	mA	$V_{IH} = 2.4V$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS/PIC1650A, PIC1650AI

Operating Temperature $T_A = 0°C$ to $+70°C$ (PIC1650A), $T_A = -40°C$ to $+85°C$ (PIC1650AI)

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz — 1.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{RT}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{RT}$	—	—	—	(Notes 2 and 3)
I/O Ports						
Data Input Setup Time	t_S	—	—	$\frac{1}{4}t_{CY}-125$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	600	1000	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	120	800	3500	Ω	$V_{OSC} = 5V$ } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	$V_{OSC} = 0.4V$ } OSC drive only.

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the RTCC input, CLK OUT may be directly tied to the RTCC input.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows: $f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$

   For example: if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

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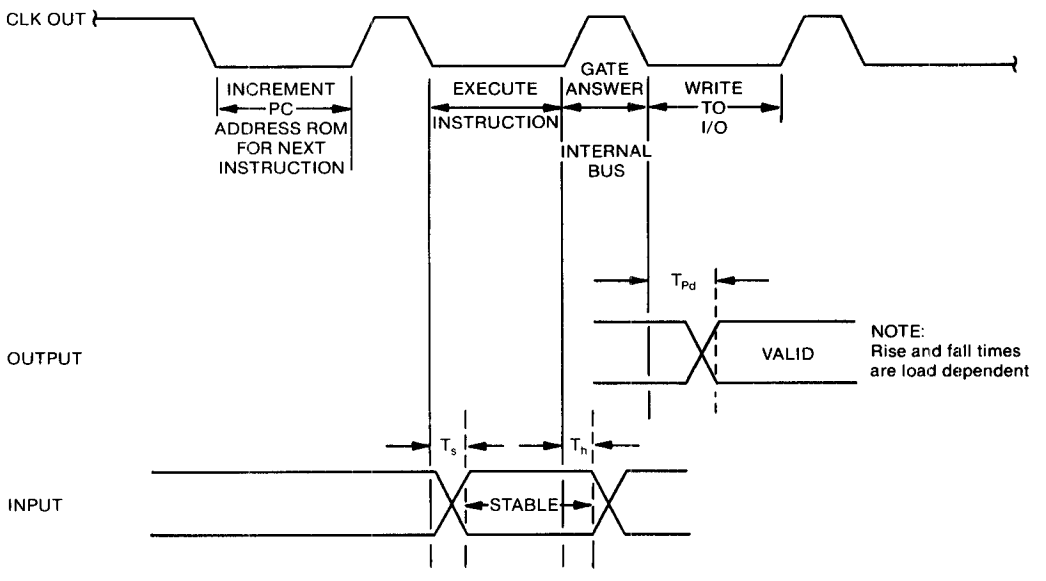
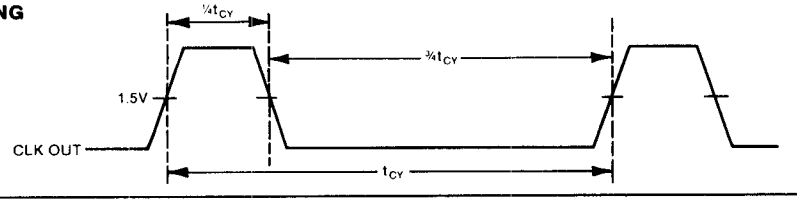
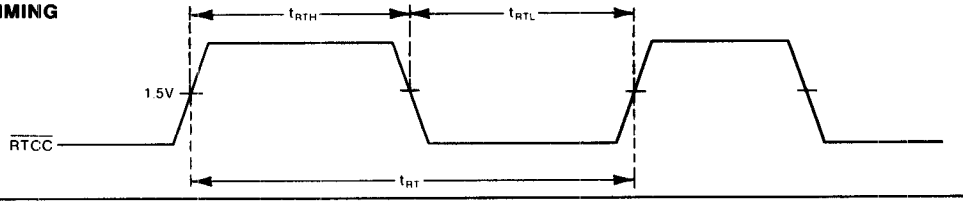
I/O TIMING



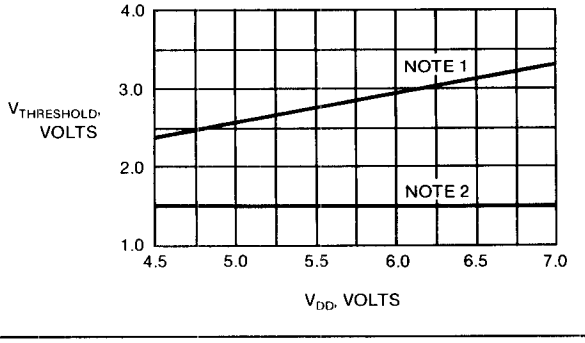
CLK OUT TIMING



$\overline{\text{RTCC}}$ TIMING



SCHMITT TRIGGER CHARACTERISTICS ($\overline{\text{RTCC}}$, $\overline{\text{MCLR}}$ and OSC PINS) T_A = 25°C (TYPICAL)



NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

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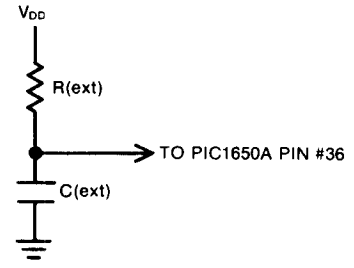
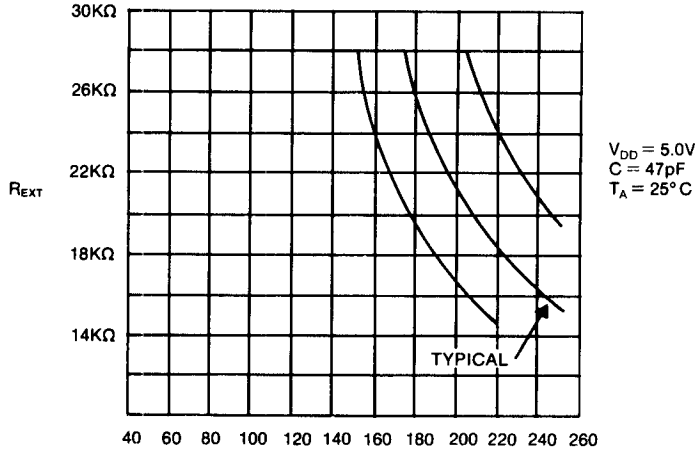
PIC1650A OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION

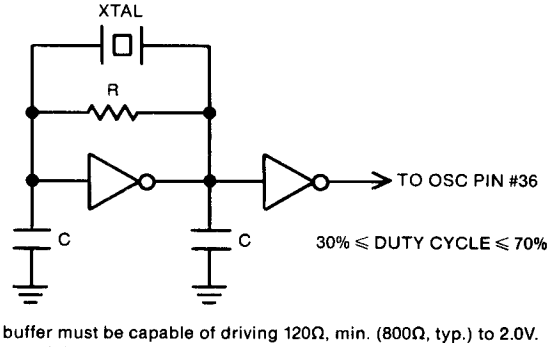




Oscillator Frequency With Typical Unit To Unit Variance

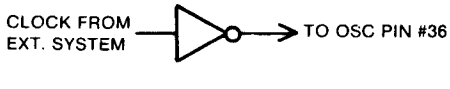
Unit to Unit Variation at V_{DD} = 5.0V, T_A = 25°C is ±25%
Variation from V_{DD} = 4.5V −7.0V referenced to 5V is −3%, +9%
Variation from T_A = 0°C −70°C referenced to 25°C is +3%, −5%

BUFFERED CRYSTAL INPUT OPERATION



The buffer must be capable of driving 120Ω, min. (800Ω, typ.) to 2.0V. However, it is recommended that the pull-down transistor on the OSC pin be removed (an option) if OSC is to be driven externally.

EXTERNAL CLOCK INPUT OPERATION



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EXTENDED TEMPERATURE RANGE

PIC series microcomputers are available in two temperature ranges. The preceding data sheets describe the commercial grade device, 0°C to 70°C centigrade. An industrial/automotive temperature range version is available. The −40° to 85° centigrade option is specified with the addition of a suffix, I, to the part number.

The specifications for these devices differ from their commercial grade counterparts in a few electrical parameters, typically interface voltage/current levels. Refer to the data sheets for details.

OPEN DRAIN OPTIONS

PIC1650A, PIC1670

Open-Drain I/O Ports

Any or all of the I/O lines may be specified by the customer to be open drain, that is, the internal pull-up device will be removed. This enables the outputs to be pulled up to +10.0V maximum with an external pull-up resistor, allowing easy interface to external devices requiring a logic one level greater than V_{DD} of the PIC. In the logic one state, the leakage current of the I/O port is ± 5μA, maximum.

The customer shall specify on the "PIC Series Order Form" the pin number and port name (e.g., "RB3") of each port required to be open drain.

PIC1655A, PIC1656

Open Drain I/O, Input and Output Ports

Any or all of the I/O, input only or output only lines may be specified by the customer to be open drain, that is, the internal pull-up device will be removed. This enables the outputs to be pulled up to +10.0V maximum with an external pull-up register, allowing easy interface to external devices requiring a logic one level greater than V_{DD} of the PIC. In the logic one state, the leakage current of the I/O port is ±5μA, maximum.

The customer shall specify on the "PIC Series Order Form" the pin number and port name (e.g., "RB3") of each port required to be open drain.

PIC16C55

Input-only, Output-only and I/O Ports

Any or all of the input-only and I/O lines may be specified to have an internal pull-up resistor inserted via a mask option. This allows easy interface to an external transistor or switch without the need for an external pull-up resistor. Furthermore, any or all of the output-only or I/O pull-down transistors can be specified to be removed via a mask option. This facilitates interfacing with external circuitry which has signal swings below V_{SS}. In this case the maximum voltage permitted to be applied to the pin is −12V with respect to V_{DD}.

PIC1654

Optional Internal Connection to RTCC

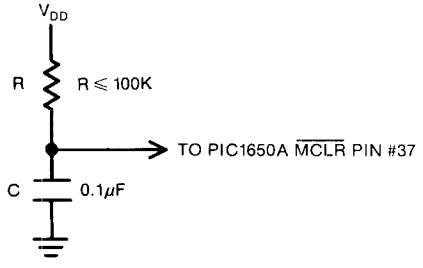
A mask option will allow an internal clock signal whose period is equal to the instruction execution time to drive the real time clock/counter register. In this mode, transitions in the $\overline{RTCC}$ pin will be disregarded.

PIC1655XT

Prescaler Division Ratio

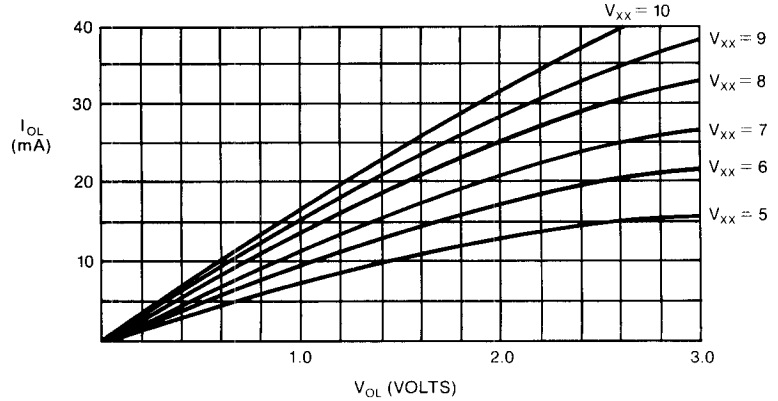
A mask option will allow the division ratio of the RTCC prescaler to be selected as 1, 2, 4, 8 or 16. Consult the data sheet for the details.

MASTER CLEAR (TYPICAL CIRCUIT)



Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin, for the oscillator to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

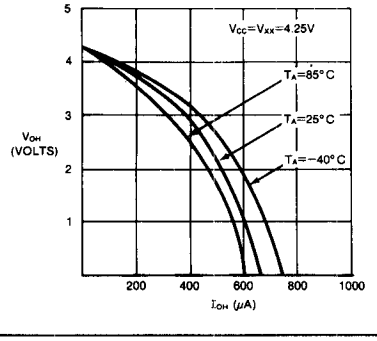
OUTPUT SINK CURRENT GRAPH



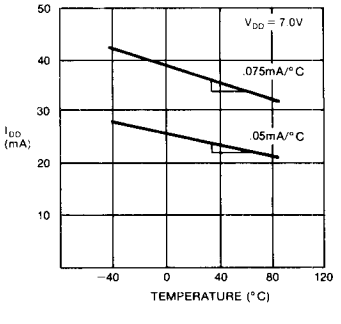
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

V_{OH} VS I_{OH} (I/O PORTS) (TYPICAL)



POWER SUPPLY CURRENT VS TEMPERATURE (TYPICAL LIMITS)



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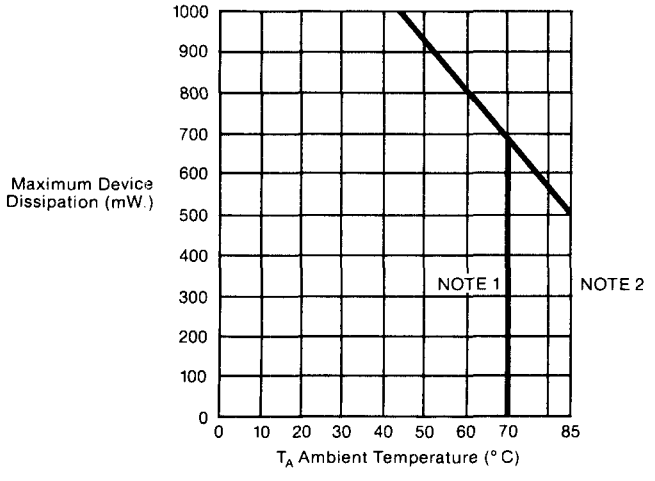
POWER DISSIPATION DERATING GRAPH



NOTES:
1. 70° C is the maximum operating temperature for standard parts.
2. 85° C is the maximum operating temperature for "I" suffix parts.

PIC1650A EMULATION CAUTIONS

When emulating a PIC1650A using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1650A mode. (Refer to PICES II Manual). The PIC1664B contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The OSC1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the module plug.

E. Make sure that during an actual application the $\overline{MCLR}$ input swings from a low to high level a minimum of 1msec after the supply voltage is applied to allow the oscillator to start up.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1664.

G. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1650A.

TELEVIEW Control Chip

FEATURES

- Interfaces user to Teleview system
- Initializes Teleview system
- PIC1650A-518 4 x 4 Keyboard, Teletext and Viewdata
- PIC1650A-519 4 x 4 Keyboard, Viewdata only, local programing of EAROM
- PIC1650A-532 ASCII or IR remote, Teletext and Viewdata
- PIC1650A-533 ASCII or IR remote, Viewdata only, local programing of EAROM

DESCRIPTION

The Teleview control chip PIC1650A interfaces the user to the Teleview system and generally organizes the operation of the system.

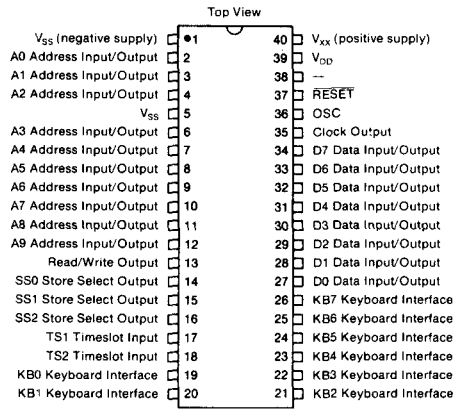
It is available in several versions each providing alternative user inputs and operating features.

Customized versions can be provided if required.

The features of the various versions are shown in the appendices.

PIN CONFIGURATION

Top View



PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Negative supply (Ground).
2-12	A0-A9	Address Input/Outputs which are connected to the Teleview Address Bus.
5	V_{SS}	Test pin — connect to V_{SS}.
13	Read/$\overline{\text{Write}}$	Control output connected to the Teleview R/W input.
14-16	SS0-SS2	Store Select outputs.
17, 18	TS1, TS2	Time Slot Inputs from Video Generator.
19-26	KB0-KB7	Keyboard Interface, may be Inputs, Outputs or Inputs/Outputs depending upon the version.
27-34	D0-D7	Data Inputs/Outputs which are connected to the Teleview Data Bus.
35	Clock Output	Not used except to check the Clock frequency (output frequency $f_X/4$).
36	Oscillator	Oscillator resistor and capacitor connected to this pin.
37	$\overline{\text{Reset}}$	Master reset input which must be kept at ground potential until the V_{DD} power is within specification.
38		Not used.
39	V_{DD}	Positive power supplies +5V Nom.
40	V_{XX}	

VIDEO

ELECTRICAL CHARACTERISTICS

(See PIC1650A Data Sheet for full specification).

Maximum Ratings*

Voltage on any pin with Respect to V_{SS} pin ..... −0.3V to +15V
Ambient Operating Temperature Range..... 0° C to +70° C
Storage Temperature Range ..... −55° C to +150° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

$V_{SS} = 0V$
$V_{DD} = +5V \pm 10\%$
$V_{XX} = +5V \pm 10\%$
$F_{clock} = 1MHz$
$T_A = 0° C$ to $+70° C$

Characteristic	Min	Typ	Max	Units	Conditions
Clock Frequency	0.8	—	1	MHz	
Input Low Voltage	−0.2	—	0.8	V	
Input High Voltage	2.4	—	—	V	
Input High Voltage ($\overline{\text{Reset}}$)	$V_{DD}-1$	—	—	V	
Input Low Current	−200	—	−1600	μA	$V_{IL} = 0.4V$
Input High Current	−100	—	—	μA	$V_{IH} = 2.4V$
Input Leakage Current (Reset)	−10	—	10	μA	
Output Low Voltage	—	—	0.4	V	$I_{OL} = 1.6$ mA
Output High Voltage	2.4	—	—	V	$I_{OH} = -100\mu A$
Supply Current: I_{DD}	—	—	55	mA	
I_{XX}	—	—	5	—	

APPENDIX 1/PIC1650A-518

This version interfaces with a 4 x 4 keyboard and provides basic Teletext/Viewdata operation. It replaces pattern 514.

INPUT 4 x 4 matrix keyboard
POWER UP MODE Picture
POWER UP DISPLAY Teleview White
POWER UP PAGE XOO in Store 7
KEYBOARD INTERFACE

KB0 pin 19	Row Input/Output
KB1 pin 20	Row Input/Output
KB2 pin 21	Row Input/Output
KB3 pin 22	Row Input/Output
KB4 pin 23	Column Input/Output
KB5 pin 24	Column Input/Output
KB6 pin 25	Column Input/Output
KB7 pin 26	Column Input/Output

KEYBOARD CODES

KB0/KB4	7	KB2/KB4	1
KB0/KB5	8	KB2/KB5	2
KB0/KB6	9	KB2/KB6	3
KB0/KB7	Picture/Text	KB2/KB7	Reveal/Conceal
KB1/KB4	4	KB3/KB4	Page/*
KB1/KB5	5	KB3/KB5	0
KB1/KB6	6	KB3/KB6	Time/#
KB1/KB7	Update	KB3/KB7	Store Select

NOTES:

1. Details of the operating features are contained in the general Teleview documents.
2. Two double key operations are recognized:
   (a) Store Select 9 is equivalent to Box Clock.
   (b) Store Select 0 is equivalent to Hold.

APPENDIX 2/PIC1650A-532

This version interfaces either with an ASCII return to zero keyboard or with an AY-3-8475 remote control receiver. It replaces pattern 516.

INPUT (a) ASCII Return to zero
(b) Binary Return to zero (from local keyboard or AY-3-8475 remote control)
POWER UP MODE Picture
POWER UP DISPLAY (a) ASCII Teleview Cyan
(b) Binary Teleview Yellow
POWER UP PAGE XOO in Store 7
KEYBOARD INTERFACE

KB0 pin 19	LSB Input
KB1 pin 20	LSB Input
KB2 pin 21	LSB Input
KB3 pin 22	LSB Input
KB4 pin 23	LSB Input
KB5 pin 24	LSB Input
KB6 pin 25	MSB Input
KB7 pin 26	ASCII/Local Binary Input or Remote Acknowledge

KEYBOARD CODES

(a) ASCII
Standard 7 Bit ASCII (These codes are only acted upon in Viewdata Mode)

(b) Binary (Local or Remote)

Binary Code MSB LSB	Key Meaning
1100000	Picture/Text
1100001	Mix
1100010	Half Page Expansion
1100011	Store Select
1100100	7
1100101	8
1100110	9
1100111	Box Clock
1101000	4
1101001	5
1101010	6
1101011	Hold (Store Rotating Pages) (Release Line)

VIDEO

Binary Code MSB LSB	Key Meaning
1101100	1
1101101	2
1101110	3
1101111	Reveal/Conceal
1110000	Page (or * in Viewdata)
1110001	0
1110010	Time (or # in Viewdata)
1110011	Update/Clear
1110100	Rounding + Flash Off
1110101	Cursor ON
1110110	Cursor OFF
1110111	Roll Headers

NOTES:

1. During initialization the PIC1650A-532 decides whether an ASCII keyboard or an AY-3-8475 remote control receiver is being used. If all Keyboard Interface inputs are low an ASCII keyboard is assumed.
   (a) ASCII Mode
   Return to zero signalling is employed, the KB7 input being used to switch from full ASCII to local Binary.
   With KB7 equal to 1 the other 7 bits are read as standard ASCII. (Note this input must be pulsed with the other bits).
   With KB7 equal to '0' the other 7 bits are read as binary with meanings detailed above.
   (b) Remote Mode
   In this case the same binary codes are used but an acknowledgement routine is performed by the PIC1650A-532. See AY-3-8475 data sheet for details.
   The connections between the PIC1650A-532 and the AY-3-8475 are made as follows:

PIC1650A-532		AY-3-8475
KB0	pin 19	I/O A pin 14
KB1	pin 20	I/O B pin 15
KB2	pin 21	I/O C pin 16
KB3	pin 22	I/O D pin 17
KB4	pin 23	I/O E pin 20
KB5	pin 24	I/O F pin 21
KB6	pin 25	I/O G pin 22
KB7	pin 26	Digital Data Control + Data Available (pins 18, 19).

2. The codes should be valid for a minimum of 20ms. In the ASCII mode if the two key operation SS0 is used the Second code (0) should only be valid for a maximum of 120ms to avoid changing keyboard modes.
3. The double key operations are recognized:
   (a) Store Select 9 is equivalent to Roll Headers.
   (b) Store Select 0 is equivalent to Reset (Clear Stores).

APPENDIX 3/PIC1650A-519

This version interfaces with a 4 x 4 keyboard and as such may replace pattern 518.

It provides control of Viewdata functions only, together with local programing of Telephone numbers via PIC1650-536.

INPUT	4 x 4 matrix keyboard
POWER UP MODE	Text (picture mode not available). Cursor off
POWER UP DISPLAY	Double height Teleview in yellow on blue
POWER UP STORE	Store 1 (binary 000)
KEYBOARD INTERFACE	
KB0 pin 19	Row Input/Output
KB1 pin 20	Row Input/Output
KB2 pin 21	Row Input/Output
KB3 pin 22	Row Input/Output
KB4 pin 23	Column Input/Output
KB5 pin 24	Column Input/Output
KB6 pin 25	Column Input/Output
KB7 pin 26	Column Input/Output

KEYBOARD CODES

0/4	7	2/4	1
0/5	8	2/5	2
0/6	9	2/6	3
0/7	Hold/Disconnect	2/7	Reveal/Conceal
1/4	4	3/4	Star
1/5	5	3/5	0
1/6	6	3/6	Square
1/7	Half page expansion	3/7	Store Select

Operation

(a) Star, Square and digits 0-9 transmitted to line via UAR/T and MODEM. If 536 autodialer fitted then the square key plus digits 1-4 are used to dial.

(b) Hold. If 536 autodialer fitted this key will cause the telephone line to be released while maintaining the display.

(c) Print. The two key sequence SS.9 is used to alternately put the system into MIX mode and back to normal. Mix mode enables monochrome video to be generated and removes colored backgrounds. When entering mix mode character rounding and flashing are inhibited until a new page is received (only for AY-3-9735).

(d) Reveal/Conceal. Alternately reveals and conceals concealed characters. Reveal mode off when new page received or new store selected.

(e) Store select. Followed by digits 1-8 will select one of eight possible Stores for display. If 536 autodialer fitted and system in "link-back" mode then local programing of telephone numbers may be enabled by selecting Store zero. SS0 will clear screen and digits 1-4 may be pressed to enable the programing of the appropriate telephone number. The numbers entered using digits 0-9 (0 displayed as :), star for access pause (displayed as ;) and square for formatting and space filler (displayed as ?) to complete all 16 digits. SS0 followed by Reveal will display all the telephone numbers on the screen.

APPENDIX 4/PIC1650A-533

This version interfaces either with an ASCII, return to zero keyboard or with an AY-3-8475 remote control receiver and as such may replace pattern 532.

It provides control of Viewdata functions only together with Local Programing of Telephone numbers via PIC1650-536.

INPUT ASCII return to zero or binary return to zero from local keyboard or direct connection to remote receiver.

POWER UP MODE Text, Cursor off

POWER UP DISPLAY Double height Teleview in yellow on blue

POWER UP STORE Store number 1 (binary 000)

KEYBOARD INTERFACE

KB0 pin 19	LSB Input
KB1 pin 20	LSB Input
KB2 pin 21	LSB Input
KB3 pin 22	LSB Input
KB4 pin 23	LSB Input
KB5 pin 24	LSB Input
KB6 pin 25	MSB Input
KB7 pin 26	ASCII/Local Binary Input or Remote Acknowledge

KEYBOARD CODES

(a) ASCII

Full 7 bit ASCII set

(b) Binary (Local or Remote)

Binary Code	Key Meaning
1100000	Picture/Text
1100001	Print
1100010	Half page expansion
1100011	Store Select
1100100	7
1100101	8
1100110	9
1100111	(not used)
1101000	4
1101001	5
1101010	6
1101011	Hold/Disconnect line
1101100	1
1101101	2
1101110	3
1101111	Reveal/Conceal
1110000	Star
1110001	0
1110010	Square
1110011	Clear (inhibit display)
1110100	Rounding & Flashing off
1110101	Cursor ON
1110110	Cursor OFF
1110111	Reset

Notes 1 and 2 as for pattern 532.

Operation

(a) ASCII codes transmitted directly to line via UAR/T and MODEM. If 536 autodialer fitted, square and digits 1-4 will enable dialing.

(b) Picture/Text. Switches display alternately between picture and text. If 536 autodialer fitted this key will drop the telephone connection.

(c) Print. Alternately puts system into MIX mode and back to normal. Mix mode enables monochrome video to be generated and removes colored backgrounds. When entering mix mode character rounding and flashing are inhibited until new page received (only for AY-3-9735).

(d) Store/Select. Followed by digits 1-8 will select one of eight possible Stores for display. If 536 autodialer fitted and system in "link-back" mode then Local Programing of telephone numbers may be enabled by selecting store zero. SS0 will clear screen and digits 1-4 may be pressed to enable the programing of the appropriate telephone number. The number is entered using digits 0-9 (0 displayed as :) star for access pause (displayed as ;) and square as formatter and space filler (displayed as ?) to complete all 16 digits. SS0 followed by Reveal will display all the telephone numbers on the screen.

(e) Hold. If the 536 autodialer is fitted this key will drop the telephone line.

(f) Reveal/Conceal. Will alternately reveal and conceal concealed characters. Initialized to conceal state for new page or new Store.

(g) Clear. Clears the screen of all text. Display restored by second depression of the key and by reception of a new page.

(h) Rounding and Flashing Off. Character rounding and flashing may be inhibited in AY-3-9735 until a new page is received.

(i) Cursor ON/OFF. The cursor may be locally controlled by these codes.

(j) Reset. Simulate the power-on reset. All stores are cleared and initialized to "Teleview".