Mastering the PIC16C7X A/D Converter

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The Analog-to-Digital converter (A/D) is the primary tool that allows analog signals to be quantized into the world of digital electronics. Once the signal is digitally represented, it can be stored, analyzed and manipulated by a variety of logic devices. The PIC16C7X microcontrollers have an A/D integrated onto the PIC16CXX core processor. Utilizing Microchip's A/D requires only a basic level of understanding to get a result. However, maximizing the effectiveness of the A/D for each specific application requires a higher level of thought and understanding. Typically, a thorough comprehension of a device is obtained through experience, studying data sheets and studying application notes for a reasonable amount of time. This article addresses the main technical considerations for an effective design to reduce your design time.

When detailing how to maximize the effectiveness of any design, we look at the weakest (and strongest) elements. Please DO NOT misinterpret the statements detailing weaknesses to be below our specification. Our part specifications are based upon the worst case. All suggestions should improve on the worst case specifications.

We'll start by covering the A/D Basics, then dive into the other three general technical categories, which are essential for an effective design:

- Speed
- Accuracy
- Power Usage

BASICS

Specifications

Microchip's A/D is a successive approximation A/D which uses a bank of internal capacitors totalling 51.2 pF. The maximum resolution of the A/D is 8-bits. The converter accuracy specification is ±1 bit, but that can be made better or worse by your design. The analog channels are multiplexed to the converter which means that only one analog channel can be sampled at a time. The conversion time and maximum sampling frequency is application specific.

General

Even though we are converting to the 'digital world', we must remember that certain analog 'laws' still hold true. Specifically, the A/D is basically a capacitor which has to have time to charge/discharge to the analog level on the I/O pin before a conversion can be started. Source impedance and internal impedances add up to give an effective resistance in series with the capacitor(s). This RC time constant determines the minimum amount of charge/discharge time to achieve a desired accuracy. This time is the minimum tracking time (referred to as the minimum sampling time in our data book). Once the minimum time has been met, the voltage on the capacitor will track the voltage on the I/O pin until a conversion is started. Once the conversion has begun, the I/O pin is internally disconnected from the capacitor. The voltage on the capacitor is held constant for the entire conversion process. This type of sampling circuit is referred to as a "track and hold".

Step by Step

1. In order to perform a conversion, you must enable the A/D by setting the ADON bit (ADCON0 register).
2. Select the channel to be sampled by setting/clearing the CHS2, CHS1, and CHS0 bits (ADCON0 register). See the ADCON0 register's bit descriptions in the device's data sheet for the actual bit combinations for the selected channel(s).
3. The default input setup of all analog I/O pins is analog, not digital. For I/O pins set up as analog, the digital input buffers are internally disconnected. This is to keep analog voltages off of the CMOS input buffer. If the input voltage on a digital I/O was 0.5 V_{DD} for example, then both the PMOS and NMOS cells which make up the CMOS input buffer would be turned on. This causes the input buffer to draw around 100 to 150 µA.

If you are using an analog I/O as a digital input, load the register ADCON1 with the correct value to change the default from analog to digital. The I/O pin's bit will always read as a 0 when configured as an analog input (since it is disconnected from the pin). See the ADCON1 register's bit descriptions in the device's data sheet for the actual bit combinations for the selected channel(s).

Step by Step (cont'd)

4. Wait for at least the minimum tracking time. The tracking time is the time required to charge a 51.2 pF capacitor (located internal of the PIC16C7X) to the voltage level of the selected channel. The tracking time is made up of three components:
   - Amplifier Settling Time
   - Holding Capacitor Charging Time
   - Temperature Coefficient

$T_{TRACKING} = T_{AMP} + T_{CHARGE} + T_{TEMP}$

Given: $T_{tAMP} = 5\ \mu s$

Given: $T_{TEMP} = (\text{Temp} - 25°C)(0.05\ \mu s/°C)$, if $> 25°C$
$T_{TEMP} = 0$, if $\leq 25°C$

T_{CHARGE} Equation Derivation:

Basic Capacitor Charge Equation

$$V_{CAP} = V_{FINAL} - (V_{FINAL} - V_{INITIAL})\ e^{\frac{-T}{RC}}$$

or as it applies

$$V_{HOLDCAP} = V_{REF} - (V_{REF} - 0)\ e^{\frac{-T_{CHARGE}}{RC_{HOLD}}}$$

Where: $R = R_{IC} + R_{SS} + R_S$
R_S = Source Impedance
R_{IC} = Internal Interconnect Impedance
R_{SS} = Internal Sampling Switch Impedance

(see PIC16/17 Data Book, Section 13.1 for values)

$$C_{HOLD} = 51.2\ pF$$

$$V_{HOLDCAP} = V_{REF} - \frac{V_{REF}}{error}$$

Therefore:

$$\left(V_{REF} - \frac{V_{REF}}{error}\right) = V_{REF} - V_{REF}\ e^{\frac{-T_{CHARGE}}{(R_{IC} + R_{SS} + R_S)\ C_{HOLD}}}$$

$$V_{REF}\left(1 - \frac{1}{error}\right) = V_{REF}\left(1 - e^{\frac{-T_{CHARGE}}{(R_{IC} + R_{SS} + R_S)\ C_{HOLD}}}\right)$$

$$\frac{1}{error} = e^{\frac{-T_{CHARGE}}{(R_{IC} + R_{SS} + R_S)\ C_{HOLD}}}$$

$$T_{CHARGE} = -(R_{IC} + R_{SS} + R_S)\ C_{HOLD}\ (\ln \frac{1}{error})$$

Reducing this time can significantly reduce the accuracy of the result.

EXAMPLE 1:

$V_{DD} = V_{REF} = 5V$
$R_{IC} = 1\ k\Omega$
$R_{SS} = 7\ k\Omega$
$R_S = 10\ k\Omega$
$\text{Error} = 8 \text{ bits } \pm 1/2 = 2^9 = 512$

$T_{CHARGE} = -(1\ k\Omega + 7\ k\Omega + 10\ k\Omega)(51.2\ pF) \ln 1/512 = 5.75\ \mu s$

EXAMPLE 2:

Same values as Example 1, except we put a .01 µF decoupling capacitor on the I/O pin. This effectively reduces R_S to the impedance of the capacitor:
$R_S \approx 50\Omega$
$T_{CHARGE} = -(1\ k\Omega + 7\ k\Omega + 50\Omega)(51.2\ pF) \ln 1/512 = 2.57\ \mu s$

5. Choosing the A/D clock source (T_{AD}) determines the time required for the conversion of each bit. There are four choices for the clock source: $F_{OSC}/2$, $F_{OSC}/8$, $F_{OSC}/32$ and F_{RC}. Bits ADCS1 and ADCS0 (ADCON0 register) determine the clock source.

Table 1 will help you to choose the clock source according to your oscillator frequency.

TABLE 1: DEVICE OSCILLATOR FREQUENCY BY CLOCK SOURCE

	Fosc/2	Fosc/8	Fosc/32	FRC
PIC16C71	≤1 MHz	≤4 MHz	≤16 MHz	any F
PIC16C70/71A/72/73/74	≤1.25 MHz	≤5 MHz	≤20 MHz	any F

Note: F_{RC} assigns T_{AD} to an internal RC oscillator which is typically 4 µs (min = 2 µs, max = 6 µs).

To calculate the precise T_{AD} period you have chosen:

$$T_{AD} = \frac{x}{F_{OSC}} \quad \text{where x = either 2, 8 or 32}$$

6. After setting up the A/D and waiting the minimum tracking time, set the GO/DONE bit (ADCON0 register) to start the conversion.
7. Either poll for the GO/DONE bit to be cleared, poll for the ADIF to be set, or enable interrupts and wait for the interrupt to happen. When any one of these events occurs, the conversion is finished and the result is located in the ADRES register.
8. The A/D will begin tracking the analog signal again 2 T_{AD} (T_{RESET}) after the conversion has completed.
9. The time necessary to take an analog-to-digital sample is the total of tracking time plus conversion time. For repetitive samples, T_{RESET} is added to the total time. Use this equation to calculate the max. repetitive sampling rate ($F_{SAMPLING}$).

$1/F_{SAMPLING}$
$= T_{SAMPLE}$
$= T_{TRACKING} + T_{CONVERSION} + T_{RESET}$

SPEED

If your design will require an A/D sample time less than 60 µs, then you will want to consider the following factors: tracking time, conversion time, and minimum acceptable precision.

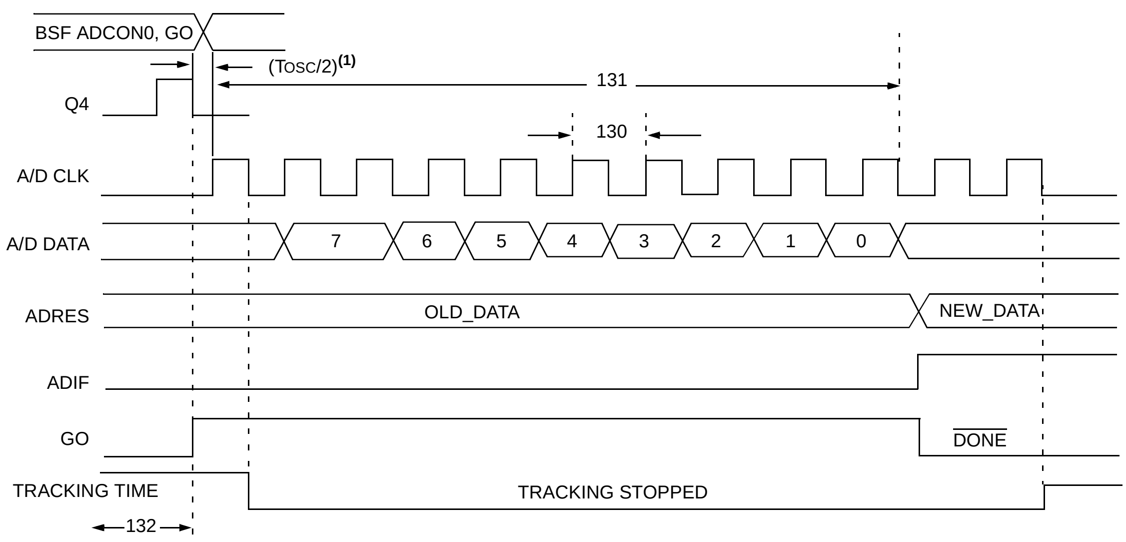
When choosing the clock source to get the fastest conversion time, we want to get a T_{AD} as close to (but not less than) 2 µs for a PIC16C71 and 1.6 µs for a PIC16C70, PIC16C71A, PIC16C72, PIC16C73 or PIC16C74.

1. What is the minimum precision your design requires (i.e., 4-bit, 6-bit or 8-bit)? This is an important question, since we can accelerate the conversion after the desired accuracy has been achieved. We cannot interrupt or abort the conversion after achieving the desired accuracy, since the result is not written to ADRES until the entire 8 bits have been converted (regardless of the accuracy of each bit). Figure 1 illustrates the timing required to determine each bit. Since the A/D operates synchronously with respect to the internal instruction cycle ($4/F_{OSC}$), we can accurately determine when to select a faster T_{AD} ($F_{OSC}/2$). The Least Significant bits determined after the conversion has been accelerated will be unreliable and most likely inaccurate. The following calculation determines the minimum amount of time before you can change the T_{AD} clock select bits for the resolution required.

$$T_{CONVERSION} = 1.5 \bullet T_{AD} + N \bullet T_{AD} + (8\text{-}N)(2 \bullet T_{OSC})$$

(where N = Number of bits of resolution)

FIGURE 1: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

TABLE 2: A/D CONVERSION REQUIREMENTS*

Param. #	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
130	T_{AD}	A/D Clock Period	1.6		—	μs	V_{REF} ≥ 3.0V
			2.0		—	μs	V_{REF} full range
130	T_{AD}	A/D Internal RC Oscillator source					ADCS1,0 = 11 (RC oscillator source)
			3.0	6.0	9.0	μs	PIC16LC74
			2.0	4.0	6.0	μs	PIC16C74
131	T_{CNV}	Conversion Time (not including S/H time) **(Note 1)**	—	9.5 T_{AD}	—	—	
132††	T_{SMP}	Sampling Time	5	—	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSb (i.e., 20 mV @ 5.12V) from the last sampled voltage (as stated on C_{HOLD}).

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† T_{TRACK} = T_{SMP}. Parameter #132 is T_{SMP} Sampling Time.

Note 1: ADRES register may be read on the following T_{CY} cycle.

EXAMPLE 3: A STANDARD 8-BIT (±1 LSb) FAST CONVERSION

Processor = PIC16C74

Oscillator = 20 MHz

Max possible T_{AD} = 1.6 μs

T_{AD} clock source = F_{OSC}/32 ∴ T_{AD} = 1.6 μs

$T_{TRACKING}$ = (5 μs + 0 μs + 2.57 μs) = 7.65 μs [from Example 2]

$T_{CONVERSION}$ = 1.5 • 1.6 μs + 8 • 1.6 μs + (8 - 8)(2 • 50 ns) = 15.2 μs

T_{AD_SAMPLE} = 15.2 μs + 7.6 μs + 2 • 1.6 μs = 26 μs

$F_{MAX\_A/D\_SAMPLING\_RATE}$ = 38.4 kHz

EXAMPLE 4: A 4-BIT (±1/32 LSb) FAST CONVERSION

Processor = PIC16C71

Oscillator = 16 MHz

Max possible T_{AD} = 2.0 μs

T_{AD} clock source = F_{OSC}/32 ∴ T_{AD} = 2.0 μs

$T_{TRACKING}$ = (5 μs + 0 μs + 2.57 μs) = 7.65 μs [from Example 2]

$T_{CONVERSION}$ = 1.5 • 2.0 μs + 4 • 2.0 μs + (8 - 4)(2 • 62.5 ns) = 11.5 μs

T_{AD_SAMPLE} = 11.5 μs + 7.6 μs + 2 • 2.0 μs = 23.1 μs

$F_{MAX\_A/D\_SAMPLING\_RATE}$ = 43.3 kHz

2. Executing a few instructions while the previous conversion is still running will allow ‘overhead’ code to be executed during the tracking time and conversion time. Don’t worry about using the data from the A/D immediately after the GO bit has been cleared. The ADRES register will contain the previous A/D result until it is updated with the new result. (The GO bit is cleared at that time.) In order to ensure that the sampling time is started as quickly as possible, set up the A/D channel for the next conversion (ADCON1) after the current tracking has stopped and before the current conversion is done (this will not affect the current conversion).

ACCURACY

Every designer should understand what effects the accuracy of the A/D. The following techniques may improve your designs. A meticulous and careful design can achieve approximately ±1 LSb.

1. A critical factor in our A/D's accuracy is the power supply to the PIC16C7X. Noise or ripple on V_{DD} can adversely affect the conversion's accuracy (the degree to which the accuracy is affected is dependent upon the amplitude of the noise). To improve the supply, use common filtering techniques, such as decoupling capacitors for various frequencies.

Note:	Remember that capacitors are not ideal and are really band-pass, not low-pass, filters (i.e., more than one of different values may be necessary).

2. V_{REF} can pull up to 1 mA for 8 to 20 ns when a conversion is started. The V_{REF} source (either RA3 or V_{DD}) doesn't change the current draw. Make sure your design can source this current (and be able to do it very fast). Capacitors on V_{REF} will act as a source for this current draw.
3. V_{DD} is a better V_{REF} source than RA3 because if noise is present on V_{DD}, it is absolutely coupled, NOT linearly coupled.

EXAMPLE 5:

20 mV of noise when V_{DD} = 5.0V = V_{REF} is ±1 LSb

20 mV of noise when RA3 = 3.0V = V_{REF} is ±1 LSb

4. Noise on the A/D input channel during tracking will add error to the desired result. A properly sized filter capacitor on the input pin will help correct this.

Note:	On the PIC16C71 and PIC16C70, RA0 is right next to OSC1 and cannot help but pick up some noise. If possible, make this pin an output to help isolate the noise from getting to RA1.

5. Increasing the tracking time ($T_{TRACKING}$) > 5 µs produces a measurable increase in accuracy. 20 µs is generally a good length of tracking time before starting a conversion.
6. Increase T_{AD} to about 4 µs. This allows the internal comparator response time to increase with less overdrive error. Notice that T_{RC} is typically 4 µs.
7. Operate at room temperature (25°C), since a high temperature increases leakage from the sample capacitor and low temperatures shift threshold levels. If you know that high temperature operation is possible, keep T_{AD} as close to the minimum as possible.
8. Do not change the value on any I/O pins which are configured as output while a conversion is in progress (regardless of the port). The high source/sink capability of the pins could directly inject noise onto V_{DD}..
9. The A/D is capable of finishing a conversion while the part is sleeping. Putting the part to SLEEP helps accuracy, since this mode eliminates the internal switching noise of the processor core.

Note:	You can do this with any Oscillator mode, but you will have to allow for the osc wake-up time when using LP, XT or HS modes. RC mode has no start-up timer and starts up instantly.

If you put the processor to SLEEP, consider clearing all interrupt enable bits (including the GIE bit), except for the ADIE. This will cause the processor to wake-up from SLEEP when the conversion is complete and resume executing code with the instruction following the `SLEEP` instruction. This method helps simplify your Interrupt Service Routine for other peripherals.

EXAMPLE 6: (PIC16C71 AND PIC16C70)

```
CLRF    INTCON
BSF     INTCON,ADIE
BSF     ADCON0,GO
SLEEP
MOVF    ADRES,0
```

POWER USAGE

The following simple, straight forward pointers can help any application meet its power requirements.

1. Keeping the A/D turned off until you are ready to start tracking will reduce approximately 180 µA of current draw from your system. The ADON (ADCON0) bit turns the A/D on or off.
2. Configure all analog inputs to be analog since this will disconnect the CMOS digital input buffer. If you do not, and the signal on the pin is 0.5 V_{DD}, both transistors in the CMOS input buffer will be turned on, causing the maximum current draw of the input buffer.
3. You may want to put the controller to SLEEP during the conversion. There are several factors to consider for this decision, here are a few:
   - The F_{RC} move must be selected for A/D conversion clock.
   - Do you have any timers running that cannot be stopped?
   - Is the wake-up from SLEEP time longer than the conversion time?
   - Can you afford to lose the processing time while sleeping and waking up from SLEEP?

Keeping the A/D Usage Simple

- Put a decoupling capacitor on V_{DD}.
- Put a .01 µF capacitor on the analog input source.
- Select which pins are digital and which pins are analog (register ADCON1).
- Using the internal RC oscillator to determine the T_{AD} provides a relatively fast and accurate conversion for most applications (bits ADCS1, ADCS0 = 1,1 in register ADCON1). If you are using RC mode for the core's oscillator, then you should put the part to SLEEP during the conversion, or choose an appropriate T_{AD} source other than RC.
- Select which channel is to be sampled (bits CHS2, CHS1 and CHS0 in register ADCON0).
- Turn on the A/D by setting the ADON bit (register ADCON0).
- Wait 20 µs (tracking time).
- Set the GO bit (register ADCON0) to start the conversion.
- Poll either the ADIF or the GO bit to determine when the conversion has completed.
- Utilize the result located in the ADRES register.
- Clear the ADIF bit.

EXAMPLE 7:

```
           BSF        STATUS,RP0
           MOVLW      0xFE              ;MAKE RA0 AN OUTPUT
                                        ;AND RA1 AN INPUT
           MOVWF      TRISA
           CLRF       ADCON1            ;MAKE ANALOG INPUTS
           BCF        STATUS,RP0
           MOVLW      0C9h              ;RC OSC, RA1, ADON
           MOVF       ADCON0,W
           CALL       20US_DELAY
GIE_OFF    BCF        INTCON,GIE        ;
           BTFSC      INTCON,GIE        ;MAKE SURE BCF WAS NOT INTERRUPTED
           GOTO       GIE_OFF           ;
           BSF        ADCON0,G0
AD_GOING   BTFSC      ADCON0,GO
           GOTO       AD_GOING
           ;Result is located in ADRES
```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