Discrete Logic Replacement

Logic Level Divisor by Factor of 1 to 15 or 255

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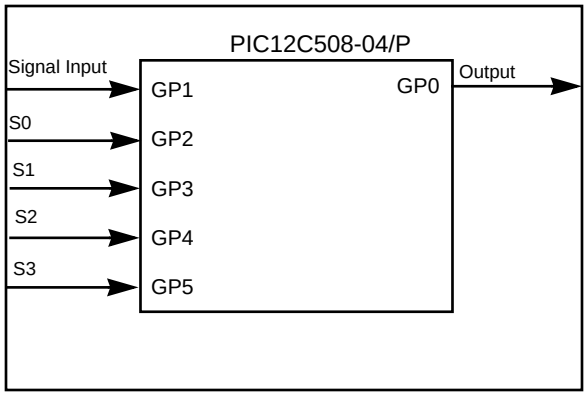
APPLICATION OPERATION :

The operation is very simple. The signal input on GP1 is divided by the factor selected at the input S3-S0. The max frequecy input is about 25 KHz or more depending on the internal RC.

Division Factor Table:

S3	S2	S1	S0	Division factor
0	0	0	0	255
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Block Diagram :



APPENDIX A: SOURCE CODE

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;*************************************************************************************************
;
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;   Project : PicDiv
;   date    : august 24  1997
;   Note    : Internal RC, No MCLR
;*************************************************************************************************
list p=12c508, f=inhx8m ;uC number
                                    ;and inhx8m output format file
gpio       equ     0x06         ; adrs  io
tmr0       equ     0x01         ; adrs  timer
status     equ     0x03         ; status register adrs
osccal     equ     x05          ; oscillator calibration register
lastlevel  equ     0x07         ; Last logic level
di         equ     0x08         ; div. factor
temp       equ     0x09         ; temp.
           org                  0000
begin
           movlw   0x3e         ; gp0 = output  gp1 gp2 gp3 gp4 gp5 = input
           tris    6            ;
           btfss   gpio,1       ; Set input level init.
           goto    zerlog       ; Branch if input is zero
           bsf     lastlevel,0  ; set last level to one
           goto    readiv       ; branch to zerlog
zerlog                          ; here input level is zero
           bcf     lastlevel,0  ; Set last level to zero
readiv     movf    gpio,0       ; read div. factor
           andlw   0x3c         ; be sure that higher bits are 0.
           movwf   div          ; move W to F to rotate it
           rrf     div,1        ; rotate right to put away lower
           rrf     div,1        ; 2 bits

readin     clrw                 ; Clear W
           btfss   gpio,1       ; test input
           goto    zero         ; branch to zero
           movlw   0x01         ; if one then w = 01
zero       addwf   lastlevel,0  ; add to last level
           movwf   temp         ; move f to temp to test bit 0
           btfss   temp,0       ; If temp = 1 then a input as changed
           goto    readin       ; If level not changed then branch to readin
change     movlw   0x01         ; load 1 in W
           xorwf   lastlevel,1  ; change last level to is complement
           decfsz  div,1        ; dec. div to see if it's time to toggle
           goto    readin       ; goto readin if div /= to zero
toggle     movlw   0x01         ; load 1 in W
           xorwf   gpio,1       ; Toggle output
           goto    readiv       ; restart read division
           end
```