

Using the C18 Compiler and the MSSP to Interface SPI™ EEPROMs with PIC18 Devices

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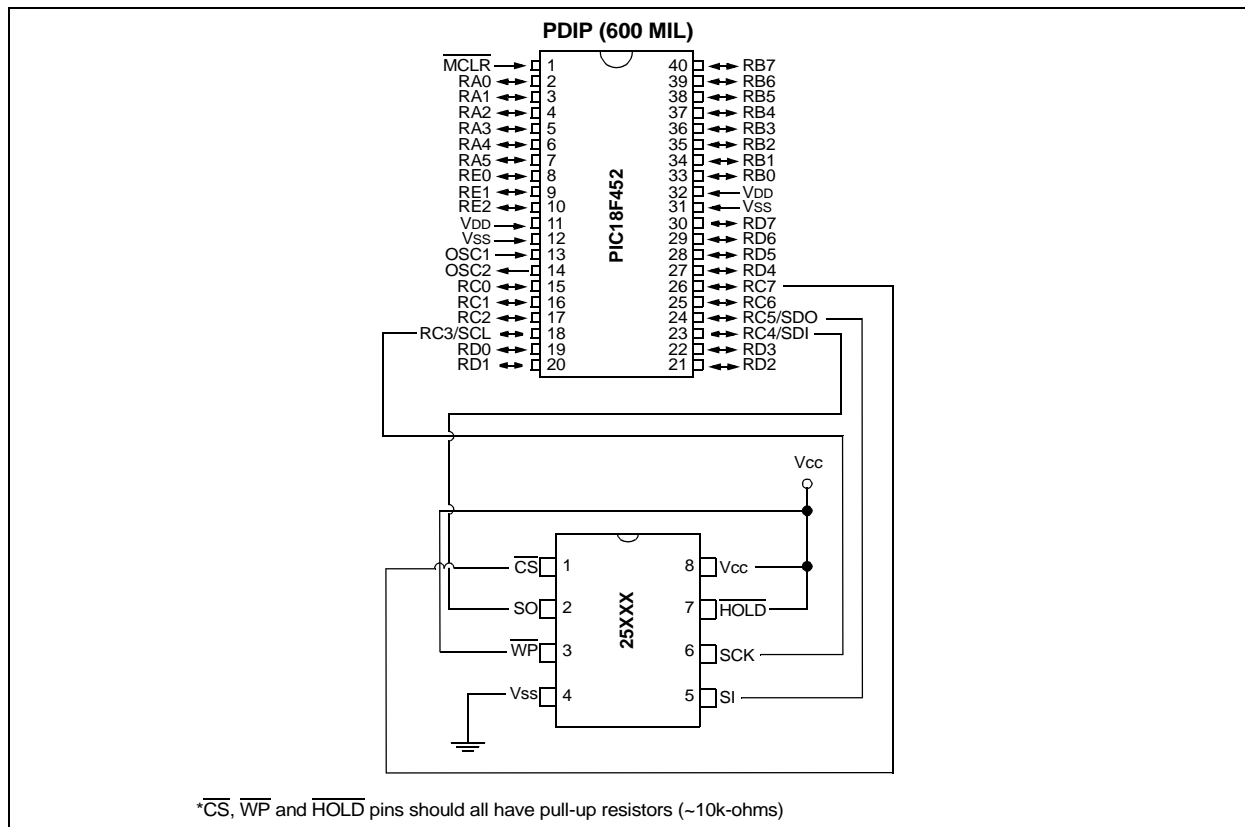
INTRODUCTION

The 25XXX series serial EEPROMs from Microchip Technology are SPI™ compatible and have maximum clock frequencies ranging from 3 MHz to 20 MHz. The MSSP module available on many PICmicro® microcontrollers provides a very easy-to-use interface for communicating with the 25XXX series devices. The largest benefit of using the MSSP module is that the signal timings are handled through hardware rather than software. This allows the firmware to continue executing while communication is handled in the background. This also means that an understanding of the timing specifications associated with the SPI protocol is not required in order to use the 25XXX series devices in designs.

This application note is intended to serve as a reference for communicating with Microchip's 25XXX series serial EEPROM devices with the use of the MSSP module featured on many PIC18 family devices. Source code for common data transfer modes is also provided.

Figure 1 describes the hardware schematic for the interface between Microchip's 25XXX series devices and the PIC18F452 PICmicro microcontroller. The schematic shows the connections necessary between the microcontroller and the serial EEPROM as tested, and the software was written assuming these connections. The \overline{WP} pin is tied to Vcc because the write-protect feature is not used in the examples provided.

FIGURE 1: CIRCUIT FOR PIC18F452 AND 25XXX SERIES DEVICE



FIRMWARE DESCRIPTION

The purpose of the firmware is to show how to generate specific SPI transactions using the MSSP module on a PICmicro microcontroller. The configuration required for SPI mode 0,0 is explained, as well as some of the specific details of the SPI protocol. The focus is to provide the designer with a strong understanding of communication with the 25XXX series serial EEPROMs using the MSSP module and SPI, thus allowing for more complex programs to be written in the future. The firmware was written in C and the Microchip C18 compiler was used. Whenever possible the standard SPI library routines were used.

Besides the standard SPI libraries supplied with the C18 compiler, the firmware consists of two .c files (AN995.c and SPI.c), organized into nine sections:

- Initialization
- Low Density Byte Write
- Low Density Byte Read
- Low Density Page Write
- Low Density Sequential Read
- High Density Byte Write
- High Density Byte Read
- High Density Page Write
- High Density Sequential Read

The low density routines are intended for use with the 4K and smaller density devices that use only one byte for addressing. Considerations need to be made to fully address the 24XX040X, 4K device. The Most Significant bit (A8) of the address resides in the control code, please refer to the data sheet for particulars. The high density routines are intended for use with 8K and higher density devices that use two bytes of address. This program also exhibits the WIP polling feature for detecting the completion of write cycles after the byte write and page write operations. Read operations are located directly after each write operation, thus allowing for verification that the data was properly written. No method of displaying the input data is provided, but a SEEVAL[®] 32 evaluation system, an oscilloscope, or a Microchip MPLAB[®] ICD 2 could be used.

The code was tested using the 25LC256 serial EEPROM. This device features 32K x 8 (256 Kbit) of memory and 64-byte pages. Oscilloscope screen shots are labeled for ease in reading. The data sheet version of the waveforms are shown below the oscilloscope screen shots. All timings are designed to meet the data sheet specs, and a 10 MHz crystal oscillator is used to clock the PIC18F452. If a faster clock is used, the code must be modified for the MSSP module to generate the correct clock frequency. All values represented in this application note are hex values unless otherwise noted.

INITIALIZATION

In order to configure the MSSP module for SPI mode 0,0, several key registers on the PICmicro microcontroller need to be properly initialized. Code examples are shown for each.

SSP STATUS Register (SSPSTAT)

SSPSTAT holds all of the Status bits associated with the MSSP module. In SPI mode 0,0 the SMP bit of the register needs to be set for data to be sampled at the end of the output time. The CKE bit also needs to be set for mode 0,0 operation, this assures that data is transmitted on the rising edge of SCK when CKP bit (SSPCON1) is cleared. This is done as shown in Example 1.

EXAMPLE 1: SSPSTAT CONFIGURATION

```
SSPSTAT = 0xC0; //SPI Bus mode 0,0
```

SSP Control Register 1 (SSPCON1)

SSPCON1 is one of the Configuration registers for the MSSP module. In SPI mode 0,0, the upper two bits of SSPCON1 are indicator bits and should be cleared initially. Also, while in mode 0,0, the Clock Polarity Select bit (CKP) needs to be cleared for Idle state of the clock to be a low level. The SSP Enable bit (SSPEN) must be set in order to enable the serial port. The mode is set using the SSPM3:SSPM0 bits, '0001', for SPI Master with FOSC/16 for approximately 625 kHz operation. This register is configured using the code shown in Example 2.

EXAMPLE 2: SSPCON1 CONFIGURATION

```
SSPCON1 = 0x21; //Enable SSP,Fosc/16
```

TRISC Register

In order to be properly controlled by the MSSP module, the \overline{CS} , SCK, SDI and SDO pins must be configured properly. This is done by setting their respective bits in TRISC to '1' for inputs and '0' for outputs, as shown in Example 3.

EXAMPLE 3: TRISC CONFIGURATION

```
DDRCbits.RC7 = 0;
                //Define CS as Output
DDRCbits.RC3 = 0;
                //Define SCK as Output
DDRCbits.RC4 = 1;
                //Define SDI as Input
DDRCbits.RC5 = 0;
                //Define SDO as Output
```

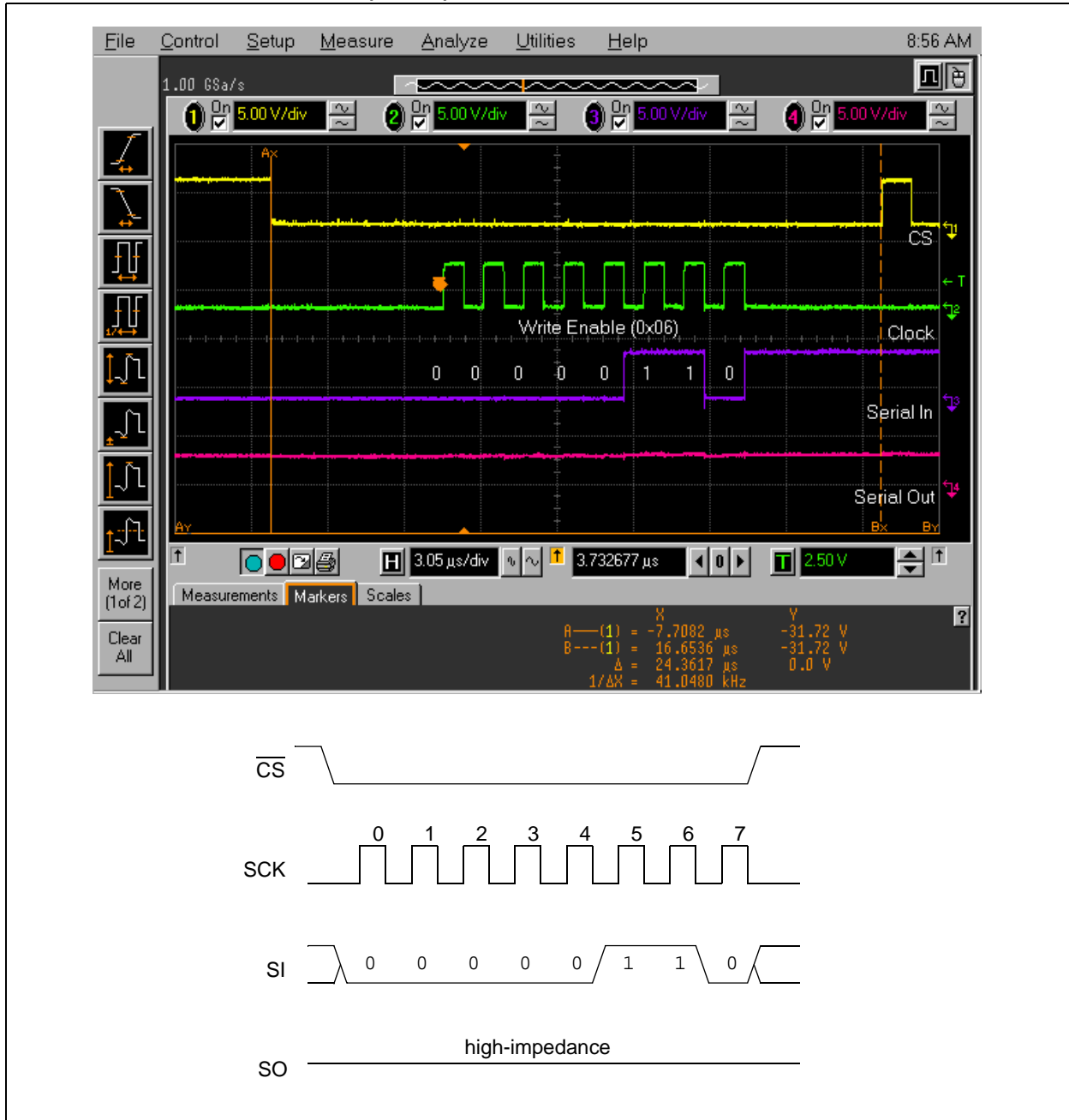
AN995

WRITE ENABLE

Figure 2 shows an example of the Write Enable command. Chip Select is brought low (active) and the opcode is sent out through the MSSP port. The Write Enable command must be given before a write is attempted to either the array or the STATUS register.

The WEL bit can be cleared by issuing a Write Disable command (WRDI) or it is automatically reset if the device is powered down or a write cycle is completed.

FIGURE 2: WRITE ENABLE (WREN)

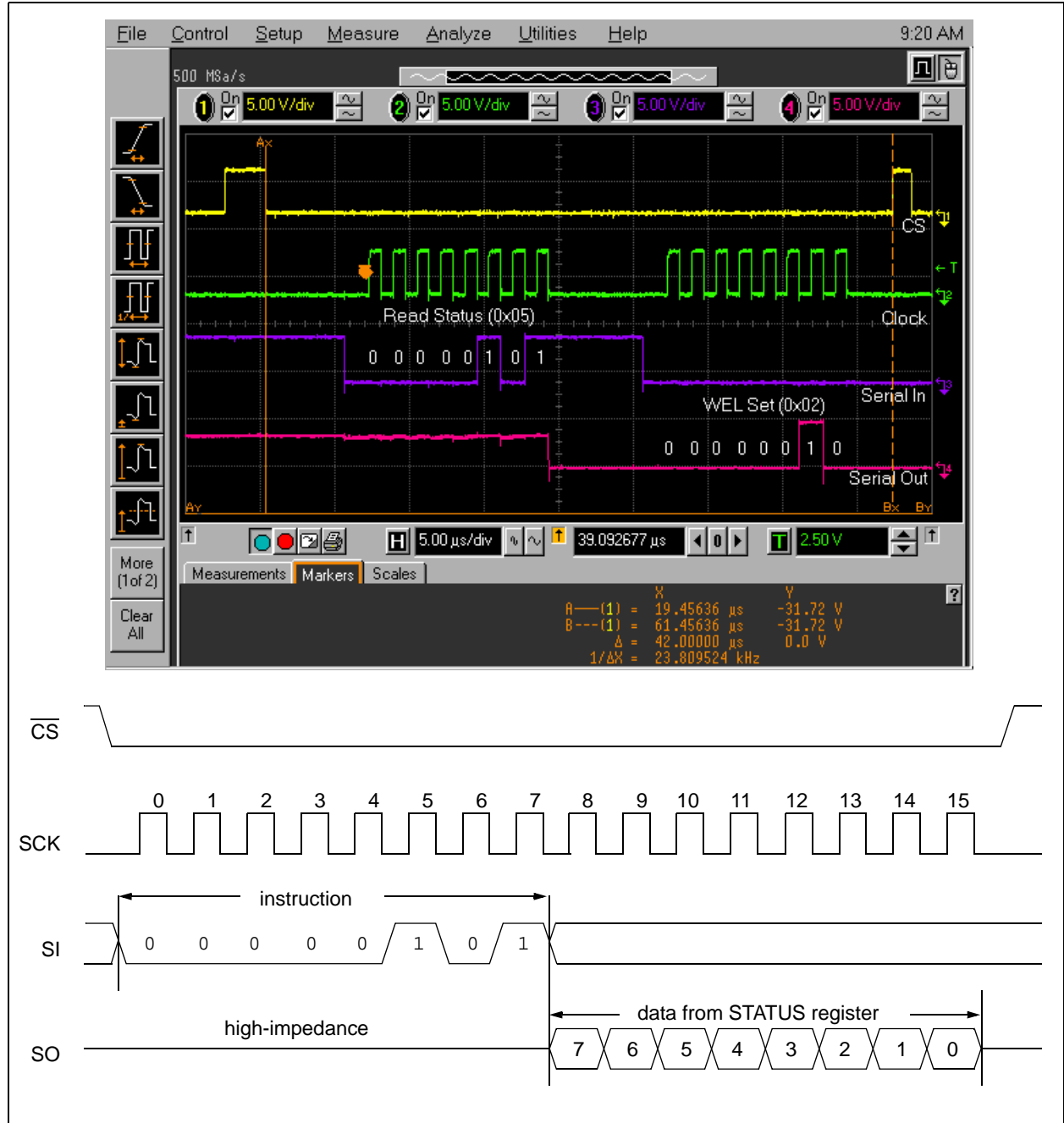


READ STATUS REGISTER TO CHECK FOR WEL BIT

Figure 3 shows an example of the Read Status Register command to check for the WEL bit. The WEL bit must be set before a write is attempted to either the STATUS register or the array. It is good programming practice to check for the bit to be set before attempting the write. Once again the device is selected and the opcode 0x05 is sent.

The STATUS register is shifted out on the Serial Out pin. A value of 0x02 shows that the WEL bit in the STATUS register has been set. The device is now ready to do a write to either the STATUS register or the array.

FIGURE 3: READ STATUS REGISTER TO CHECK FOR WEL BIT (RDSR)

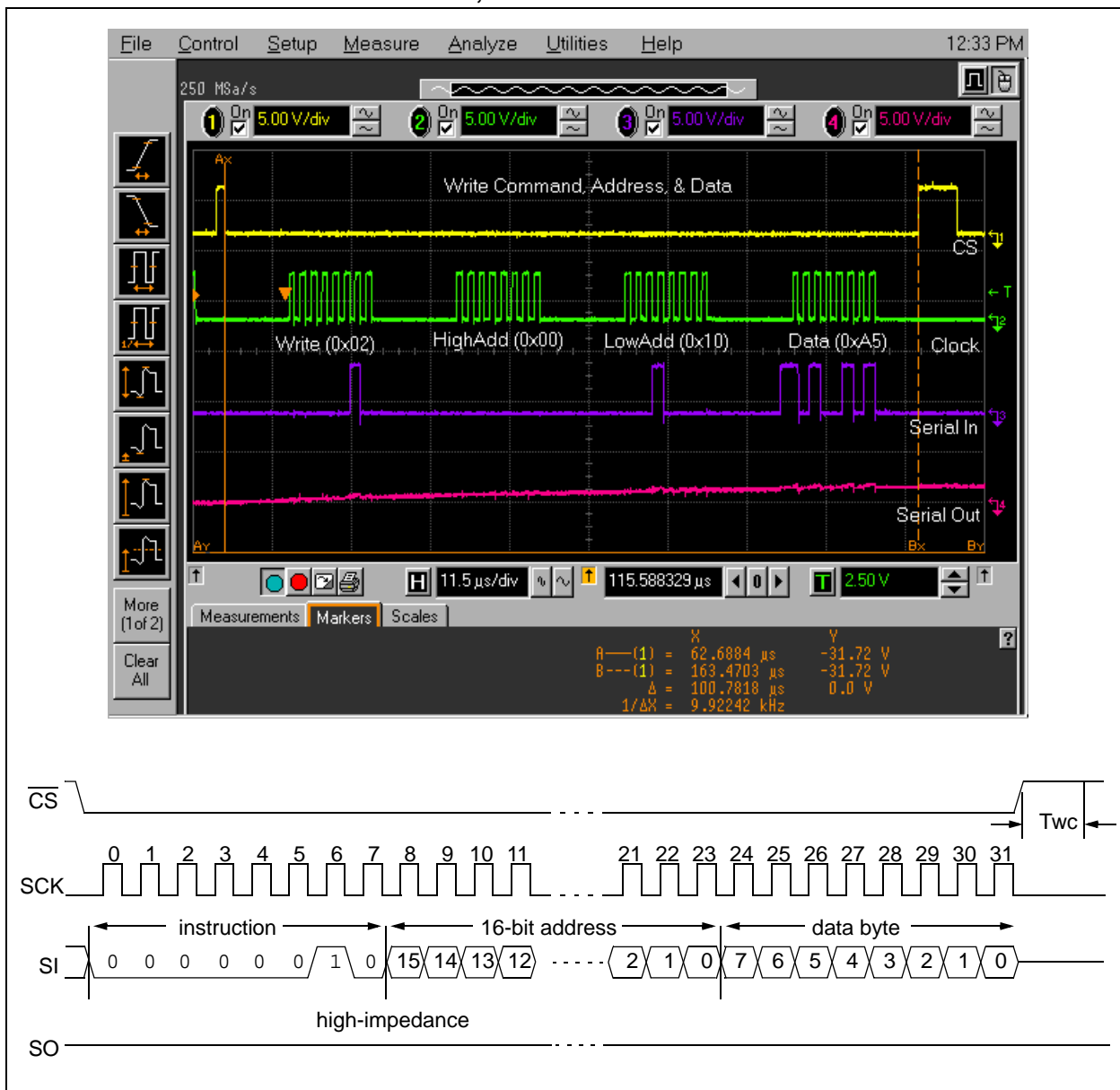


BYTE WRITE COMMAND (OPCODE, ADDRESS AND DATA)

Figure 4 shows an example of the Write command. For this, the device is selected and the opcode 0x02 is sent. The High Address byte is given 0x00, followed by the Low Address byte, 0x10. Finally, the data is clocked in last, in this case, 0xA5. Once the Chip Select is toggled at the end of this command, the internal write cycle is initiated. Once the internal write cycle has begun, the WIP bit in the STATUS register can now be polled to check when the write finishes or a delay needs to be added (~5ms), if the WIP bit is not being polled. This code uses WIP polling.

A page write can be accomplished by continuing to give data bytes to the device without toggling \overline{CS} . Up to 64 bytes can be written to the 25LC256 before a write cycle is needed. Once \overline{CS} is brought high after the data bytes have been transmitted, then the write cycle timer will begin and normal polling can be initiated. The Page Write function programs all 64 bytes of data in the first page. Since the starting address is 0x0010, the last 16 bytes of data will wrap from address 0x3F to 0x00 and complete the page. Caution should be taken when page writes are initiated in this manner so that previously stored data doesn't get over written.

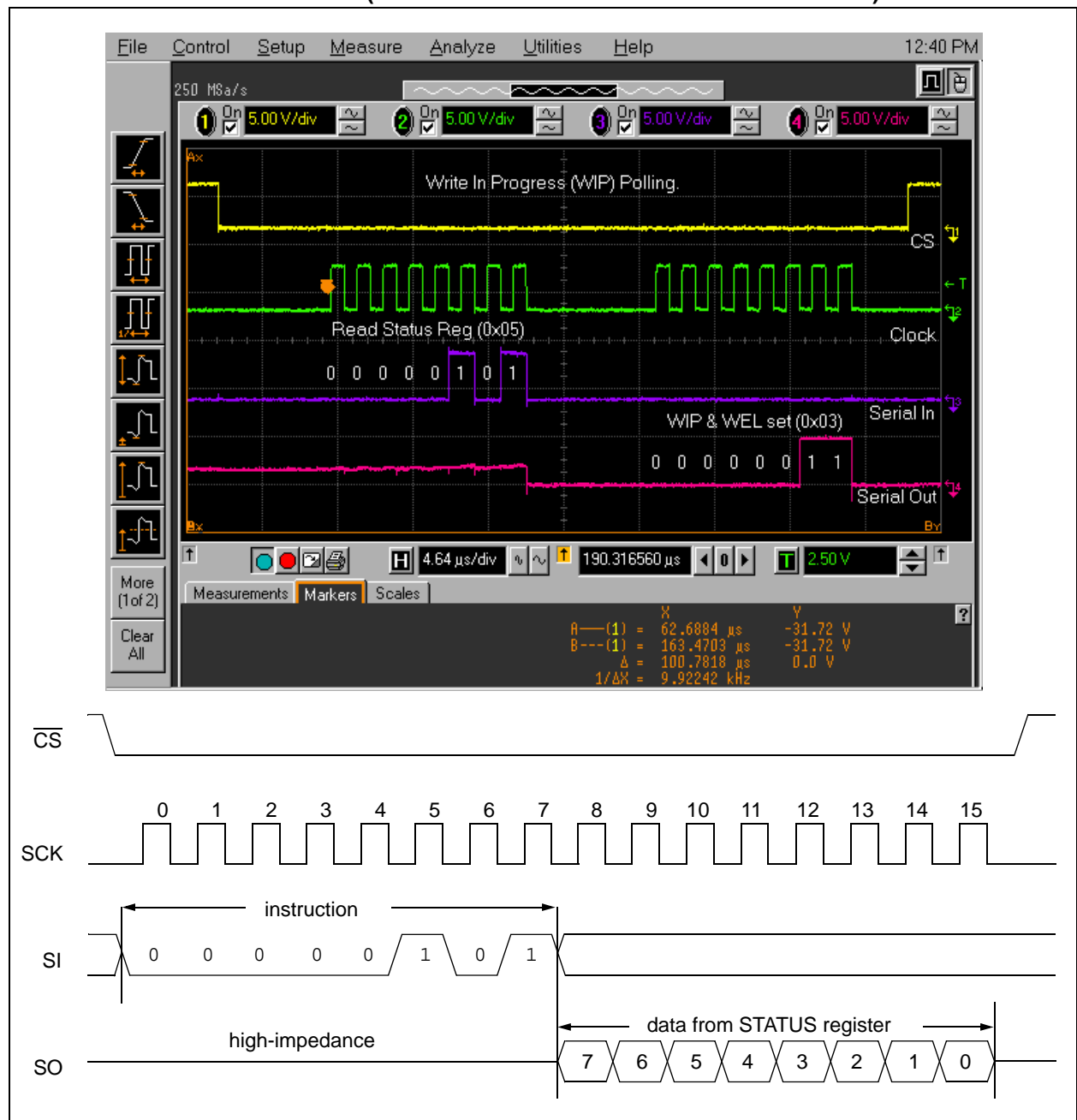
FIGURE 4: BYTE WRITE COMMAND, ADDRESS AND DATA



DATA POLLING (RDSR – CHECK FOR WIP SET)

After a valid Write command is given, the STATUS register can be read to check if the internal write cycle has been initiated, and it can continuously be monitored to look for the end of the write cycle. In this case, the device is selected and the opcode, 0x05, is sent. The STATUS register is then shifted out on the Data Out pin resulting in a value of 0x03. Figure 5 shows that both the WEL bit (bit 1) and the WIP bit (bit 0) are set, meaning the write cycle is in progress.

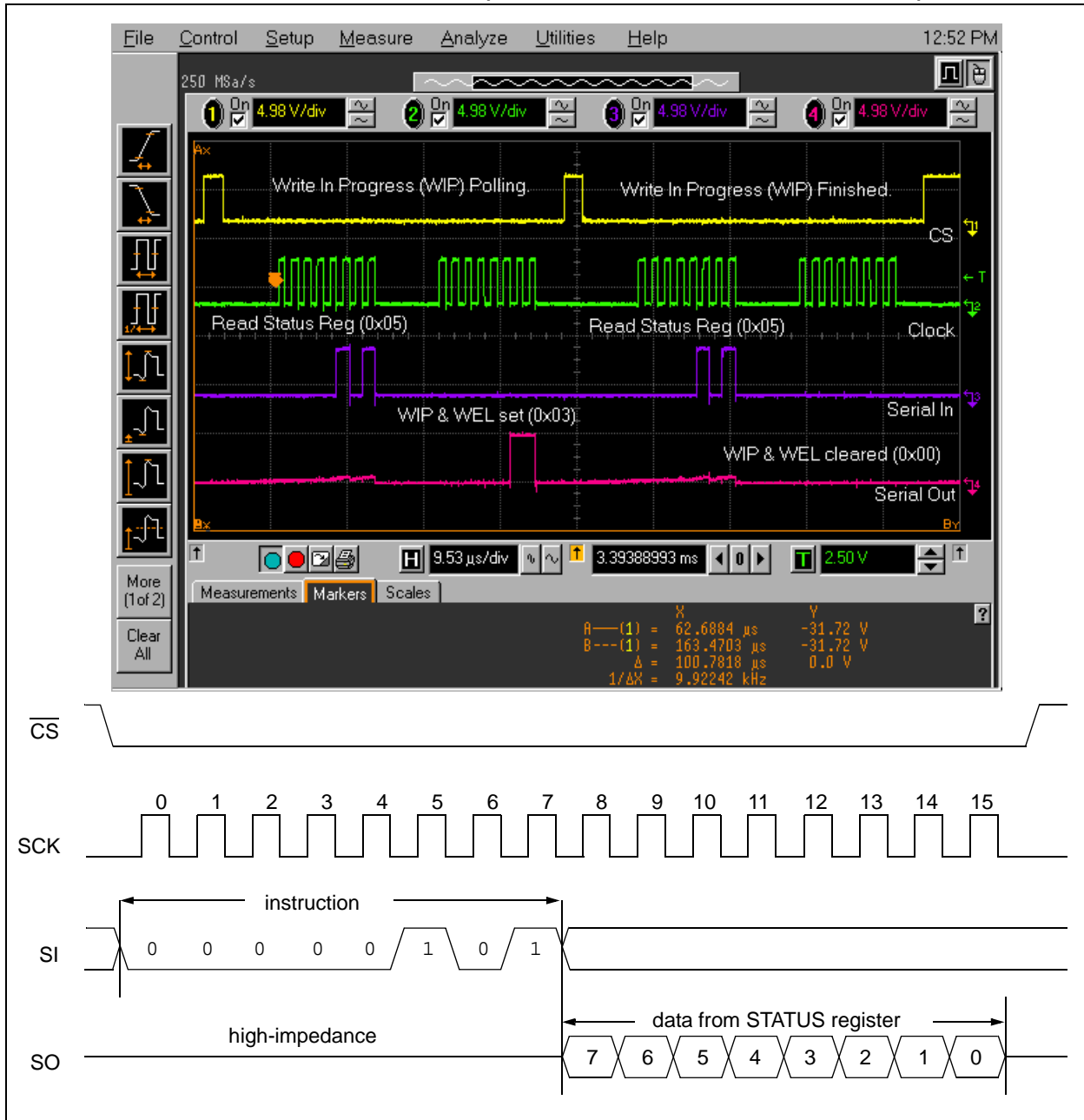
FIGURE 5: DATA POLLING (READ STATUS REGISTER TO CHECK WIP BIT)



DATA POLLING FINISHED (RDSR – WIP BIT CLEARED)

The part remains in a continuous loop and the WIP status is evaluated until the bit is cleared. Figure 6 shows the Status Register Read command followed by a value of 0x00 being shifted out on the Data Out pin. This indicates that the write cycle has finished and the device is now ready for additional commands. The WEL bit is also cleared at the end of a write cycle, which serves as additional protection against unwanted writes.

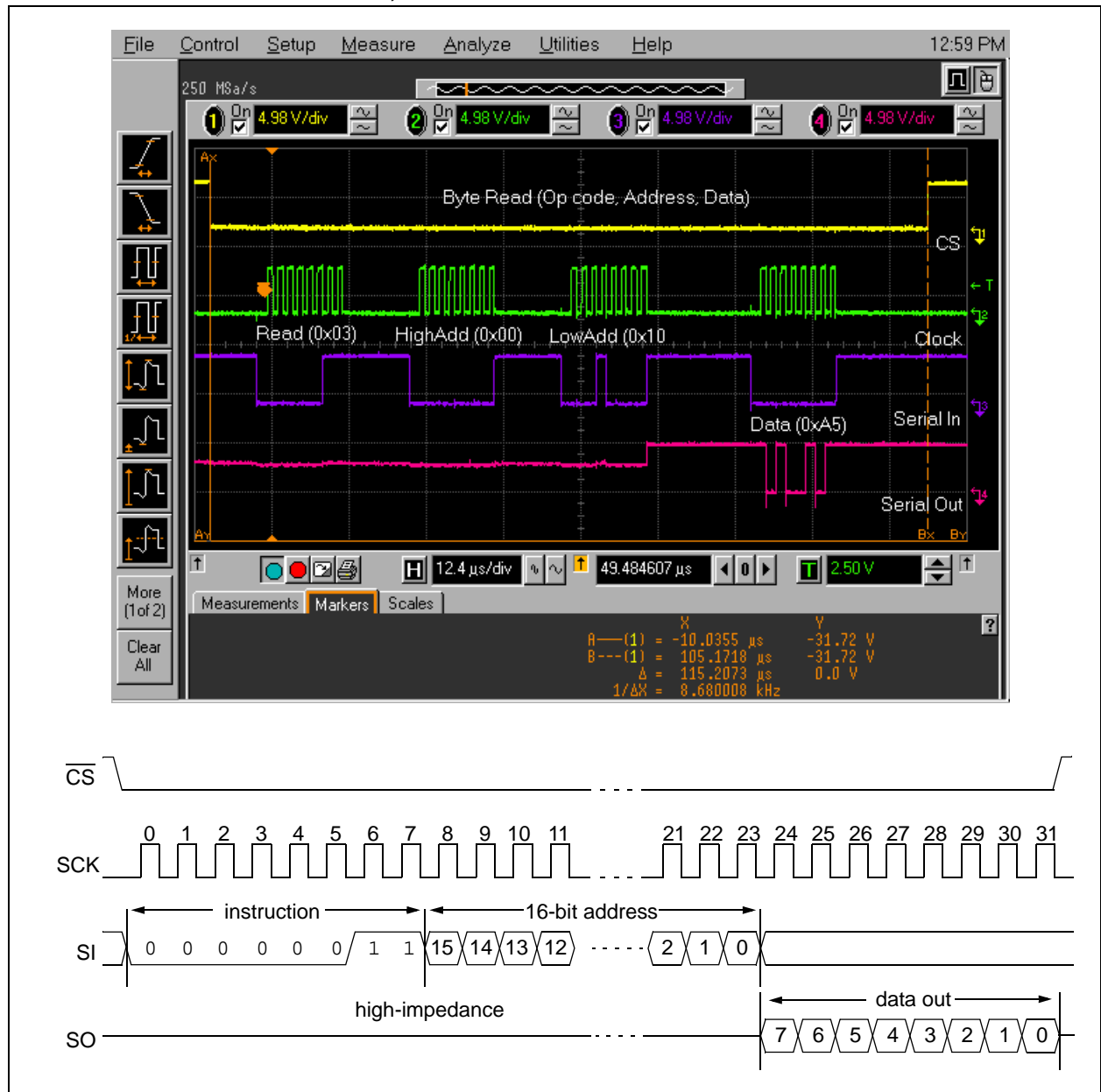
FIGURE 6: DATA POLLING FINISHED (RDSR – WIP AND WEL BITS CLEARED)



READ COMMAND (OPCODE, ADDRESS AND DATA)

Figure 7 shows an example of the Read command. For this, the device is selected and the opcode 0x03 is sent. The High Address byte is given 0x00, followed by the Low Address byte, 0x10. Finally, the data is clocked out on the Serial Out pin, in this case, 0xA5. In order to do a sequential read, more clocks need to be generated. It is possible to read the entire chip by continuing to provide clocks to the device. Once the end of the array is reached, the data will wrap to the beginning of the array (Address 0x00) and keep reading out until \overline{CS} is deselected or clocks stop being provided.

FIGURE 7: READ COMMAND, ADDRESS AND DATA



CONCLUSION

These are some of basic features of SPI communications using the MSSP module on one of Microchip's mid-range devices. The code is highly portable and can be used on many devices that have the MSSP module with very minor modifications. Using the code provided, designers can begin to build their own SPI libraries to be as simple or complex as needed. The code was tested on Microchip's PICDEM™ 2 Plus Demonstration Board with the connections shown in Figure 1.

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