# AN975

## Using the MSSP Module to Interface Microwire Serial EEPROMs to PIC16 Devices


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## INTRODUCTION

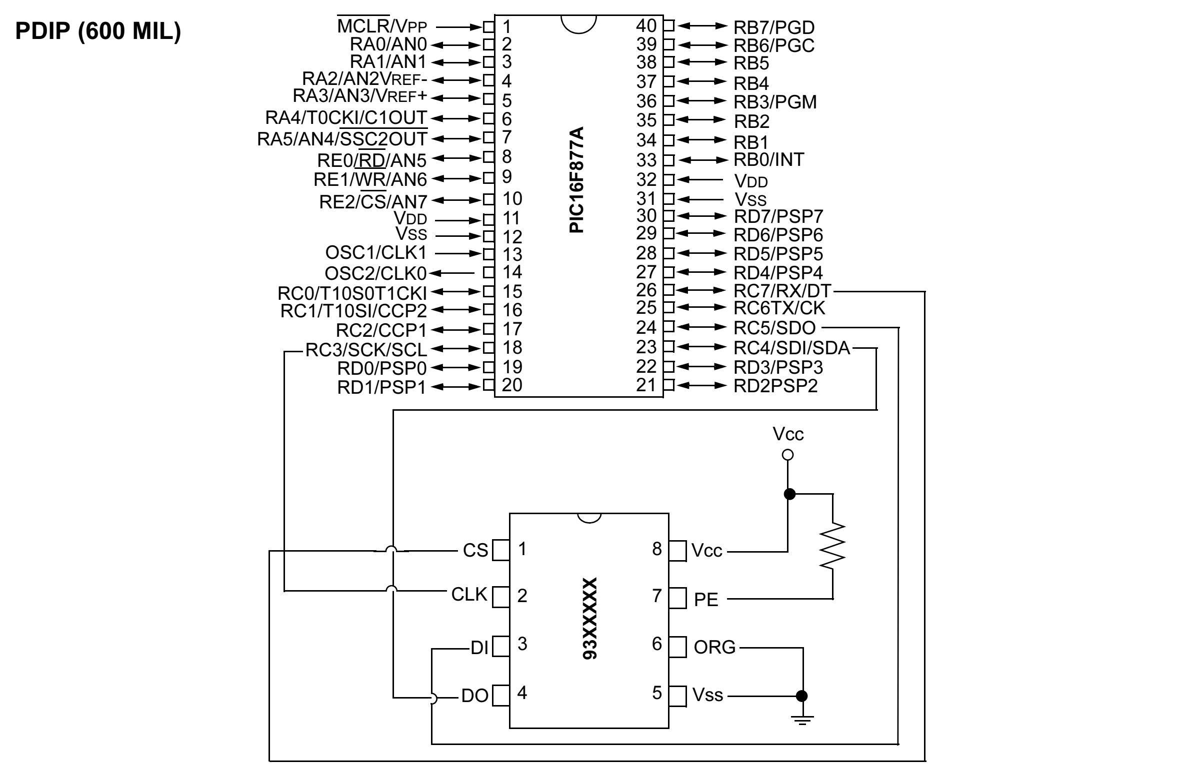
There are many different microcontrollers on the market today that are being used in embedded control applications. Many of these embedded control systems need nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low power consumption and low cost, serial EEPROMs are a popular choice for nonvolatile storage.

Microchip Technology has addressed these needs by offering a full line of serial EEPROMs covering industry standard serial communication protocol for two-wire ($I^2C$™), three-wire (Microwire), and SPI™ communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges, and packaging options.

This application note provides assistance and source code to ease the design process of interfacing a Microchip mid-range PIC16F877A microcontroller to a Microchip Microwire serial EEPROM. The Master Synchronous Serial Port (MSSP) provides a simple three-wire connection to the EEPROM and no external "glue" logic is required.

Figure 1 depicts the hardware schematic for the interface between Microchip's Microwire devices and the Microchip PIC16F877A Microcontroller. The schematic shows the necessary connections to interface the microcontroller and the serial EEPROM (software was written assuming these connections).

**FIGURE 1: CIRCUIT FOR PIC16F877A AND 93 SERIES (MICROWIRE) DEVICE**




*CS should always have a pull-down resistor to protect against data corruption during power-up or power-down of the Microcontroller.

*PE pin available only on 93XX76X and 93XX86X devices. Pull-up resistor suggested ~10K ohm.

## THEORY OF OPERATION

To use an SPI port to communicate with Microchip's Microwire Serial EEPROMs, the bytes to be output to the 93XXXX must be aligned such that the LSB of the address is the 8th bit (LSB) of a byte to be output. From there the bits should fill the byte from right to left consecutively. If more that 8 bits are required, then two bytes will be required to be output. This same method will work for any 93XXXX series device. Since more than 8 bits are necessary to control a 93LC66C, two consecutive bytes are required.

**High Byte** (Start bit, opcode bits and address MSb)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | SB | OP1 | OP0 | A8 |

The High Byte is configured in the following format: SB is the Start bit. OP1 is the MSb of the opcode and OP0 is the opcode LSb. A8 is the 9th address bit that is required to address 512 bytes. The CS line can be set before the byte is output, because the leading 0's output to the 93XXXX prevents a Start bit from being recognized by the 93XXXX until the first high bit is sent.

**Low Byte** (8 Address bits)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

The Low Byte contains A7-A0, which are the remaining address bits required to access 512 bytes.

Data output from the master MUST be set up on the falling edge of the clock so that it can be read from the 93XXXX on the next rising edge. Receiving data from the 93XXXX MUST also happen on the falling edge of the clock because the data is output from the 93XXXX on the rising edge of the clock. This requires the clock phase bit (bit 4 of the SSPCON register) of the MSSP port to be opposite for receiving than it is for transmitting. The clock phase needs to be cleared for transmitting and set for receiving data.

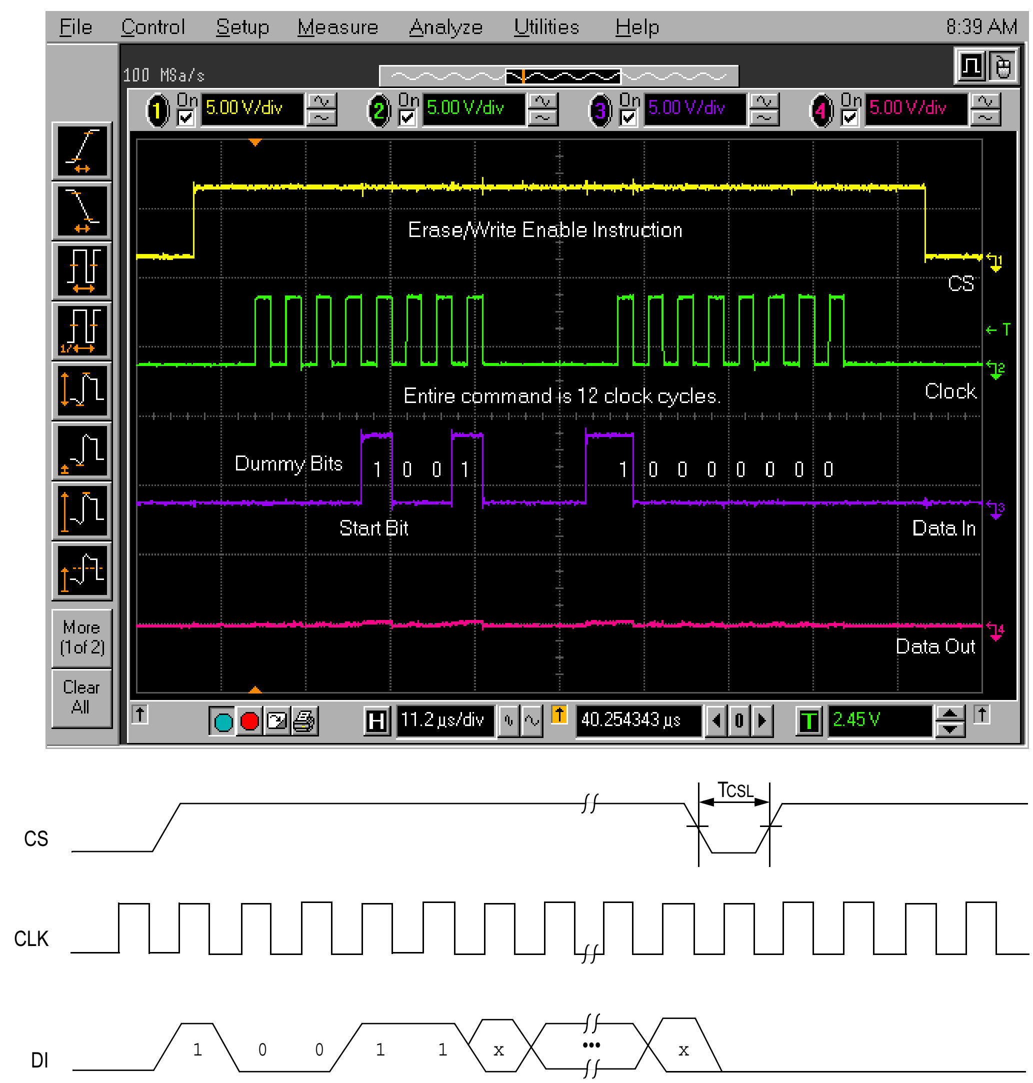
## FIRMWARE DESCRIPTION

The purpose of the program is to show individual features of the Microwire protocol and give code samples of the Start bit, opcodes and addressing schemes so that the basic building blocks of a program can be shown. The waveforms provided will be shown from CS active to CS disable so an entire instruction can be seen. To ease the interpretation of the serial data, the data sheet waveform will be provided below the oscilloscope screen shot.

## WRITE ENABLE

Figure 2 shows an example of the Erase/Write Enable (EWEN) command. Chip Select is brought high (active), the Start bit and opcode are sent out through the MSSP port. The EWEN command must be given before a write is attempted. The device will be enabled for writes until an Erase/Write Disable command is given or the device is powered down.

**FIGURE 2: ERASE/WRITE ENABLE (EWEN)**

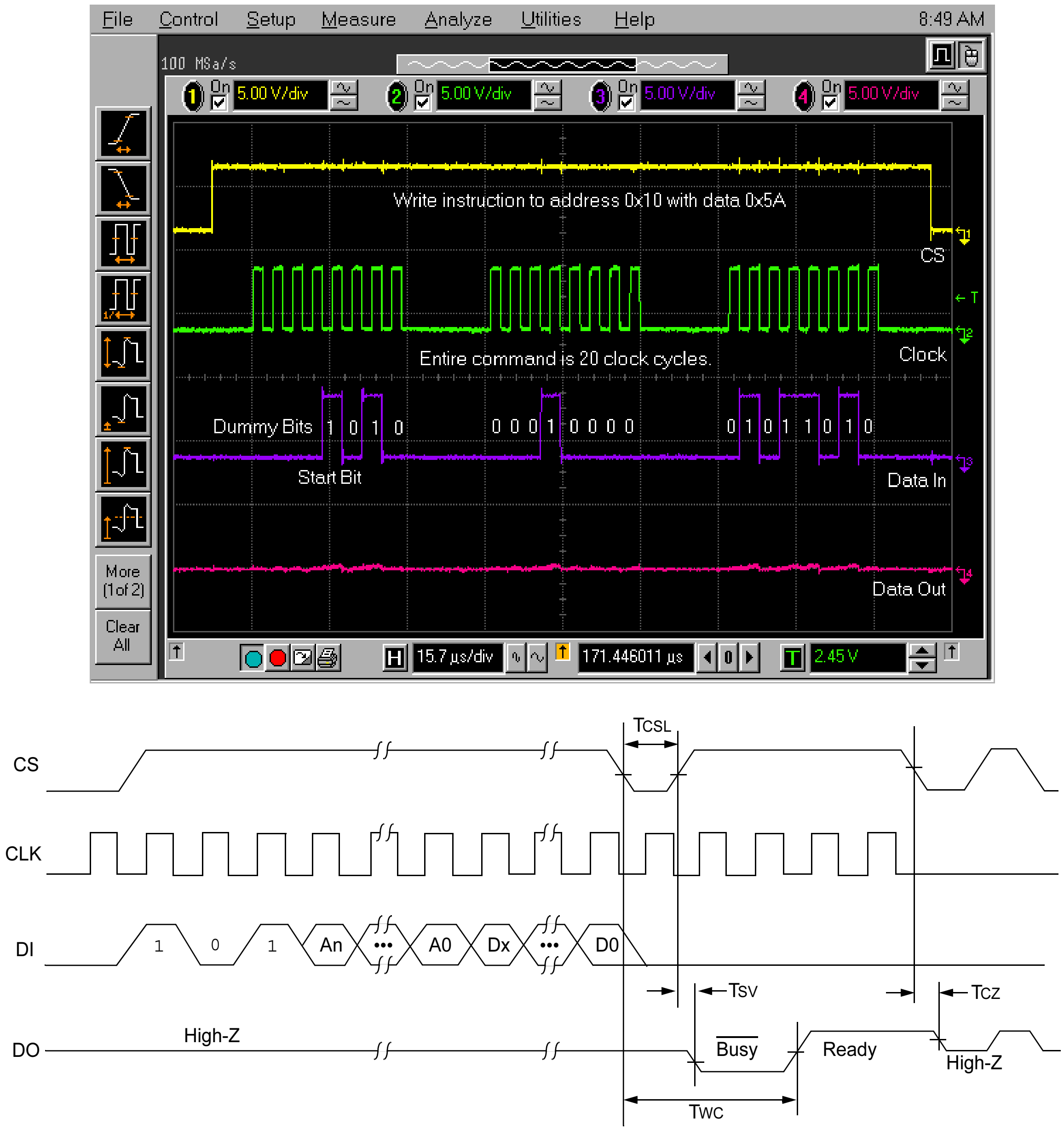


## WRITE COMMAND (START BIT, OPCODE, ADDRESS AND DATA)

Figure 3 shows an example of the Write command. The device is selected and the high byte is sent out which contains the Start bit, opcode and the MSb of the address. The second low byte is sent which contains the rest of the address bits A7-A0. Finally, the data is clocked in, in this case 0x5A. When the Chip Select is toggled, the internal write cycle is initiated.

Once the internal write cycle has begun the Ready/Busy signal can be polled on the DO pin to check when the write finishes. A 6ms delay needs to be added if the Ready/Busy status is not being polled. This code uses Ready/Busy polling.

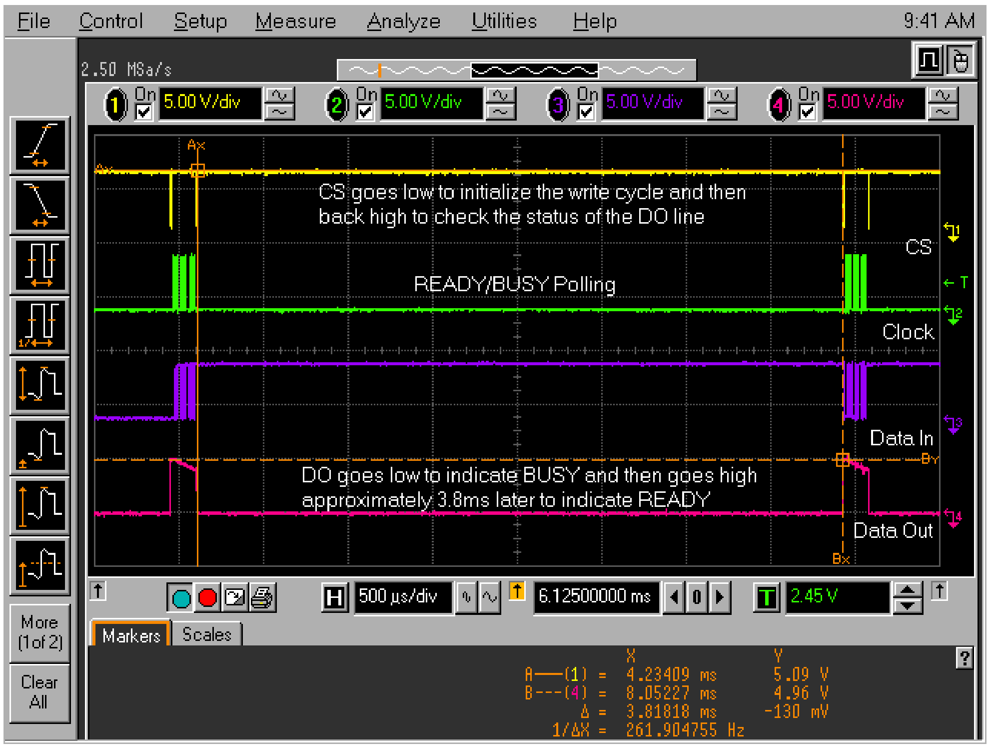
**FIGURE 3: WRITE COMMAND, ADDRESS AND DATA**



## READY/BUSY POLLING

After a valid Write command is given, the DO line of the 93XXXX can be monitored to check if the internal write cycle has been initiated and it can continuously be monitored to look for the end of the write cycle. The oscilloscope plot below shows that the device is selected and the DO line is low for approximately 3.8 ms before the device brings the DO line high, indicating that the write cycle is complete.

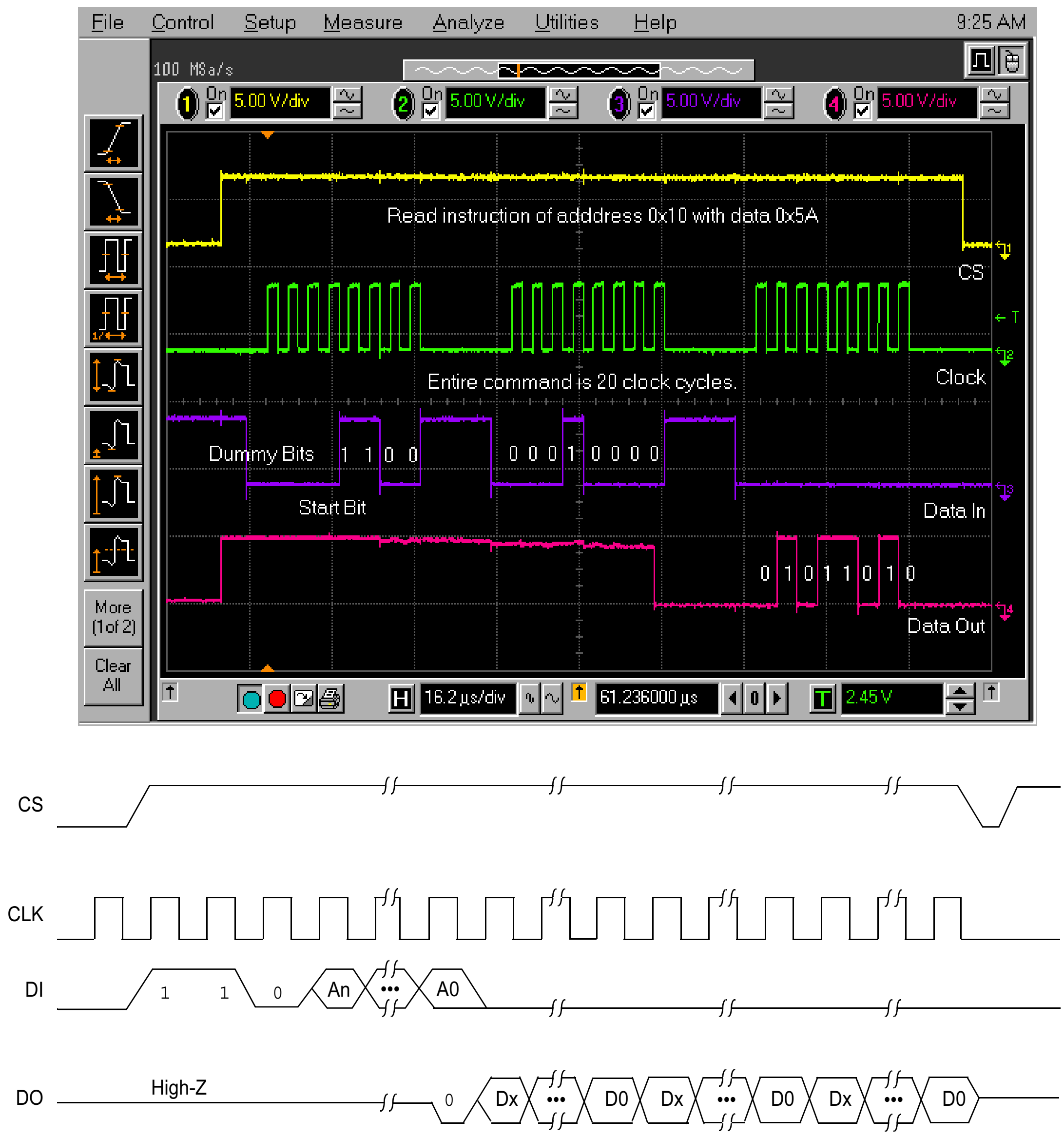
**FIGURE 4: READY/BUSY POLLING**



## READ COMMAND (START BIT, OPCODE, ADDRESS AND DATA)

Figure 5 shows an example of the Read command. The device is selected and the high byte is sent out which contains the Start bit, opcode and the MSb of the address. The second low byte is sent which contains the rest of the address bits A7-A0 (0x10). At this point the device gets ready to send data out. The controller needs to send a dummy byte in order for the clock signals to be sent so the data can be read out of the device and into the microcontroller. In this case, data being read is 0x5A.

**FIGURE 5: READ COMMAND**

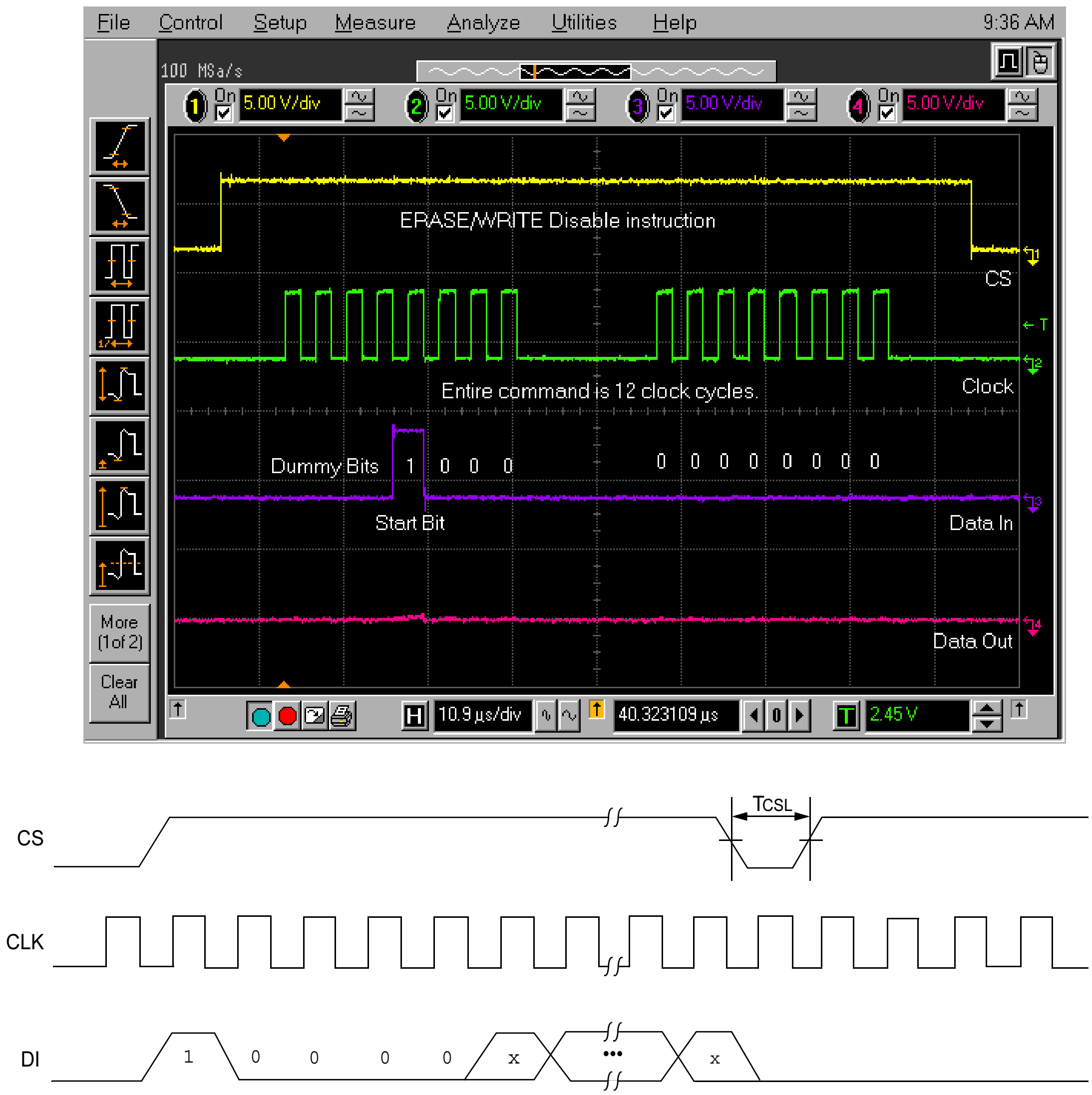


## ERASE/WRITE DISABLE COMMAND

Once the device write is finished, the Write Disable (EWDS) command should be given (see Figure 6). This command consists of a Start bit and the four-bit opcode (0000). Except for the first two high order address bits (A8 and A7), the address bits (set to zeros in this example) are “don’t cares.” Address bits A8 and A7 are used to define the third and fourth opcode bits.

The EWDS command should always be sent to the device after completing a write or prior to powering down the device/system.

**FIGURE 6: ERASE/WRITE DISABLE COMMAND**



## CONCLUSION

These are some of the basic features of Microwire communications using the MSSP module on one of Microchip's mid-range devices. The code is highly portable and can be used on many devices that have the MSSP module with very minor modifications. Using the code provided, designers can begin to build their own Microwire libraries to be as simple or as complex as needed.

The code was tested on Microchip's PICDEM™ 2 Plus Demonstration Board with the connections shown in Figure 1.

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