AN951

Amplifying High-Impedance Sensors – Photodiode Example

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INTRODUCTION

Embedded systems contain many types of sensors, used to sense events in the real world. They can be classified according to the role they play in the analog conditioning circuitry, such as voltage source, current source, resistive and capacitive (frequency-based). This application note discusses the analog conditioning circuit used for high-impedance sensors that act like current sensors.

Current sensors connect to a transimpedance amplifier which converts current to voltage. The design approach illustrated in this application note, using op amps, is broken down into four design steps: DC, stability compensation, closed-loop gain and noise reduction.

A design using a PIN photodiode (light detector) illustrates the principles discussed. Measurement results are provided to support the theory presented.

The last sections of this application note contain supplemental information. The **References** section contains references to pertinent literature, while **Appendix A: "Op Amp Stability Analysis"** covers op amp stability analysis. Finally, **Appendix B: "Set-up Overview"** discusses the tools used to measure the design.

DESIGN

Figure 1 shows the equivalent circuit of a transimpedance amplifier and a high-impedance source. I_S represents the output current of the source. C_S is the sum of the source's output capacitance and the op amp's input capacitance. R_F, with the help of the op amp, converts I_S to a voltage.

At low frequencies, the op amp's inverting input is forced to be at ground potential and I_S must flow through R_F. This combination of effects creates an output voltage of $I_S R_F$.

At higher frequencies, the capacitors will affect the circuit response. The output capacitance of a current sensor has a strong effect on the stability of the op amp feedback loop. Bode plots are aids in both analyzing this effect and in properly compensating the transimpedance amplifier using the capacitor (C_F). The capacitors also limit the bandwidth of the transimpedance amplifier.

R_N and C_N reduce the output noise. The output noise is also kept low by not over-compensating the feedback loop.

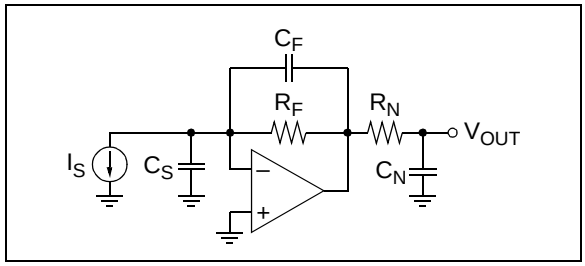

FIGURE 1: *Transimpedance Amplifier Equivalent Circuit.*

Step 1: DC

This design step sets the DC gain and bias point to ensure proper operation. It also addresses DC offsets.

High-impedance sensors have a finite output resistance. The source's output resistance is negligible because it is significantly larger than R_F in most transimpedance amplifier applications.

As explained earlier, the DC output voltage due to the source current will be:

$$V_{OUT} = I_S R_F$$

The op amp will contribute a DC offset voltage to the output:

$$V_{OS} + I_B R_F = \textit{output offset voltage}$$

Where:

V_{OS} = op amp's input offset voltage
I_B = op amp's input bias current

Select the feedback resistor value to give a high gain to I_S. Usually, this gain is high enough to use most of the op amp's output voltage swing when I_S is at its extreme values.

The op amp needs to have V_{OS} and I_B low enough to not cause a large DC offset. Choose an op amp such that:

$$|I_B| + |V_{OS}/R_F| < \textit{acceptable error in } I_S$$

Step 2: Stability Compensation

Transimpedance amplifiers need to be stabilized in many cases. This design step shows how to do this in a relatively straightforward manner.

The result of the circuit in Figure 1 depends on the interaction of C_S, R_F, C_F and the op amp to be stable. Since C_S, R_F and the op amp have already been selected, use C_F to stabilize the transimpedance amplifier. **Appendix A: "Op Amp Stability Analysis"** outlines the theory used in this discussion.

BACKGROUND

The capacitors in Figure 1 (C_S and C_F) lump several physical capacitances together:

- C_{SEN} = sensor's output capacitance
- C_{CM} = op amp's common mode capacitance
- C_{DM} = op amp's differential mode capacitance
- C_C = compensation capacitor (placed in parallel with R_F)
- C_{RF} = R_F's parasitic capacitance
- C_S = $C_{SEN} + C_{CM} + C_{DM}$
- C_F = $C_C + C_{RF}$

The following definitions simplify the description of the op amp's stability:

- f_{GBP} = op amp's Gain Bandwidth Product (GBWP)
- G_{N1} = low-frequency noise gain
  = 1 V/V
- G_{N2} = high-frequency noise gain
  = $1 + C_S/C_F$
- f_{NZ} = noise gain's zero
  = $1 / (2\pi R_F(C_F + C_S))$
- f_{NP} = noise gain's pole
  = $1 / (2\pi R_F C_F)$

The following is an important constraint on these parameters:

$$\frac{f_{NP}}{f_{NZ}} = \frac{G_{N2}}{G_{N1}} \geq 1$$

The noise gain is:

$$G_N(s) = G_{N1}\frac{1 + s/\omega_{NZ}}{1 + s/\omega_{NP}}$$

The op amp's open-loop gain can be approximated as:

$$A(s) \approx \frac{\omega_{GBP}}{s}$$

The crossover frequency (f_{XVR}) is the point where $G_N(2\pi f_{XVR}) = A(2\pi f_{XVR})$. Phase margin is defined at this frequency. Refer to **Appendix A.1 "Loop-Gain"**.

The following sections use Bode plots to describe the stability Figure 1's circuit (see **Appendix A.2 "Bode Plots"** for a discussion of these Bode plots). Note that the design starts with $C_C = 0$.

NOISE GAIN – CASE 1

Figure 2 shows this case defined by the relations:

$f_{NZ} > f_{GBP}$
$f_{XVR} \approx f_{GBP}$

The distinguishing features of this case are:

- This design point is potentially stable
- C_S is relatively small
- $G_N(\omega)$ is constant and equal to G_{N1} at f_{XVR}
- There is a 20 dB/decade difference in slope between |A(f)| and $|G_N(f)|$ at f_{XVR}
- C_C will:
  - Not change when C_S is small enough
  - Increase when the phase margin is low

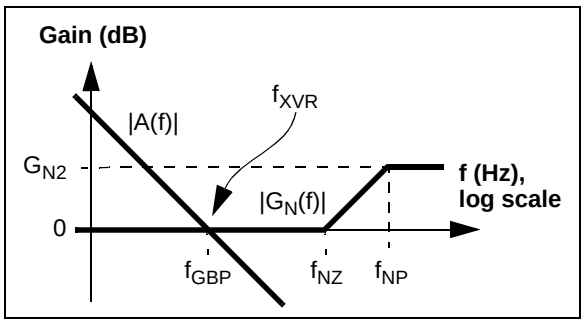

FIGURE 2: *Bode Plot – Case 1.*

NOISE GAIN – CASE 2

Figure 3 shows this case defined by the relations:

$$f_{NZ} < f_{GBP}$$
$$f_{NP} > f_{GBP}/G_{N2}$$
$$f_{XVR} \approx (f_{NZ}f_{GBP})^{1/2}$$

The distinguishing features of this case are:

- This design point has poor stability
- C_S is neither small nor large
- $G_N(\omega)$ is increasing and has a value between G_{N1} and G_{N2} at f_{XVR}
- There is a 40 dB/decade difference in slope between |A(f)| and $|G_N(f)|$ at f_{XVR}
- C_C must increase to:
  - Improve the phase margin
  - Correct the difference in slope

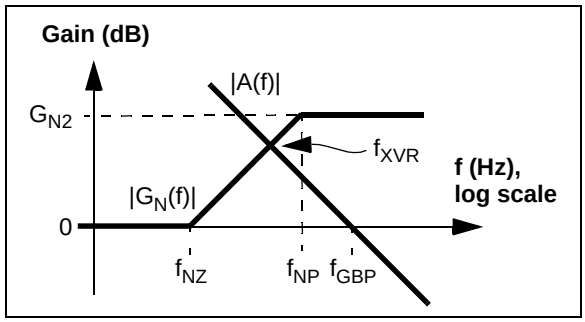

FIGURE 3: *Bode Plot – Case 2.*

NOISE GAIN CASE – 3

Figure 4 shows this case defined by the relations:

$$f_{NP} < f_{GBP}/G_{N2}$$
$$f_{XVR} \approx f_{GBP}/G_{N2}$$

The distinguishing features of this case are:

- This design point has good stability
- C_S is relatively large
- $G_N(\omega)$ is constant and equal to G_{N2} at f_{XVR}
- There is a 20 dB/decade difference in slope between |A(f)| and $|G_N(f)|$ at f_{XVR}
- C_C will:
  - Not change when it is small enough
  - Decrease to improve noise performance when $f_{NP} << f_{GBP}/G_{N2}$ (but the condition $f_{NP} < f_{GBP}/G_{N2}$ must still hold)

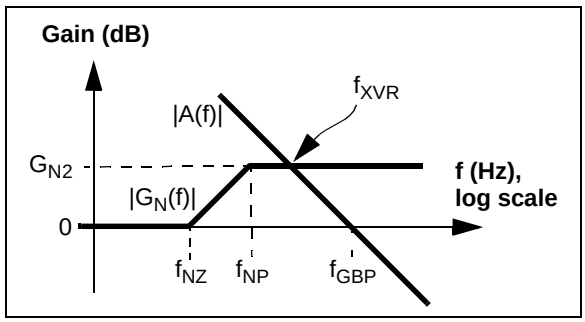

FIGURE 4: *Bode Plot – Case 3.*

SELECTING THE COMPENSATION CAPACITOR

The noise gain case is important in choosing the compensation capacitor (C_C). For Case 1 (Figure 2), there may not be a need to add compensation. In all other cases, C_C needs to be large enough to keep the transimpedance amplifier stable. This means that f_{NP} needs to be less than f_{XVR} (see Figure 4). To minimize output noise, choose C_C small enough to make f_{NZ} as large as possible. The following equations produce a design that meets these criteria:

$$C_C = 0, \quad f_{NZ} > 10f_{GBP}$$
$$C_C \approx 2\,(1/(2\pi\, f_{XVR}R_F)) - C_{RF}, \quad f_{NZ} < 10f_{GBP}$$

Now re-calculate C_F, G_{N2}, f_{NZ} and f_{XVR}. The final Bode plot should be like Figure 4.

The -3 dB bandwidth is approximately f_{XVR} when C_C is chosen as described above.

LOOP-GAIN SIMULATION

Microchip's op amp macro models (available at www.microchip.com) are a tool to simulate the loop-gain response. **Appendix A.4 "Loop-Gain Simulation"** has a circuit for simulating loop-gain.

Step 3: Closed-Loop Gain

A stable transimpedance amplifier does not always behave exactly as desired. This design step discusses how to adjust the performance without losing stability performance.

Figure 5 shows the closed-loop response for a representative design. It shows two different cases: before compensation ($C_C = 0$) and after compensation ($C_C > 0$). The gain-peaking shown in the before case corresponds to significant step response overshoot and ringing. The after-compensation curve corresponds to a step response with little overshoot or ringing.

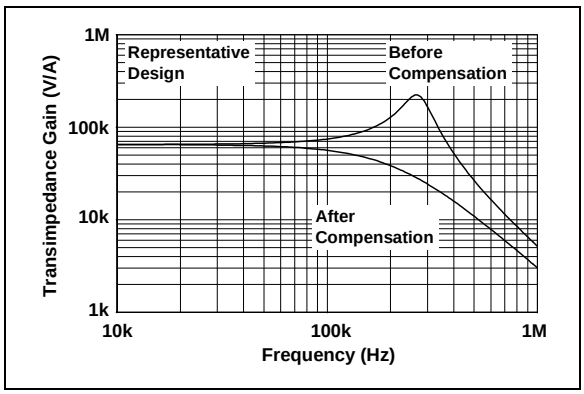

FIGURE 5: *Closed-Loop Gain.*

Use Microchip's op amp macro models (available at www.microchip.com) to simulate the closed-loop gain in SPICE and to refine the response. Increasing C_C will reduce the bandwidth and gain-peaking. Increasing C_C too much may cause f_{NZ} to be too low, which can cause the output noise to be too high within the bandwidth of interest.

If the final closed-loop bandwidth is too low, try the following remedies:

- Select a faster op amp
- Use a feedback resistor with lower parasitic capacitance (e.g., a SMD 0603 resistor)
- Bias the high-impedance sensor for lower capacitance (e.g., reverse bias a photodiode)
- Reduce the transimpedance gain (R_F)

Step 4: Noise Reduction

The last design consideration is the amount of random noise at the transimpedance amplifier's output. This can usually be improved with some simple steps.

The most important thing to do is to maximize R_F; as much of the transimpedance gain as possible needs to be developed across this resistor. It is possible to add more gain with subsequent stages, but the noise performance will not be as good.

Choosing an op amp with low noise voltage density and noise current density is also important.

Reducing the overall signal bandwidth with the RC low-pass filter (R_N and C_N) can help. The pole set by this output filter is:

$$f_{RCN} = \frac{1}{2\pi R_N C_N}$$

If possible, set f_{RCN} lower than the noise gain's zero (f_{NZ}). This will overcome the increase in output noise voltage density caused by the increase in noise gain with frequency.

EXAMPLE CIRCUIT

Figure 6 is a circuit that was built for demonstration purposes (see Figure B-1 in **Appendix B: "Set-up Overview"**). The photodiode D_1 is biased in Photovoltaic mode to minimize its noise and DC errors. The output needs to go almost rail-to-rail in order to drive an A/D Converter (ADC) on a PICmicro® microcontroller.

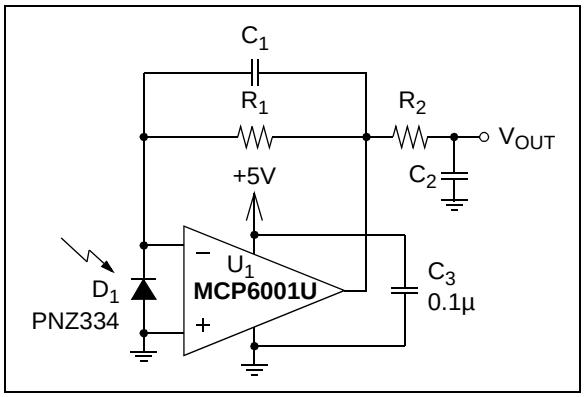

FIGURE 6: *Transimpedance Amplifier.*

Design Before Stability Compensation

D_1 is the Panasonic® PNZ334 PIN photodiode [2]. Its C_{SEN} is roughly 24 pF with 0V reverse bias. The maximum output current (I_S) is 70 µA when the input illuminance is 10,000 lx. The minimum I_S is 0 µA when the input illuminance is 0 lx. The output current is reasonably linear with the input illuminance.

The MCP6001U op amp [3] comes in a SOT-23-5 package to conserve space. It has the specifications f_{GBP} = 1 MHz, C_{DM} = 3 pF and C_{CM} = 6 pF. It has a CMOS input stage with very small bias current at room temperature.

All of the resistors and capacitors are SMD 0805.

R_1 is 64.9 kΩ so that $V_{OUT} \approx 4.5V$ is at the maximum I_S and $V_{OUT} \approx 0V$ is at the minimum I_S. Since it is a SMD 0805 metallic resistor, C_{RF} is approximately 0.2 pF.

C_3 is a 0.1 µF capacitor for good supply bypass performance.

The performance before compensation is approximately:

$$C_S = 24\text{ pF} + 3\text{ pF} + 6\text{ pF} = 33\text{ pF}$$
$$C_F = 0\text{ pF} + 0.2\text{ pF} = 0.2\text{ pF}$$
$$G_{N1} = 1\text{ V/V}$$
$$G_{N2} = 1 + (33\text{ pF})/(0.2\text{ pF}) = 166\text{ V/V}$$
$$f_{NZ} = 1/(2\pi(64.9\text{ k}\Omega)(33\text{ pF} + 0.2\text{ pF})) = 73.9\text{ kHz}$$
$$f_{NP} = 1/(2\pi(64.9\text{ k}\Omega)(0.2\text{ pF})) = 12.2\text{ MHz}$$
$$f_{XVR} \approx ((73.9\text{ kHz})(1.0\text{ MHz}))^{1/2} = 272\text{ kHz}$$

This corresponds to Case 2 (Figure 3); the compensation capacitor C_C (C_1) needs to increase.

Design After Stability Compensation

The design value for C_1 is:

$$C_1 \approx 2\,(1/(2\pi\,(272\text{ kHz})(64.9\text{ k}\Omega))) - (0.2\text{ pF})$$
$$= 17.8\text{ pF}$$

Choosing the nearest standard value of 18 pF gives the updated values:

$$C_F = 18\text{ pF} + 0.2\text{ pF} = 18.2\text{ pF}$$
$$G_{N2} = 1 + (33\text{ pF})/(18.2\text{ pF}) = 2.81\text{ V/V}$$
$$f_{NZ} = 1/(2\pi(64.9\text{ k}\Omega)(33\text{ pF} + 18.2\text{ pF})) = 47.9\text{ kHz}$$
$$f_{NP} = 1/(2\pi(64.9\text{ k}\Omega)(18.2\text{ pF})) = 135\text{ kHz}$$
$$f_{XVR} \approx (1.0\text{ MHz})/(2.81\text{ V/V}) = 356\text{ kHz}$$

This corresponds to Case 3 (Figure 4), so the stability is good. Also, f_{NP} and f_{GBP}/G_{N2} are not far apart, so the noise performance will be reasonable.

Noise Reduction Design

Select R_2 and C_2 for both noise performance and as an anti-aliasing filter for the A/D converter. The cutoff frequency needs to be below the noise gain zero (f_{NZ}) at 48 kHz. The Nyquist rate is 2.5 kHz since the A/D sample rate is 5 kSPS. Setting the low-pass pole near 500 Hz achieves both goals.

$$R_2 = 10.0\text{ k}\Omega$$
$$C_2 \approx 1/(2\pi(500\text{ Hz})(10.0\text{ k}\Omega)) = 32\text{ nF}$$

Choosing the nearest standard value of 33 nF gives:

$$f_{RCN} = 1/(2\pi(10.0\text{ k}\Omega)(33\text{ nF})) = 482\text{ Hz}$$

Table 1 summarizes the final design values for the components in Figure 6.

TABLE 1: COMPONENTS

Component	Value/Part No.	Size/Package
C_1	18 pF, ±5%	SMD 0805
C_2	33 nF, ±10%	SMD 0805
C_3	0.1 µF, ±10%	SMD 0805
D_1	PNZ334 Panasonic	Plastic Through-hole, 100 mil pitch
R_1	64.9 kΩ, ±1%	SMD 0805
R_2	10.0 kΩ, ±5%	SMD 0805
U_1	MCP6001U	SOT-23-5

Measured Transimpedance Gain

Figure 7 shows the circuit used to measure the transimpedance amplifier's frequency response. The input source V_X was arbitrarily chosen to be a 10 V_{P-P} sinewave. The resistor R_X was 10.0 MΩ and its parasitic capacitance (C_X) was measured to be 0.15 pF using a HP4285A LCR meter. To avoid output clipping, the photodiode was placed close enough to a lamp to bias the output voltage (V_Y) to 202 mV.

The current injected into the transimpedance amplifier by V_X and R_X is:

$$I_X \approx (V_X / R_X)\,(1 + sR_XC_X)$$
$$\approx (1\ \mu A_{P-P})\,(1 + s/(2\pi(106\text{ kHz})))$$

The measured transimpedance gain under these conditions, in units of V/A, is:

$$V_Y/I_X \approx V_Y / [(1\ \mu A_{P-P})\,(1 + s/(2\pi(106\text{ kHz}))]$$

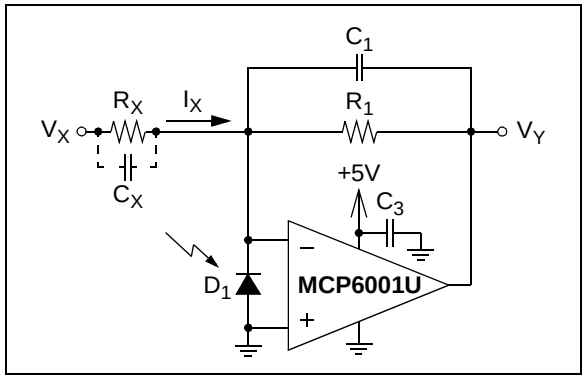

FIGURE 7: *Measuring Transimpedance Gain.*

Figure 8 shows the measured results. The uncompensated curve ($C_1 = 0$) has 7.4 dB of peaking, which indicates severe stability problems for this type of circuit. The compensated curve ($C_1 = 18$ pF) has 0.1 dB of peaking; it will have a good step response.

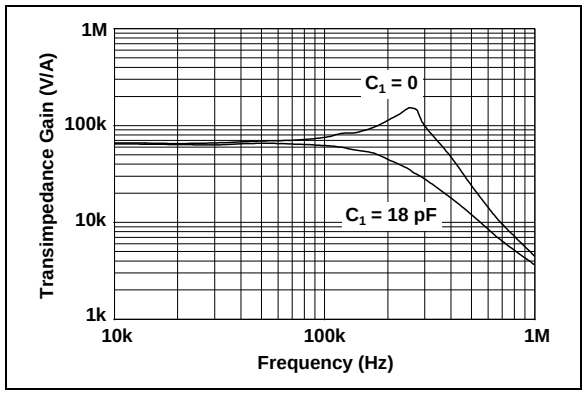

FIGURE 8: *Gain vs. Frequency.*

Measurement Data

Two different measurements were made under the following conditions:

- Sample rate = 5.0 ksps (kilo samples per second)
- Number of samples = 8192
- A/D converter = 10-bit on the PIC16F684
- V_{DD} = 5.0V
- Boards and software described in **Appendix B: "Set-up Overview"**

The measured illuminance for the circuit can be calculated with:

L = illuminance (lx)

= (V_{OUT}/R_1) (10,000 lx / 70 µA)

The Panasonic photodiode's data sheet [2] shows variation in the photocurrent over process and temperature. The following estimates were made based on that data.

There is an approximate ±30% variation in photocurrent (I_S) over process at 25°C. Typically, there is a -15% to +50% variation in I_S over temperature (-25°C to +85°C). This means that accurate measurements require calibration for both process and temperature variations.

R_1's tolerance (1%) also affects the V_{OUT} measurement accuracy. This error is much smaller than the photodiode error and can be corrected with the same calibration routine.

INCANDESCENT LAMP

The histogram in Figure 9 shows data taken near an incandescent lamp powered by a battery. The average output was 366.7 LSb, or 1.791V. The output RMS error (standard deviation) was 0.47 LSb_{RMS}, or 2.3 mV_{RMS}. This compares favorably with the ideal ADC error of 1.4 mV_{RMS}. The estimated illuminance is 3942 lx, with an RMS error of 5 lx_{RMS}. The circuit was not calibrated for absolute accuracy.

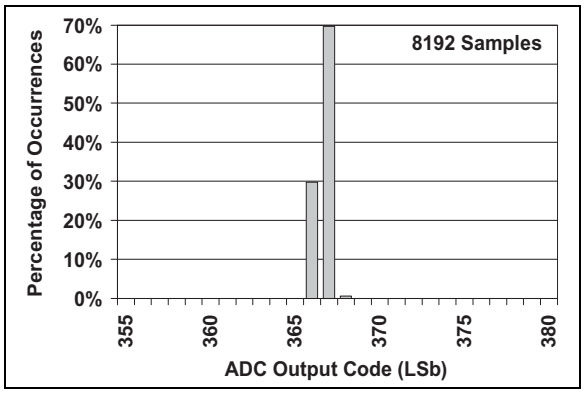

FIGURE 9: *ADC Output Codes.*

FLUORESCENT LAMP

The histogram in Figure 10 shows data taken near a fluorescent lamp. The average output was 176.7 LSb (or 0.863V). The output RMS error (standard deviation) was 8.10 LSb_{RMS} (or 39.6 mV_{RMS}). This is much larger than the ideal ADC error of 1.4 mV_{RMS}. The estimated illuminance is 1900 lx, with an RMS error of 87 lx_{RMS}. The circuit was not calibrated for absolute accuracy.

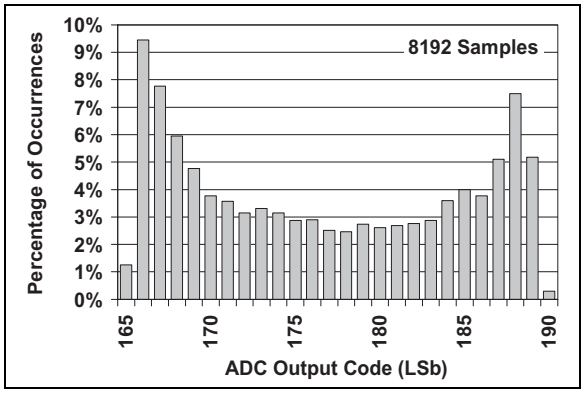

FIGURE 10: *ADC Output Codes.*

The histogram's shape (Figure 10) indicates the presence of an interfering sine wave. An FFT plot of the sampled data showed that most of the energy is at 120 Hz. This corresponds to the fluorescent lamp's ballast "zero crossover" phenomenon. Averaging measurements in a PICmicro® microcontroller is one way to reduce the 120 Hz noise.

SUMMARY

High-impedance current sensors often connect to a transimpedance amplifier in order to convert current to voltage while maintaining good noise performance. An ADC can then convert the signal to the digital domain. This application note uses an op amp to implement the transimpedance amplifier. The design approach shown in this application note uses four steps: DC, stability compensation, closed-loop gain and noise reduction. A circuit using a PIN photodiode illustrates this approach.

REFERENCES

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APPENDIX A: OP AMP STABILITY ANALYSIS

Figure A-1 shows a general op amp circuit with arbitrary impedances (Z_S and Z_F) in the feedback loop. The output voltage is a function of input voltages (V_M and V_P), the feed-forward path they take to the output (V_{OUT}) and the behavior of the feedback loop. This appendix focuses on the feedback loop’s behavior and how it relates to stability. See [1, 4, 5, 6, 7] for background information on compensating op amp circuits.

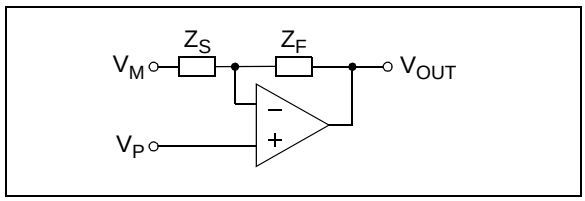

FIGURE A-1: *General Op Amp Circuit.*

A.1 Loop-Gain

To analyze this op amp’s feedback loop, first break the loop at the output pin, as shown in Figure A-2. Then inject a signal (V_X) into the feedback network. The loop-gain is the negative of the total gain around the broken loop ($-V_{OUT}/V_X$):

$$T(s) = \beta(s)A(s)$$

Where:

$\beta(s)$ = feedback gain = $Z_S / (Z_S + Z_F)$

A(s) = op amp’s open loop gain

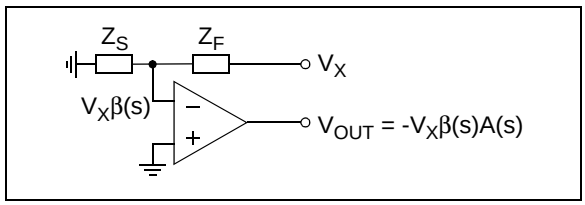

FIGURE A-2: *Analyzing the Loop-gain.*

All closed-loop transfer functions have the denominator:

$$D(s) = 1 + T(s)$$

To ensure stable negative feedback, this denominator must meet the criteria:

$$\angle T(f_{XVR}) > -180°$$
$$|T(f_{180})| < 0db$$

Where:

$|T(f_{XVR})| = 0$ dB

$\angle T(f_{180}) = -180°$

and the phase $\angle T(f)$ is continuous (it starts at 0° at 0 Hz and has no 360° jump discontinuities).

The commonly used measures of stability are Phase Margin (PM) and Gain Margin (GM). They measure how strong the above inequalities are:

$PM = \angle T(f_{XVR}) + 180°$

$GM = -|T(f_{180})|$, in units of dB

Figure A-3 shows the loop-gain magnitude and phase, and visually depicts GM and PM.

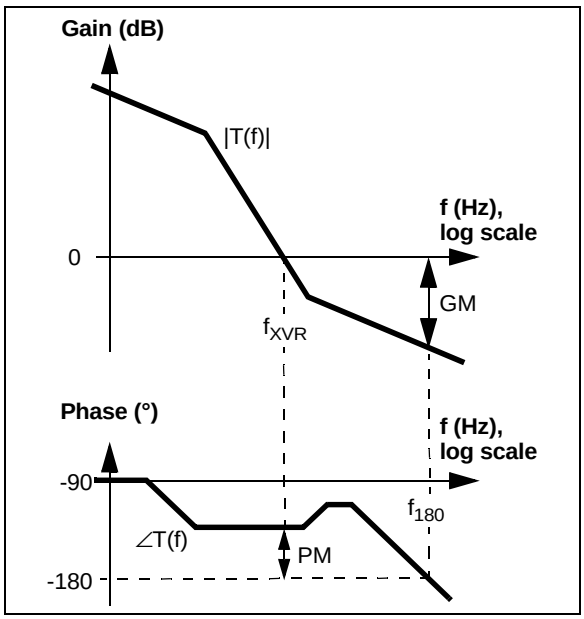

FIGURE A-3: *Loop-gain.*

The larger (more positive) both GM and PM are, the more stable the feedback loop is. For most op amp applications, keep PM > 60° and GM > 10 dB.

A.2 Bode Plots

It is easier to analyze and stabilize the feedback loop by showing the op amp and feedback network effects separately. It is also more convenient to use the noise gain instead of the feedback gain. The noise gain is the reciprocal of the feedback gain and describes the gain from a source at the op amp's non-inverting input to its output.

$G_N(s) = 1/\beta(s)$

$= 1 + Z_F/Z_S$

The Bode plot in Figure A-4 accomplishes these goals (it is the same case as shown in Figure A-3).

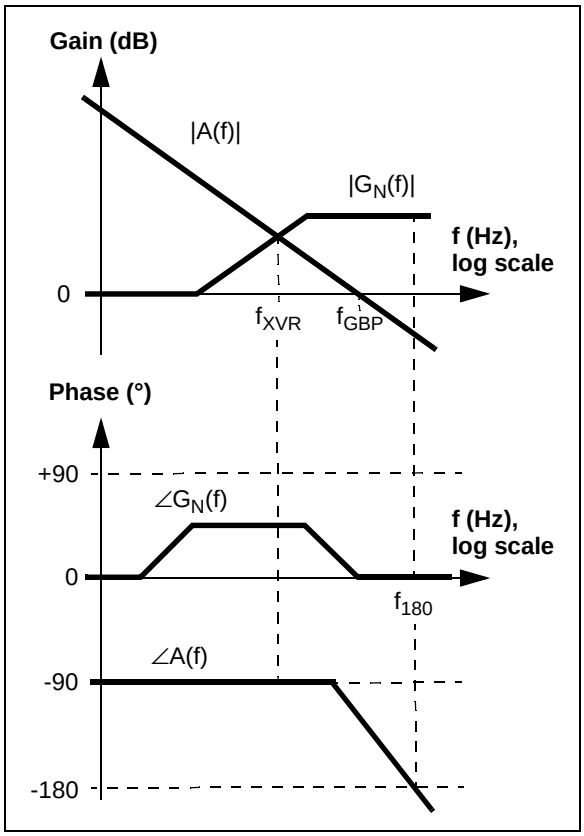

FIGURE A-4: *Bode Plot.*

The individual gains relate to the loop-gain as follows:

$|T(f)| = |A(f)| - |G_N(f)|$, in units of dB

$\angle T(f) = \angle A(f) - \angle G_N(f)$, in units of ° (degrees)

The op amp's open-loop gain is usually plotted in the data sheet against frequency. The phase response is of special interest in the Bode plot.

The crossover frequency (f_{XVR}) is the point where $|A(f)|$ and $|G_N(f)|$ are equal in magnitude and is easy to find in this plot. The phase at this frequency ($\angle T(f_{XVR})$) determines the phase margin.

$$PM = \angle A(f_{XVR}) - \angle G_N(f_{XVR}) + 180°$$

The frequency at -180° phase (f_{180}) is the point where $\angle A(f) - \angle G_N(f)$ is -180°. The gain at this frequency ($|T(f_{180})|$) determines the gain margin.

$$GM = -(|A(f_{180})| - |G_N(f_{180})|), \text{ in units of dB}$$

As a rule of thumb, design the feedback network so that the difference in slope between $|A(f)|$ and $|G_N(f)|$ is 20 dB/decade at f_{XVR}. In Figure A-4, $|A(f)|$ has a slope of -20 dB/decade and $|G_N(f)|$ has a slope of +20 dB/decade, at f_{XVR}. The difference in slope is thus 40 dB/decade (noise gain case 2), indicating a poor design.

A.3 Stabilization of Feedback

One way to stabilize an op amp feedback circuit is to make the noise gain ($G_N(f)$) have a slope of 0 dB/decade at f_{XVR}. Most op amp circuits use a constant noise gain, which correctly sets this slope. Figure A-4 can be stabilized by making the noise gain pole occur at a lower frequency than f_{XVR}. This is the method used in this application note.

Another method to stabilize an op amp feedback circuit is to modify the phase, but not the magnitude, of the noise gain at f_{XVR}. Zeros and/or poles are added to the noise gain (or moved in frequency) above f_{XVR}. This approach is not used in this application note.

A.4 Loop-Gain Simulation

An easy way to simulate loop-gain in SPICE is shown in Figure A-5. The AC source (V_{AC}) provides the energy to make the voltages in the loop non-zero. The negative of the ratio of the resulting voltages on either side of the AC source ($-V_B/V_A$) is the loop-gain, and is easily calculated from the simulation results. Note that V_{AC} is not part of the loop-gain calculations; it is only used to disturb the closed feedback loop. Also, a unity-gain buffer would be simulated by setting $Z_F = 0$ and removing (opening) Z_S.

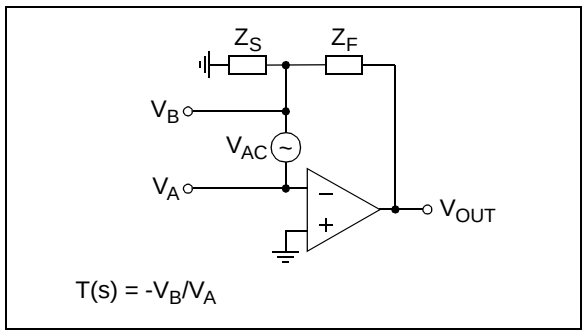

FIGURE A-5: *Simulating the Loop-gain.*

APPENDIX B: SET-UP OVERVIEW

B.1 Photodiode PGA PICtail™ Daughter Board

The Photodiode PGA PICtail™ Daughter Board contains the analog circuitry represented in Figure B-1. Light incident to the photodiode is converted to current. The op amp converts current to voltage (transimpedance amplifier). This voltage is sent to the CH0 input of the PGA. The PGA gains and buffers this output, which is sent off board (V_{OUT}). Board power is applied at the +5V and GND inputs. The Serial Peripheral Interface (SPI™) bus makes it possible to control the PGA; its gain and input channel can be set as desired from the software.

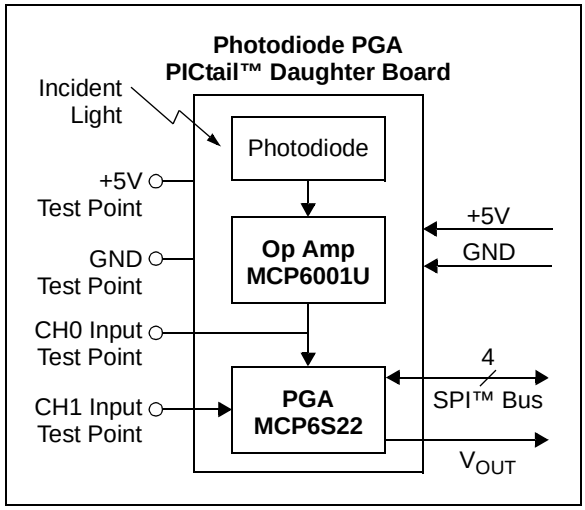

FIGURE B-1: *Photodiode PGA PICtail™ Daughter Board Block Diagram.*

The test points make it easier to test key points in the circuit, change the input signals and to use this board as a stand-alone board.

- GND Test Point – Connected to the ground plane and is a convenient ground point for any lab equipment
- +5V Test Point – Allows measurement of the positive supply voltage and provides a means to power this board with a laboratory power supply
- CH0 Test Point – Is the place to measure the transimpedance amplifier's output voltage (also the PGA's CH0 input)
- CH1 Test Point – Makes it possible to send any desired signal to the PGA

More detail on setting up this demonstration board can be found in the Photodiode PGA PICtail™ Daughter Board User's Guide (DS51514A) [11].

B.2 Associated Tools

Figure B-2 shows the block diagram of the hardware and software tools that the Photodiode PGA PICtail™ Daughter Board is designed to work with. More information on these tools can be found in the **"References"** section.

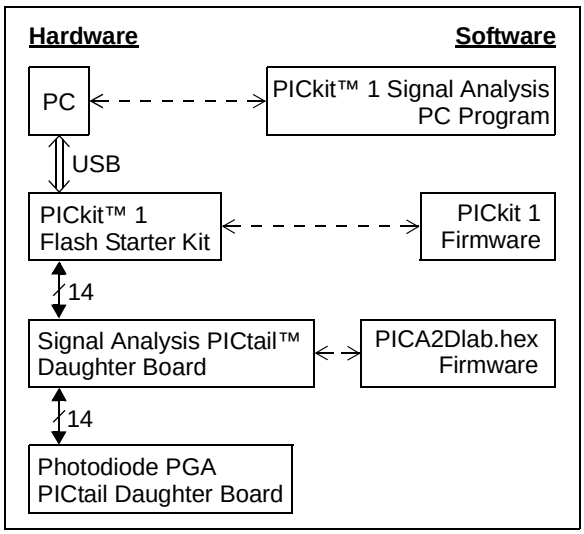

FIGURE B-2: *Measurement Set-up Block Diagram.*

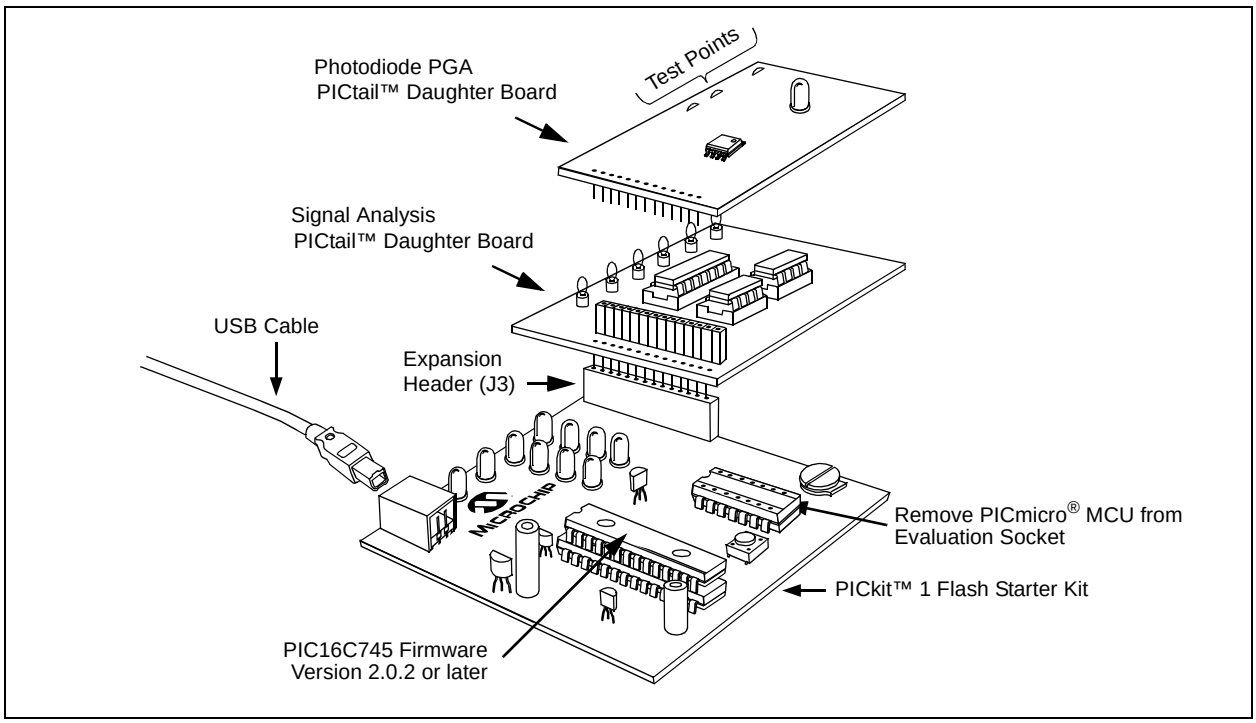

FIGURE B-3: *Board Connections.*

B.2.1 PC PLATFORM

The Personal Computer (PC) shown in Figure B-2 needs to run on Windows® 98 SE or later. It provides a convenient interface for the user, communicates with the other boards and provides power through the USB connection.

B.2.2 PICkit™ 1 SIGNAL ANALYSIS PC PROGRAM

The PICkit™ 1 Signal Analysis PC program configures and programs the PIC16F684 PICmicro® microcontroller on the Signal Analysis PICtail Daughter Board through the USB port on the PICkit 1 Flash Starter Kit. It also imports data through the same connection and displays the data in strip-chart, histogram, FFT plot and oscilloscope plot formats. Data can be output in CSV format for importing into a spreadsheet program.

B.2.3 PICkit 1 FLASH STARTER KIT

The PICkit 1 Flash Starter Kit (DV164101) programs PICmicro microcontrollers using the PIC16C745's USB port to communicate with the PICkit 1 Signal Analysis PC program. It connects to the Signal Analysis PICtail Daughter Board via a header (see Figure B-3).

This board provides a single +5V supply voltage for the daughter boards. It can drive up to 5 µF on the supply; a larger capacitance may interfere with program timing.

B.2.4 PICkit 1 FIRMWARE

This software resides on the PICkit 1 Flash Starter Kit's PIC16C745 microcontroller. Use version 2.0.2 or later.

B.2.5 SIGNAL ANALYSIS PICtail DAUGHTER BOARD

This board is Microchip Development Tool AC164120. It connects to the PICkit 1 Flash Starter Kit, which it uses for power and a communications link to the PC. The on-board PIC16F684 has a 10-bit ADC, which converts the Photodiode PGA PICtail™ Daughter Board's output voltage. The results are temporarily stored on the board's 25LC640 serial EEPROM chips.

The +5V single-supply voltage from the PICkit 1 Flash Starter Kit board is bypassed with a bulk 1 µF capacitor and local 0.1 µF capacitors for each IC.

B.2.6 FIRMWARE FOR THE SIGNAL ANALYSIS PICtail DAUGHTER BOARD

"PICA2Dlab.hex" is the standard file that supports the PICkit™ 1 Signal Analysis PC program. The PGA and 10-bit ADC configuration are selected in the Signal Analysis PC program and written to the PIC16F684. The PIC16F684 then sends the command(s) over the SPI™ bus to the PGA.

B.2.7 INTERFACE DETAILS

A more detailed look at how the Photodiode-PGA PICtail Daughter Board interfaces with the other boards is shown in Figure B-4.

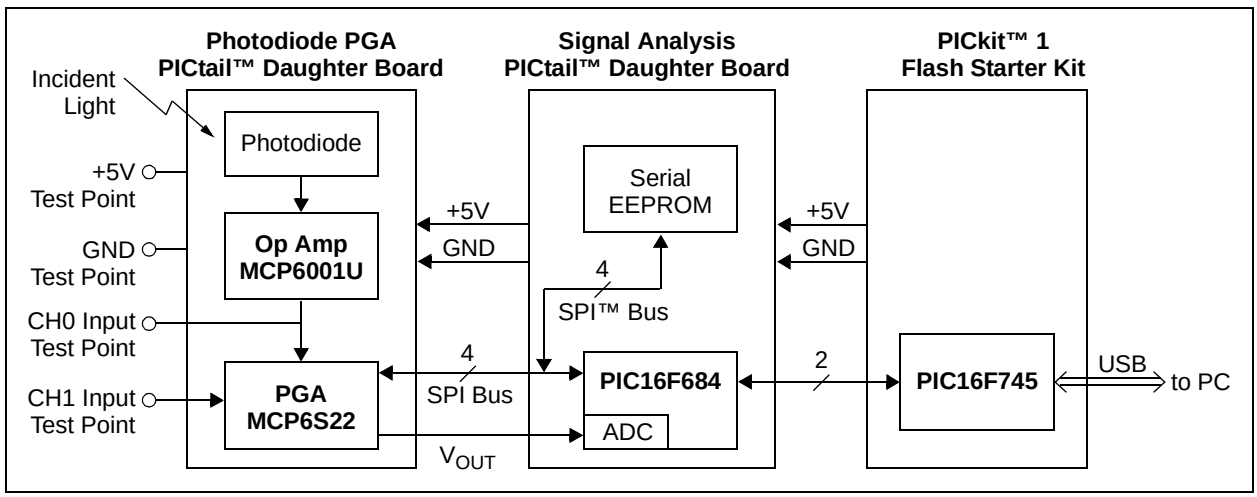

FIGURE B-4: *Detailed Interface Diagram.*

NOTES:

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