AN915

1K, 2K and 4K Microwire EEPROM Migration

Author: *Ken Dietz*
Microchip Technology Inc.

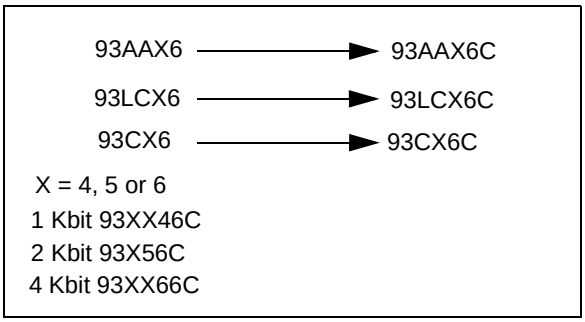
INTRODUCTION

Microchip Technology recently introduced a new family of Microwire serial EEPROMs with smaller packaging, faster write times, and faster bus speeds. In addition to this migration document, we recommend that you review the data sheets for each device to see how these changes may apply to your system requirements. This document is intended to assist customers with migrating to the latest Microchip Technology Microwire EEPROMs from older versions of our products.

This document addresses migration of 93XX46, 93XX56, and 93XX66 devices with a selectable ORG pin to 93XX46C, 93XX56C, and 93XX66C components, respectively. There are six topics addressed throughout this text:

- Bus Speed Compatibility
- Write Cycle Time
- Write Cycle Initiation
- Ready/$\overline{\text{Busy}}$ Operations
- Noise Immunity
- New Packaging Options

FIGURE 1: RECOMMENDED MIGRATION PATHS



BUS SPEED COMPATIBILITY

When the power supply applied to the chip is below 4.5 Volts, the new 93LCX6C devices can run up to 2 MHz as opposed to the 1 MHz bus speed of 93LCX6 devices.

WRITE CYCLE TIME

Write cycle time is also a key specification for system designers. Many of these specifications remained the same for the recommended migration paths, and some improved. Differences between the families are noted in Table 1.

TABLE 1: WRITE CYCLE TIME DIFFERENCES

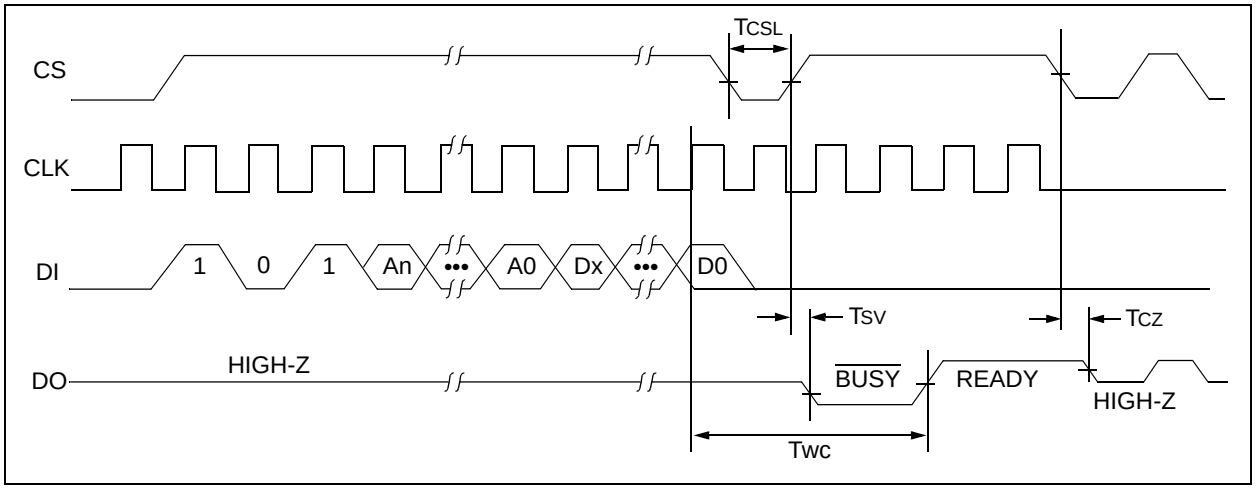
Old Part Number	Old Spec. (Maximum)	New Part Number	New Spec. (Maximum)
93CX6	10 ms	93CX6C	2 ms
93AAX6	10 ms	93AAX6C	6 ms
93LCX6	10 ms	93LCX6C	6 ms

X = 4, 5 or 6

INITIATING WRITE CYCLES

Depending on the migration path taken, write cycle initiation may have also changed. Almost all of the methodologies remained the same. However, those that did change were limited to 93CX6 devices when migrating to the 93CX6C Family. For older devices, 93CX6, the write cycle initiated after the last data bit. On the newer devices, the write cycle now initiates on the rising edge of the last data bit clock. The latest waveform is shown in Figure 2 and the timing characteristics for each symbol can be found in the respective data sheets. This change does not effect 93AAX6 or 93LCX6 devices.

FIGURE 2: 93CX6C WRITE CYCLE TIMING



READY/$\overline{\text{BUSY}}$ OPERATIONS

Ready/$\overline{\text{Busy}}$ signals have also changed between the older and newer devices. Microwire EEPROMs use three different methods to observe Ready/$\overline{\text{Busy}}$ operations. These three methods are summarized as follows:

1: Chip Select must be cycled from **low-to-high** prior to the completion of a write cycle in order to observe the Ready/$\overline{\text{Busy}}$ transitions. The Ready/$\overline{\text{Busy}}$ signal remains high for the device under test until the next Start bit, once this waveform is realized.

2: Chip Select must be cycled from **high-to-low-to-high** prior to the completion of a write cycle in order to observe the Ready/$\overline{\text{Busy}}$ transitions. The Ready/$\overline{\text{Busy}}$ signal remains high for the device under test until the next Start bit, once this waveform is realized.

3: Chip Select must be cycled from **low-to-high** prior to the completion of a write cycle in order to observe the Ready/$\overline{\text{Busy}}$ transitions. The Ready/$\overline{\text{Busy}}$ signal remains in a high-impedance state for the device under test until the next Start bit, once this waveform is realized. **This property enables designers to tie the data-in and data-out pins together in a circuit.**

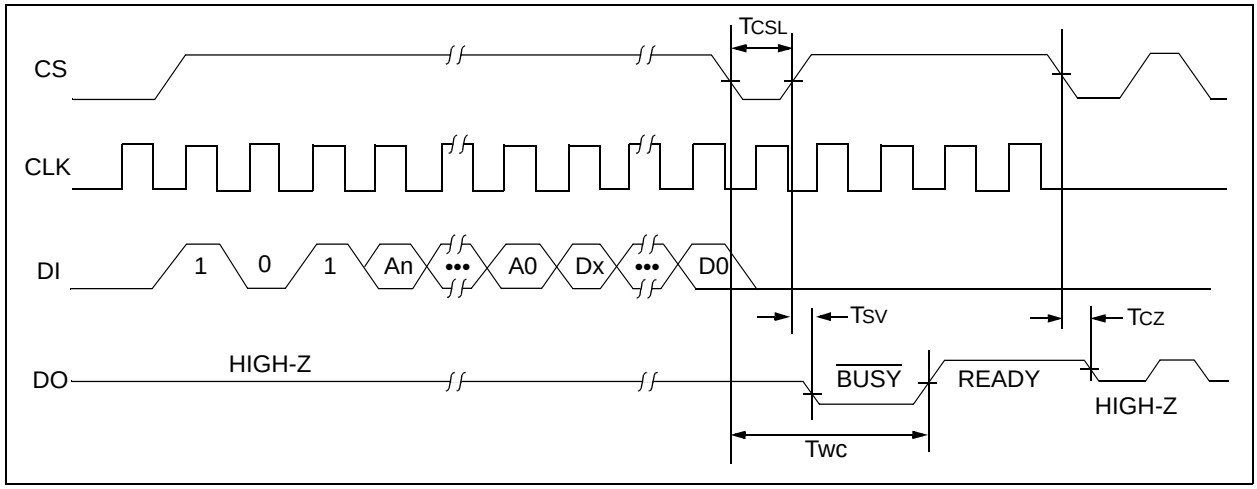
Table 2 shows the Ready/$\overline{\text{Busy}}$ polling method for each device. Ready/$\overline{\text{Busy}}$ operations for 93CX6C devices are shown in Figure 2, and Ready/$\overline{\text{Busy}}$ operations for 93AAX6C/93LCX6C devices are shown in Figure 3. These diagrams are also provided within the respective EEPROM data sheets.

TABLE 2: READY / $\overline{\text{BUSY}}$ OPERATIONAL CHANGES

Old Part Number	Old Ready/$\overline{\text{Busy}}$ Method	New Part Number	New Ready/$\overline{\text{Busy}}$ Method
93CX6	3	93CX6C	2
93AAX6	3	93AAX6C	1
93LCX6	3	93LCX6C	1

X = 4, 5 or 6

FIGURE 3: 93AAX6C/93LCX6C WRITE CYCLE TIMING



NOISE IMMUNITY

Circuitry has been implemented on the new 93XXX6C devices to improve noise spike rejection. One circuit has been added to each input for CS, DI and CLK.

NEW PACKAGING OPTIONS

With the release of the latest Microwire EEPROMs, Microchip Technology has now introduced ORG-enabled devices small enough to fit into MSOP and TSSOP packaging, which translates to more memory in smaller places. These packages have small footprints and are only 1.1 mm in height. Be sure to check the individual data sheets for specific package dimensions and marking information. All packages that were previously available for 93XX46, 93XX56 and 93XX66 devices are still available for 93XX46C, 93XX56C and 93XX66C components.

DATA SHEET INFORMATION

The following table shows how the devices migrate from one data sheet to another in accordance with Figure 1.

TABLE 3: DATA SHEETS

Old		New	
93AA46	DS20067	93AA46C	DS21749
93LC46	DS21712	93LC46C	DS21749
93C46	DS11179	93C46C	DS21749
93AA56	DS20067	93AA56C	DS21794
93LC56	DS21712	93LC56C	DS21794
93C56	DS11156	93C56C	DS21794
93AA66	DS20067	93AA66C	DS21795
93LC66	DS21712	93LC66C	DS21795
93C66	DS11158	93C66C	DS21795

NOTES:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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Fax: 905-673-6509

ASIA/PACIFIC

Australia
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Australia
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Fax: 61-2-9868-6755

China - Beijing
Unit 706B
Wan Tai Bei Hai Bldg.
No. 6 Chaoyangmen Bei Str.
Beijing, 100027, China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

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Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

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223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
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Shanghai, 200051
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No. 5022 Binhe Road, Futian District
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Qingdao 266071, China
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India
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-22290061 Fax: 91-80-22290062

Japan
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3-18-20, Shinyokohama
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Kanagawa, 222-0033, Japan
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Korea
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Samsung-Dong, Kangnam-Ku
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82-2-558-5934

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#07-02 Prime Centre
Singapore, 188980
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Taiwan
Kaohsiung Branch
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Min Chuan 2nd Road
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D-85737 Ismaning, Germany
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Italy
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20025 Legnano (MI)
Milan, Italy
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Fax: 39-0331-466781

Netherlands
P. A. De Biesbosch 14
NL-5152 SC Drunen, Netherlands
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Fax: 31-416-690340

United Kingdom
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Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
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