AN903

8K and 16K Microwire EEPROM Enhancements

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INTRODUCTION

The purpose of this document is to inform current or potential customers about changes made to Microchip's Microwire product line. More specifically, this document will focus on the 8K and 16K devices and any changes or improvements that have been made on the new devices. For the most part, the new devices were designed as "drop-in" replacements for the older devices. However, some changes to this product line have been made to expand the Microwire Family and introduce new products and packaging options. In addition to points listed here, we recommend that your design engineer or design team review the respective data sheets, as they have been updated to represent new devices listed here.

There are seven major areas we will talk about.

- Nominal VCC Detect
- Write Cycle Initiation
- Ready/$\overline{\text{Busy}}$ Operations
- Organization
- Program Enable
- Noise Immunity
- New Packaging Options

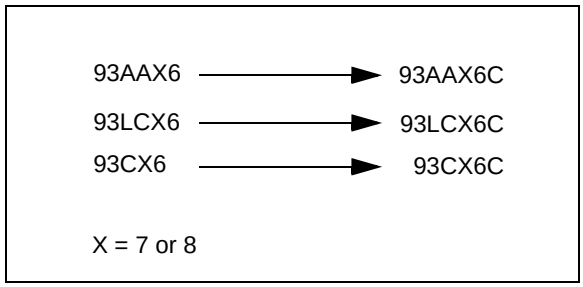
Each of these topics are covered individually in this application note under the section heading of the same name as shown above.

Table 1 below will categorize the new and old devices, into groups according to functionality.

TABLE 1: FUNCTIONAL GROUPING

Group	Devices
1 (Original)	93AA76, 93LC76, 93C76 93AA86, 93LC86, 93C86
2 (New)	93AA76A/B, 93LC76A/B 93AA86A/B, 93LC86A/B
3 (New)	93C76A/B 93C86A/B
4 (New)	93AA76C, 93LC76C 93AA86C, 93LC86C
5 (New)	93C76C 93C86C

FIGURE 1: RECOMMENDED MIGRATION PATHS



NOMINAL VCC DETECT

All of the Group 1 original devices whether 'AA', 'LC' or 'C' had a nominal voltage detect at ~1.5V. Nominal voltage detect for the new 'C' devices (Groups 3 and 5) have changed. The new 'C' devices (Groups 4 and 5) have added a voltage detect of ~3.8V to make these devices compatible with the smaller density 1K, 2K and 4K devices. This added feature provides extra protection during power-up and power-down periods when runaway processors can erroneously write to the EEPROM.

Because of this change in nominal voltage detect, applications that used Group 1 'C' devices, and have a requirement to operate below 4.5V, should be converted to Group 4 'LC' devices.

TABLE 2: NOMINAL VCC DETECT DIFFERENCES

Old Part Number	Old Spec. (Typical)	New Part Number	New Spec. (Typical)
93CX6	1.5V	93CX6C	3.8V
93LCX6B	1.5V	93AAX6B	1.5V
93LCX6B	1.5V	93LCX6B	1.5V

X = 7 or 8

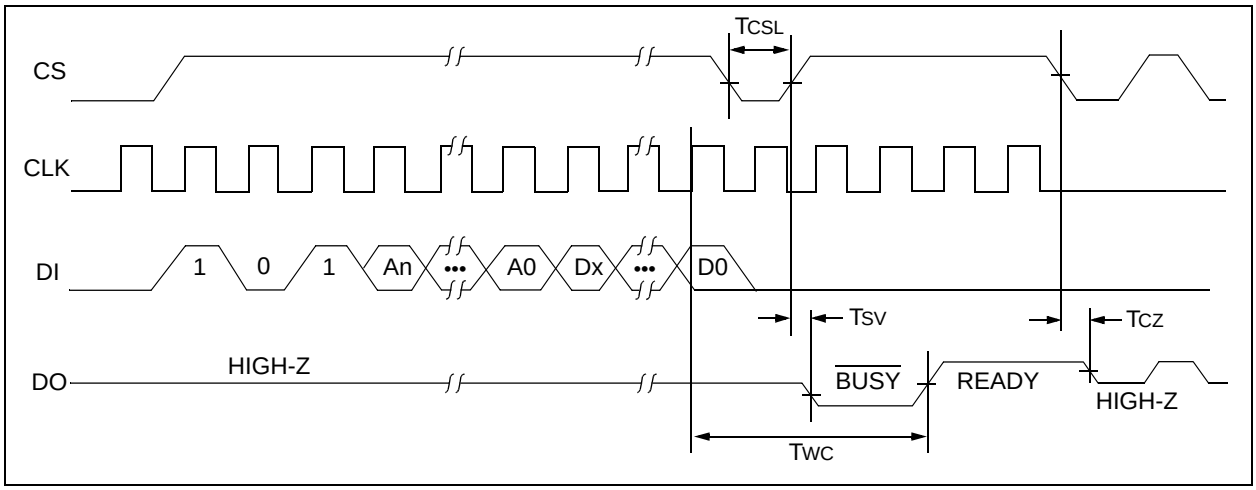
WRITE CYCLE INITIATION

Write cycle initialization has not changed on the new 8K and 16K devices. All devices initialize the write cycle on the rising edge of clock after the last data bit. Some of the lower density devices require a CS toggle in order to initiate the write cycle, but not on the 8K and 16K devices.

READY/$\overline{\text{BUSY}}$ OPERATIONS

Ready/$\overline{\text{Busy}}$ operations have not changed either. However, it is important to note that CS must be toggled (H-L-H) after the write cycle has been initiated and before the write cycle is complete in order to see transitions on the DO pin. If the CS pin has been toggled and the write cycle has been completed, the DO line will remain in the Ready (Logic '1') state until a valid Start command is given, at which point Ready/$\overline{\text{Busy}}$ operations have been reset. Ready/Busy operations are illustrated in Figure 2.

FIGURE 2: WRITE TIMING



ORGANIZATION

One of the biggest enhancements to the Microwire line for the 8K and 16K devices is the addition of dedicated 8-bit or 16-bit word organization. These devices are available only in the new 6-lead SOT-23 package and are represented by Groups 2 and 3 in Table 1. 'A' designated devices have a 8-bit dedicated word and 'B' designated devices have a 16-bit dedicated word. In addition to the ORG pin, the PE (Program Enable) pin has been eliminated and PE functions will be "don't care" for these devices.

PROGRAM ENABLE

The PE pin functionality has changed from the old devices to the new devices. On the older devices if PE was brought low at any time during a write command then that write was disabled. On the new devices the PE pin is sampled at the rising edge of clock on the last data bit. If the PE pin is low at that point the write will be disabled, if the PE pin is high at that point the write cycle will initiate.

NOISE IMMUNITY

Circuitry has been implemented on the new 8K and 16K devices to improve noise spike rejection. One circuit has been added to each input for CS, DI and CLK.

NEW PACKAGING OPTIONS

For the first time, Microchip has introduced the Microwire Family available in a new 6-lead SOT-23 package that will allow for the smallest footprint available. In order to do this, the ORG pin operations and PE pin operations have been removed so the devices are available in only dedicated 8-bit ‘A’ or 16-bit ‘B’ versions. These devices are represented in Groups 2 and 3 in Table 1.

NOTES:

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