AN880

Converting from 8051 to Microchip Assembler: A Quick Reference

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INTRODUCTION

When migrating assembly language programs from one family of microcontrollers to another, the first question is almost always: “What’s the equivalent opcode?” Some operations, like addition and subtraction, are self-evident and practically universal. Other instructions may have some subtle differences in syntax or spelling that make direct conversions a bit trickier. Occasionally, some instructions simply don’t have a direct equivalent in the target set, or an equivalent exists but is explained in different terms. Another question that arises is that of addressing modes. Typically, Direct and Indirect Addressing modes are standard in all architectures. However, they tend to be different in limitations and feature set.

To help simplify the conversion process, this application note provides a table of the instruction set of the 8051 8-bit microcontroller family and their equivalents in the PICmicro® instruction sets (Table 1). It is organized alphabetically by the 8051 instruction mnemonic in the first column, followed by the common description of the operation and the closest equivalent opcode or opcode sequence in the Microchip PIC16 and PIC18 instruction sets. In addition, the size of the instructions (in words or bytes, as appropriate) and the number of machine or instruction cycles required for execution are listed for each entry.

There are some instructions in the PICmicro® architecture that do not have exact equivalents in the 8051 architecture. For the convenience of users more familiar with 8051 instructions, these are listed separately in Table 2. They are organized by the PIC18 mnemonic in the first column, followed by the PIC16 equivalent, the closest 8051 equivalent or equivalent sequence and the common description. Again, information on the instruction size and execution time is provided.

It is important to remember that this reference list is only a starting point for code conversion. There are several considerations to keep in mind when moving code from 8-bit 8051 devices to PICmicro devices:

1. The basic processor architecture is significantly different. The 8051 processor core is a von Neumann machine which places data and program memory in the same flat memory space and accesses all information through a single bus. In contrast, all PICmicro processor cores are Harvard machines which use separate data and program memory spaces and two separate busses.
2. Both the 8051 and PICmicro devices use a data memory that is 8 bits wide. With their core architecture, 8051 devices are also limited to 8-bit wide program memories as well. Microchip PICmicro devices, on the other hand, have program memories that are either 14 bits or 16 bits wide (PIC16 and PIC18 families, respectively).
3. The 8051 devices result in greater variance in the size of instructions, from one to three bytes (depending on the operand requirements of the instruction). In contrast, PICmicro instructions are mostly single-word (two bytes) with a small amount of two-word instructions. In general, the first byte of the opcode represents the instruction, while the second byte represents the data or address payload.

4. Addressing modes in 8051 and their equivalents in PIC® microcontrollers:
   a) Direct Addressing: Both the PIC and the 8051 architecture support the Direct Addressing mode, where an 8-bit address is specified in the operand. On the 8051, only the lower 128 bytes of RAM and SFRs can be accessed in this mode. On the PIC architecture, the entire data memory is accessible in this mode.
   b) Indirect Addressing: Both the PIC MCUs and the 8051 support this mode, where a register contains the address of the operand. The 8051 cannot access SFRs in this mode. It can access both internal and external memory in this mode. PIC devices can access whole data memory and SFRs in this mode. PIC devices cannot access external memory data in this mode (some devices on the PIC18 architecture offer external data memory; however, it is accessed in Indexed Addressing mode).

      The 8051 uses R0, R1 and DPTR for indirect access. PIC devices use File Select Registers (FSR) for Indirect Addressing. The FSRs also provide the options for pre-increment, post-increment, post-decrement and the use of 8-bit offsets on PIC18 devices.
   c) Register Instructions: The register banks on the 8051 can be accessed by certain instructions that carry 3-bit information. This mode is available only on the 8051.
   d) Register Specific Instructions: On the 8051, some instructions are specific to certain registers (e.g., `CPL A`). On the PIC MCUs, most of the instructions can work on any register (e.g., same instruction as `COMF M, F`).
   e) Immediate Constants: The value of constant (literal) is in opcode. On the 8051, the Immediate Constants is one addressing mode and it can be used with many instructions. In PIC architecture, different equivalent instructions handle Immediate Constants. These are documented under literal-based operations.
   f) Indexed Addressing: Only program memory is accessed in this mode on the 8051. It is used to read the program memory content. On the PIC16, this is implemented through program memory access SFRs. On the PIC18, `TBLRD` instructions provide the read access to program memory. This instruction also provides options to pre-increment, post-increment and post-decrement the access pointers. The PIC architecture provides a way to write to program memory. The PIC18 implements various options for `TBLWT` (table write, similar to table read). The 8051 architecture does not provide instructions to write to program memory.

      The external data memory on some of the PIC18 devices can be accessed in this mode.
5. The 8051 implements 128 bits of bit addressable memory. Some of the instructions can directly operate on these bit variables. Some of the SFRs are accessible in bit addressing modes. In PIC architecture, any bit in data memory is accessible through bit access instructions. Some of the instructions with bit addressing modes in the 8051 do not have equivalent instructions in PIC architecture.
6. The classic 8051 architecture supports only 384 bytes of internal RAM. However, the variant of the architecture with expanded RAM exists. This provides additional internal RAM. This RAM is mapped as external RAM and one needs to access it in a way similar to external RAM (e.g., `MOVX` instruction). On the PIC devices, the entire internal RAM (up to 4K on the PIC18) is accessed in the same way through direct and indirect addressing.
7. The equivalent register and FSR name 4-bit location/function are different in both architectures (e.g., PSW in the 8051 is equivalent to the Status register in PICmicro devices). Users are encouraged to review the documentation for both architectures.

All of these differences can significantly change the way that both data and logical program structures are implemented. This is particularly true when indexed and indirect addressing methods are used to direct code execution. Users are encouraged to review existing Microchip application notes for the appropriate family to get an idea of how different applications are implemented.

TABLE 1: 8051 INSTRUCTIONS AND THEIR MICROCHIP EQUIVALENTS

8051			Operation	Microchip					
				PIC16			PIC18		
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
ACALL	2	2	Absolute Call	CALL	1	2	RCALL rel	2	2
ADD ADD A #data	1-2 2	1 1	Add without Carry(1) Add Literal and WREG (Accumulator)(2)	ADDWF M, F ADDLW	1 1	1 1	ADDWF M, F ADDLW	2 2	1 1
ADDC	1-2	1	Add with Carry(1)	BTFSC STATUS, C INCF M, F ADDWF M, F	3	3	ADDWFC M, F	2	1
AJMP	2	2	Absolute Jump	GOTO Addr	1	2	BRA rel	2	2
ANL ANL A #data	1-3 3	1-2 2	Logical AND(1) Logical AND Literal with WREG (Accumulator)(2)	ANDWF M, F ANDLW	1 1	1 1	ANDWF M, F ANDLW	2 2	1 1
ANL Bit	2	2	Logical AND for bit variables	No equivalent instruction					
CJNE	3	2	Compare and Jump if Not Equal(1)	SUBWF M, W BTFSS STATUS, Z GOTO Addr	3	4	CPFSEQ M BRA Addr	4	4
CLR A –	1	1	Clear Accumulator(5) Clear Memory	CLRW CLRF M, F	1 1	1 1	CLRF WREG CLRF M, F	2 2	1 1
CLR bit	1-2	1	Clear bit	BCF M, F	1	1	BCF M, F	2	1
CPL A	1	1	Complement Accumulator (/Memory)(5)	COMF M, F	2	2	COMF M, F	2	1
CPL bit	1-2	1	Complement bit	MOVLW # XORWF M, F	2	2	BTG M, F	2	1

Legend: For PICmicro mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in 8051 architecture).

Note 1: Direct or indirect addressing version of instruction depending on the registers selected by M and F; equivalent to Direct, Indirect or Indexed Addressing modes in 8051 architecture.

2: Immediate addressing version of instruction; equivalent to Immediate Addressing mode in 8051 architecture.

3: Reference routines are the 8-bit fixed-point Multiply and Divide routines specified in the Microchip application note, *AN617, "Fixed Point Routines"* (DS00617).

4: Reference routine for PIC18 devices is the 8-bit fixed-point Divide routine provided with the Microchip MPLAB® C18 C compiler.

5: Register specific instruction on 8051 architecture. On PICmicro devices, it works on all memory locations.

TABLE 1: 8051 INSTRUCTIONS AND THEIR MICROCHIP EQUIVALENTS (CONTINUED)

8051			Operation	Microchip					
				PIC16			PIC18		
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
DAA	1	1	Decimal Adjust Accumulator	ADDLW 0x06 BTFSS STATUS, DC GOTO $+3 ADDLW 0x10 GOTO $+2 ADDLW 0xFA ADDLW 0x60 BTFSS STATUS, DC ADDLW 0xA0	9	10	DAW	2	1
DEC	1-2	1	Decrement(1)	DECF M, F	1	1	DECF M, F	2	1
DIV	1	4	Divide	Divide Routine	41	269	Divide Routine	50	55
DJNZ	2-3	2	Decrement and Jump if Not Zero	DECF M, F BTFSS STATUS, Z GOTO rel	3	4	DCFSNZ M, F BRA rel	4	3
INC	1-2	1	Increment(1)	INCF M, F	1	1	INCF M, F	2	1
INC DPTR	1	2	Increment Data Pointer	INCF FSR, F	1	1	INFSNZ FSR0L, F INCF FSR0H, F	4	2
JB Bit, rel	3	2	Jump if bit set	BTFSC M, n GOTO rel	2	3	BTFSC M, n BRA rel	4	3
JBC Bit, rel	3	2	Jump if bit set and Clear bit	No equivalent instruction					
JC rel	2	2	Jump if Carry is set	BTFSC STATUS, C GOTO rel	2	3	BC rel	2	2
JMP @A + DPTR	1	2	Jump Indirect	MOVWF PCL	1	2	MOVWF PCL	2	2
JNB bit, rel	3	2	Jump if bit is not set	BTFSS M, n GOTO rel	2	3	BTFSS M, n BRA rel	4	3

Legend: For PICmicro mnemonics: `M` = memory location, `n` = specific bit location, `F` = file register, `addr` = full 13-bit or 20-bit address, `rel` = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in 8051 architecture).

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Instruction	Bytes	Cycles	Operation	PIC16			PIC18		
				Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
JNC rel	2	2	Jump if Carry not set	BTFSS STATUS, C GOTO rel	2	3	BNC rel	2	2
JNZ rel	2	2	Jump if Accumulator Not Zero	BTFSS STATUS, Z GOTO rel	2	3	BNZ rel	2	2
JZ rel	2	2	Jump if Accumulator Zero	BTFSC STATUS, Z GOTO rel	2	3	BZ rel	2	2
LCALL addr16	3	2	Long Call	CALL Addr	1	2	CALL Addr	4	3
LJMP addr16	3	2	Long Jump	GOTO Addr	1	2	GOTO Addr	4	3
MOV N, M	1-3	1-2	Move byte variable	MOVF M, W MOVWF N	2	2	MOVFF N, M	4	2
MOV A, #data	2	1	Move Literal to WREG (Accumulator)	MOVLW #	1	1	MOVLW #	2	1
MOV Db Sb	2	1-2	Move bit Data	No equivalent instruction					
MOV DPTR, #data16	3	2	Load Data Pointer with a 16-bit constant	MOVLW data MOVWF FSR	2	2	LFSR data	1	1
MOVC	1	2	Move Code byte	No equivalent PIC16 instruction			TBLRD*	1	2
MOVX	1	2	Move External	No equivalent PIC16 instruction			TBLRD*	1	2
MUL AB	1	4	Multiply(5)	Multiply Routine	21	74	MULWF M, F	2	1
NOP	1	1	No Operation	NOP	1	1	NOP	2	1
ORL	1-3	1-2	Logical OR for byte variables(1)	IORWF M, F	1	1	IORWF M, F	2	1
ORL Bit	2	2	Logical OR for bit variables	No equivalent instruction					
POP	2	2	Pop from Stack	No equivalent PIC16 instruction			POP	2	1
PUSH	2	2	Push from Stack	No equivalent PIC16 instruction			PUSH	2	1
RET	1	2	Return from Subroutine	RETURN	1	2	RETURN	2	2
RETI	1	2	Return from Interrupt	RETFIE	1	2	RETFIE	2	2

Legend: For PICmicro mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in 8051 architecture).

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8051			Operation	Microchip					
				PIC16			PIC18		
Instruction	Bytes	Cycles		Instruction(s)	Words	Cycles	Instruction(s)	Bytes	Cycles
RL	1	1	Rotate Accumulator Left	No equivalent PIC16 instruction			RLNCF M, F	2	1
RLC	1	1	Rotate Accumulator Left through Carry(1)	RLF M, F	1	1	RLCF M, F	2	1
RRC	1	1	Rotate Accumulator Right(1)	No equivalent PIC16 instruction			RRNCF M, F	2	1
RRC	1	1	Rotate Accumulator Right through Carry(1)	RRF M, F	1	1	RRCF M, F	2	1
SETB	1-2	1	Set bit	BSF M, F	1	1	BSF M, F	2	1
SJMP rel	2	2	Short Jump	GOTO rel	1	2	BRA rel	2	2
SUBB	1-2	1	Subtract with Borrow(1)	BTFSS STATUS, C INCF M, F SUBWF M, F	2	1	SUBWFB M, F	2	1
SWAP A	1	1	Swap nibbles within the Accumulator(5)	SWAPF M, F	1	1	SWAPF M, F	2	1
XCH XCHD	1-2 1	1 1	Exchange Accumulator with byte variable Exchange Digit	No equivalent instruction					
XRL XRL A #data	1-3 2	1-2 1	Logical Exclusive OR for byte variables(1) Exclusive OR Literal with WREG (Accumulator)	XORWF M, F XORLW	1 1	1 1	XORWF M, F XORLW	2 2	1 1

Legend: For PICmicro mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in 8051 architecture).

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TABLE 2: MICROCHIP PIC18 INSTRUCTIONS WITHOUT EXACT EQUIVALENTS IN THE 8051 FAMILY

Microchip						Operation	8051		
Equivalent to PIC18	#Bytes	#Cycles	Equivalent to PIC16	#Words	#Cycles		Name	#Bytes	#Cycles
BN rel	2	2	BTFSC M, 7 GOTO Addr	2	3	Branch if Negative	No equivalent instruction		
BNN rel	2	2	BTFSS M, 7 GOTO Addr	2	3	Branch if Not Negative	No equivalent instruction		
BNOV rel	2	2	BTFSS STATUS, OV GOTO Addr	2	3	Branch if Not Overflow	JNB PSW.2 rel	3	2
BOV rel	2	2	BTFSC STATUS, OV GOTO Addr	2	3	Branch if Overflow	JB PSW.2 rel	3	2
CLRWDT	2	1	CLRWDT	1	1	Clear Watchdog Timer	No equivalent instruction		
CPFSGT M	2	2	No equivalent PIC16 instruction			Compare M with W, skip if M > W	No equivalent instruction		
CPFSLT M	2	2	No equivalent PIC16 instruction			Compare M with W, skip if M < W	No equivalent instruction		
DECFSZ M, F	2	2	DECFSZ M, F	1	2	Decrement M, skip if 0(1)	DEC JNZ	3-4	3
INCFSZ M, F	2	2	INCFSZ M, F	1	2	Increment M, skip if 0(1)	INC JNZ	3-4	3
INFSNZ M, F	2	2	No equivalent PIC16 instruction			Increment M, skip if not 0(1)	INC JZ	3-4	3
MOVLB #	2	1	BSF/BCF STATUS, RP0 BSF/BCF STATUS, RP1	2	2	Move Literal to BSR	CLR/SETB PSW.3 CLR/SETB PSW.4	4	2
NEGF M, F	2	1	COMF M, F INCF M, F	2	2	Negate (Two's Complement)	XCH A, M CPL A INC A XCH A, M	6	4
RESET	2	1	No equivalent PIC16 instruction			Reset	No equivalent instruction		
RETLW	2	2	RETLW	2	2	Return Literal to W	MOV A # RET	3	3

Legend: For PICmicro mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in 8051 architecture).

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Microchip						Operation	8051		
Equivalent to PIC18	#Bytes	#Cycles	Equivalent to PIC16	#Words	#Cycles		Name	#Bytes	#Cycles
SETF	2	1	MOVLW 0xFF MOVWF M	2	2	Set File to all '1's	MOV M, #	3	2
SLEEP	1	1	SLEEP	1	1	Enter Sleep (Power-down) mode	MOV A, #0x2 ORL PCON, A	4	2
SUBWF M, F	2	1	SUBWF M, F	1	1	Subtract W from M(1)	No equivalent instruction		
TBLRD (*+; *-; +*)	2	2	No equivalent PIC16 instruction			Table Read with pointer manipulation	No equivalent instruction		
TBLWT (*; *+; *-; +*)	2	2	No equivalent PIC16 instruction			Table Write with pointer manipulation	No equivalent instruction		
TSTFSZ M	2	2	No equivalent PIC16 instruction			Test M, skip if 0	CJNE M, #0, rel	3	2

Legend: For PICmicro mnemonics: M = memory location, n = specific bit location, F = file register, addr = full 13-bit or 20-bit address, rel = 8-bit or 11-bit offset, WREG = W register (equivalent to accumulator in 8051 architecture).

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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07/28/03