# AN846

# Basic PLL Filters for the rfPIC™ /rfHCS

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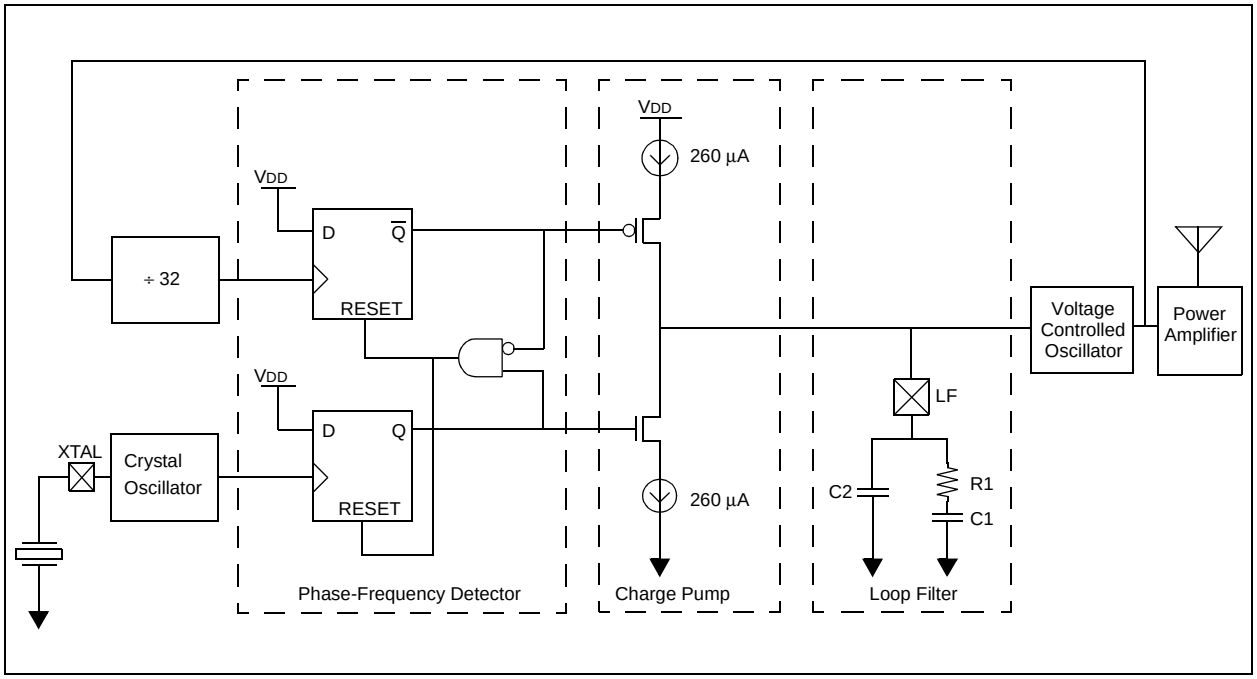
## INTRODUCTION

This application note will give designers a method to design their own Phase Lock Loop (PLL) filters for rfPIC transmitters, such as the rfPIC12C509 and the rfHCS362. First the circuit will be briefly described and then example components will be found with the included Microsoft® Excel® spreadsheet. The spreadsheet is called pllfilter.xls and can be downloaded from the same Microchip web page that hosts this application note.

A PLL circuit creates an output signal synchronized to the phase of the crystal reference signal as shown in Figure 1. The RF output frequency is from a voltage controlled oscillator (VCO). It is divided by 32 for comparison to the reference oscillator. A phase-frequency detector compares the phase of the output signal to the crystal oscillator reference signal. The loop filter closes the control loop by filtering the phase error signal to create the voltage that drives the VCO.

If the output signal drifts, then the phase-frequency detector tells the charge pump to push it back into phase. Thus, the accuracy and stability of a crystal oscillator can correct an otherwise poor RF oscillator.

**FIGURE 1: BLOCK DIAGRAM**



The loop filter we are trying to design is basically a capacitor holding the DC voltage that controls the VCO. The charge pump gives it a shot of current when the phase-frequency detector determines the output frequency is a little slow, or discharges the cap when the output is a little fast. Since the output error cannot be resolved faster than the reference frequency, the maximum frequency of current spikes hitting the loop filter is the reference frequency.

Every filter has a bandwidth and a phase response, this low pass PLL filter is no exception. The low pass bandwidth is easy to understand as the maximum frequency that the filter will pass. Low order filters roll off slowly, so we consider the frequency whose output is 3 dB down as the cutoff frequency. The phase response is a little more difficult to visualize, but just imagine that the filter is increasingly delaying the output signal as it exceeds the cutoff frequency. Our low pass filter will be able to delay the higher frequencies up to a quarter wavelength, or 90°. However, together with the 90° phase shift of the VCO we get dangerously close to 180° which would let the loop oscillate around the RF output frequency.

Oscillations would also require a minimum loop gain of 1, so for a low pass filter we only need to determine the phase shift of frequency where the filter is at unity gain. Then subtract this calculated phase shift from the 180° limit to get our safety margin, which we call the phase margin. All higher frequencies with phase shift approaching 180° will be attenuated and will not pose an oscillation threat.

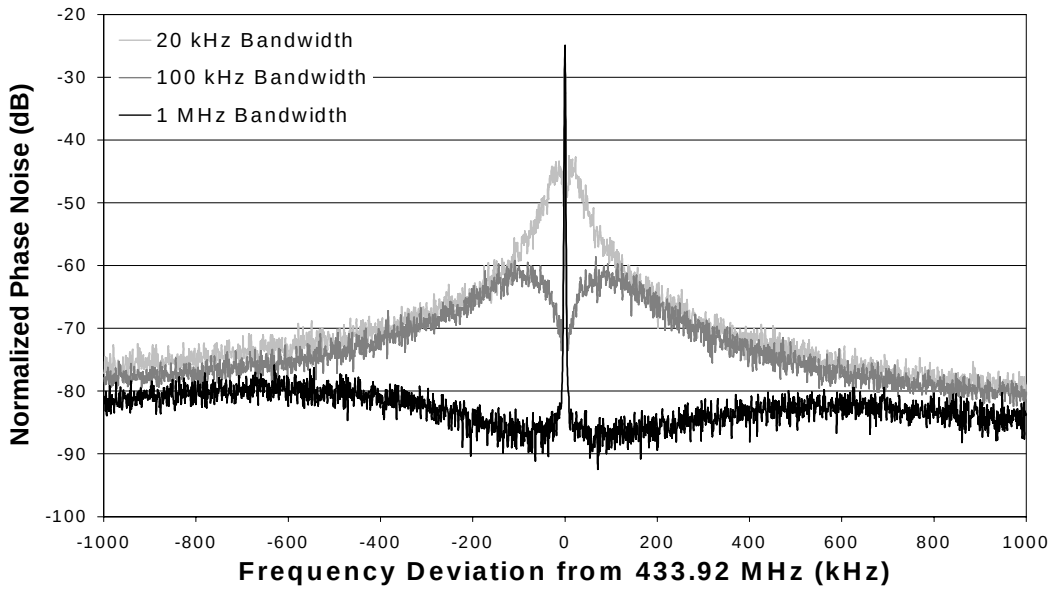
For those more familiar with control theory, phase margin ($\phi_m$) is directly related to the damping factor ($\zeta$) by this formula:

$$\tan\frac{(90^\circ - \phi_m)}{2} = \frac{1}{4 \cdot \zeta^2}$$

As the phase margin gets small, the loop filter will ring when the reference frequency starts up or is modulated. If the phase margin is large, then it takes much longer to lock on the reference frequency. The response time is actually a function of both the phase margin and the filter bandwidth. Filter capacitors larger than 10 nF, or resistive loading on the filter pin, will also affect response time by limiting the slew rate. The 260 µA peak output current from the charge pump, reduced by maximum duty cycle to about 180 µA, limits the slew rate according to this formula:

$$\text{rise time} = \Delta V \cdot C / I$$

**FIGURE 2: LOOP BANDWIDTH VS. PHASE NOISE**



The VCO output frequency is not very stable by itself and this frequency jitter is called phase noise. A benefit of the closed control loop is that the phase noise can be controlled. Figure 2 shows the filter bandwidth effect on phase noise. There is more information on this in the Microwave & RF Radio Systems article, parts 4 and 5, which are referenced at the end of this application note.

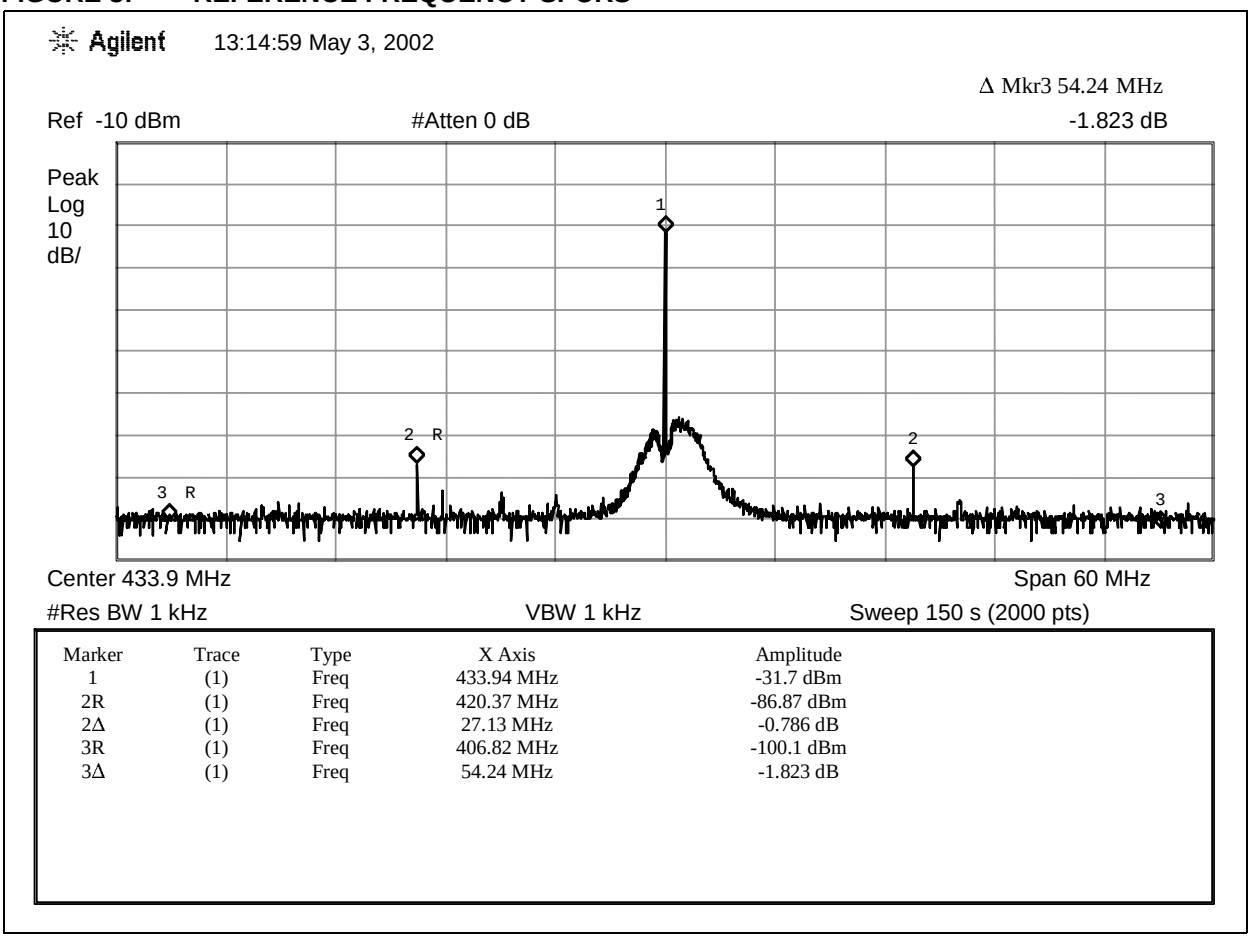
Noise within the loop bandwidth is suppressed while noise outside the bandwidth may increase. Thus it is desirable to design a filter with the largest possible bandwidth.

As the filter bandwidth is increased, more of the phase-frequency detector noise gets through. This noise appears as spurs in the RF output spectrum at the carrier frequency plus and minus integer multiples of the reference frequency. Figure 3 shows the spur levels for a filter bandwidth of 1 MHz. This is an important bandwidth because here the noise spurs start to get significant with respect to the carrier phase noise. Increasing the bandwidth further will make the spurs dominate the transmitted noise. For a narrow band receiver it may be beneficial to increase the bandwidth to 2 MHz and eliminate more of the phase noise since the spurs are filtered off by the receiver bandwidth. If the carrier frequency is adjacent to a restricted band then it is better to reduce the bandwidth to below 500 kHz which will reduce the spurs that reach into the restricted band.

Choosing a loop filter bandwidth is also limited by physical constraints. As the bandwidth gets very narrow the capacitors required become very large. Too wide a bandwidth will be difficult to manufacture because the capacitors become very small. To keep the design simple try and use capacitors that are at least 5 times bigger than the sum of the parasitic and LF pin capacitance. Assuming this is about 2 pF, the filter capacitors should be at least 10 pF. This will limit the bandwidth to a maximum of 1.2 MHz. Lower carrier frequencies can have a slightly higher loop bandwidth. The spreadsheet will let you enter a stray capacitance value to design for wider bandwidths but these designs are more susceptible to manufacturing variations.

The 2 pole filter design, shown in Figure 1, was chosen because it is the lowest order filter that gets the desired bandwidth and phase margin performance. This simple circuit is easy to analyze and uses only three passive components. More expensive active filters or more complex passive filters may improve particular characteristics, but they can also insert more noise into the control loop.

**FIGURE 3: REFERENCE FREQUENCY SPURS**




| Marker | Trace | Type | X Axis | Amplitude |
|---|---|---|---|---|
| 1 | (1) | Freq | 433.94 MHz | -31.7 dBm |
| 2R | (1) | Freq | 420.37 MHz | -86.87 dBm |
| 2Δ | (1) | Freq | 27.13 MHz | -0.786 dB |
| 3R | (1) | Freq | 406.82 MHz | -100.1 dBm |
| 3Δ | (1) | Freq | 54.24 MHz | -1.823 dB |

### Initial Requirements

For most designs, the three loop filter components can be quickly found with the spreadsheet calculator. The only value the spreadsheet requires is the RF frequency. The application and the governing regulations in the market area will determine this frequency. The Microwave & RF Radio Systems article part 2, referenced at the end of this application note, provides more detail on frequency selection.

To optimize the design a little more, you may also modify any of the assumptions that the spreadsheet makes for loop bandwidth, phase margin, and stray capacitance.

The PLL filter basically holds the DC level that controls the VCO. However, the output frequency has an impact on the filter because the VCO is not linear. At some loop filter voltages the VCO frequency is more sensitive to loop filter variations. The typical response curve is shown in Figure 4. The spreadsheet interpolates a look-up table of typical measured values to determine the loop gain.

In amplitude shift keying (ASK) the signal amplitude is modulated to transmit data while the carrier frequency is held constant. Since the frequency does not change the filter can trade off slower response time for better spurious noise filtering. The response time must be fast enough to enable and stabilize the output frequency before the power amp begins transmitting. A faster PLL also reduces unwanted frequency modulation caused by power supply variations.

In frequency shift keying (FSK), the carrier frequency is modulated to transmit data while the signal amplitude is held constant. The frequency must change quickly and smoothly to the new frequency to achieve higher baud rates and lower inter-symbol interference. Decreasing the phase margin a couple degrees and increasing the filter bandwidth will improve settling time on the start of each bit. Making the bandwidth too wide increases the size of the reference spurs. In most cases the default bandwidth of 1 MHz will work well since the data rate is already limited by how far the crystal can be pulled.

### Calculating Component Values

The formulas to do these calculations are embedded in the Microsoft Excel spreadsheet, called pllfilter.xls that can be downloaded from the same Microchip web page that hosts this application note. The format of the spreadsheet is shown in Figure 5. This spreadsheet example was run at 433.92 MHz, since it is a typical frequency for many rfPIC and rfHCS applications.

The spreadsheet is laid out in the order you would typically solve the problem. First the highlighted user input frequency, then the fixed transmitter parameters, and most importantly, the three calculated filter component values. Step 1 calculates theoretical component values for the given filter parameters. Step 2 does the reverse, calculating filter parameters for the actual filter components. Step 3 checks if your circuit measurements match the original design target.

The values for the 2 capacitors and resistor will immediately be recalculated as the RF frequency is modified. This is your opportunity to see how the components vary as the other fields, like the filter bandwidth, are modified. Just use the Undo command to restore the original default parameters or download the file again. Some of the cells are hidden to reduce clutter. Most of the cells are locked without a password to prevent accidentally changing the fixed parameters.

**FIGURE 4: TYPICAL LOOP FILTER VOLTAGE AND VCO GAIN CURVES**

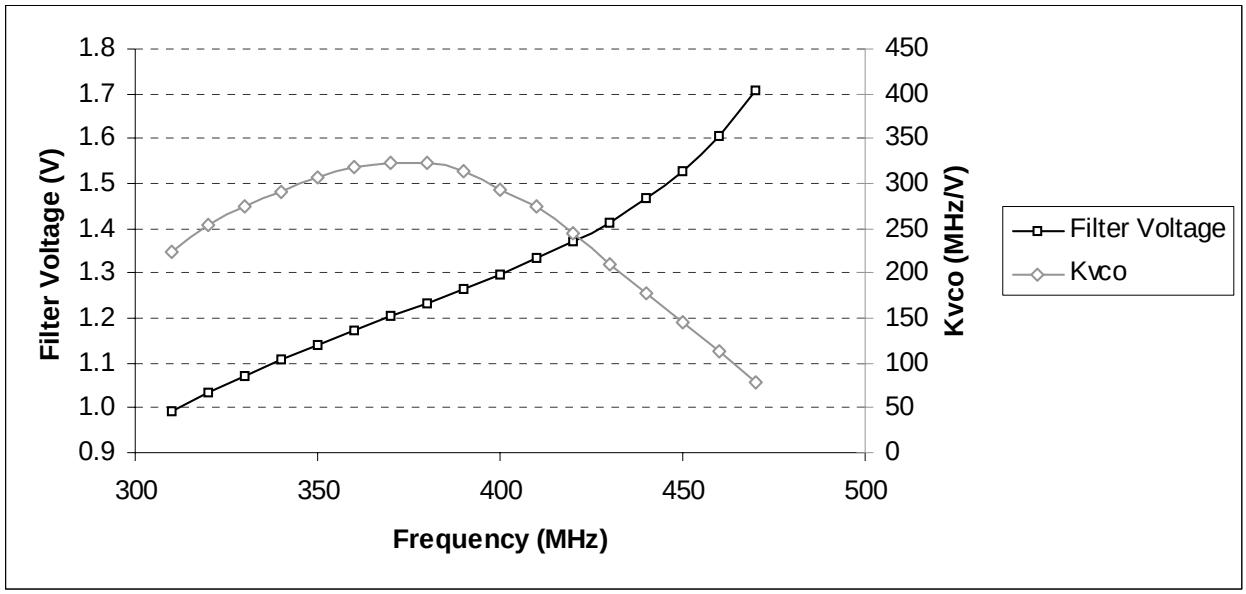


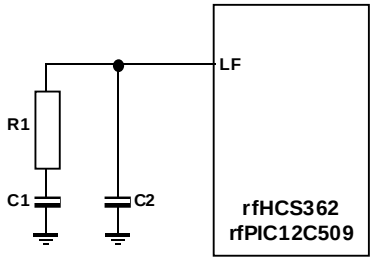
**FIGURE 5: PLL FILTER DESIGN CALCULATOR**

# AN846 Filter Design Calculator

Rev 1

## Step 1: Enter transmitter frequency

| **Desired System:** | | | **Notes:** |
|---|---|---|---|
| Transmitter Frequency | 433.92 | MHz | Determined by regulations |
| **Design Parameters:** | | | |
| Crystal Frequency | 13.56 | MHz | |
| Desired Phase Margin | 50 | degrees | |
| Desired Loop Bandwidth | 1000 | kHz | Reduce loop bandwidth for smaller spurs<br>Increase loop bandwidth for less phase noise |
| **Device Parameters:** | | | |
| Multiplication Factor (N) | 32 | times | |
| Phase Detector Gain (Kϕ) | 0.26 | mA | |
| VCO Gain (Kvco) | 197.868 | MHz/V | |
| LF pin stray capacitance | 2 | pF | |
| **Filter Calculations:** | | | |
| Natural Frequency | 641155 | Hz | |
| Loop Bandwidth | 6283185 | rad/s | |
| Calculated Pole | 17262910 | Hz | |
| Calculated Zero | 2286892 | Hz | |
| Lock Time | 5 | us | |
| Calculated Ctotal | 112 | pF | |
| Calculated C1 | 99 | pF | |
| Calculated C2 | 13 | pF | |
| Calculated R1 | 4414 | ohms | |




## Step 2: Enter Actual Components and Tolerances

| **Actual Values Used:** | | | **Tolerance:** |
|---|---|---|---|
| Actual Value C1 | 100 | pF | ± 5.0% |
| Actual Value C2 | 12 | pF | ± 5.0% |
| Actual Value R1 | 4700 | ohms | ± 1.0% |

Recalculate

| **Filter Analysis:** | **Min:** | **Typical:** | **Max:** | |
|---|---|---|---|---|
| Natural Frequency | 622766 | 638145 | 654723 | Hz |
| Actual Pole | 16435003 | 17325228 | 18300705 | Hz |
| Actual Zero | 2006280 | 2127660 | 2262264 | Hz |
| Actual Loop Bandwidth | 1023146 | 1038389 | 1054269 | Hz |
| Actual Phase Margin | 47 | 49 | 51 | degrees |
| Lock Time | 5 | 5 | 5 | us |

## Step 3: Enter Measured Voltage Peak and Bandwidth

| **Oscilloscope:** | | | | | |
|---|---|---|---|---|---|
| Voltage final | 1.466 | V | | | |
| Voltage peak | 1.648 | V | Phase Margin | 33.0 | degrees |
| Voltage valley | 1.456 | V | Damping Factor | 0.68 | |
| Time peak | 370 | us | | | |
| Time valley | 1880 | us | Natural Freq. | 450.74 | kHz |
| **Spectrum Analyser:** | | | | | |
| Shoulder-Shoulder | 1800 | kHz | Bandwidth | 900 | kHz |

### Choosing Components

The filter calculations will yield ideal component values which may be considerably different than the standard or stocked values you have the freedom to choose from. For this reason Step 2 of the filter worksheet recalculates the filter performance for real world component values and tolerances.

Choose actual capacitor and resistor values from the pull-down lists or type in your own value. Do the same for the plus/minus tolerance and then press the Recalculate button. Choose different values or more accurate components if the resulting worst case phase margins are not between 40 and 60 degrees. A wide variation in the loop bandwidth means a wide variation in the reference clock spur levels. Be sure to test boards with the widest bandwidth to ensure the spur levels are acceptable.

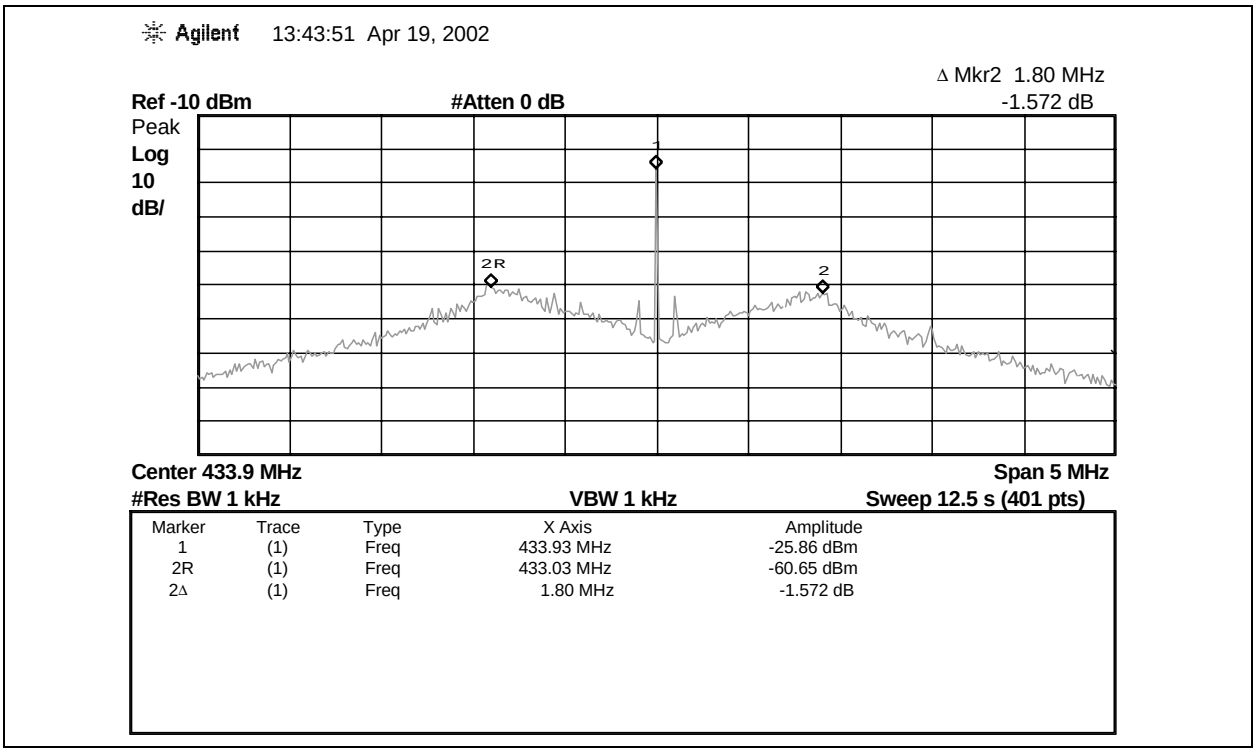
The example in Figure 5 shows the closest standard values that matched this design. Pressing the Recalculate button shows that the typical results still match our design target. It also shows the component tolerances do not exceed the phase limits.

There is a lot of flexibility in the actual components you choose. For example, the footprint size, type of dielectric, voltage rating and tolerance. The loop filter circuit runs at the crystal frequency, so typically, ceramic capacitors are the best low cost choice. For dielectrics choose NP0 if possible. The larger value for C1 may require an X7R. In this example, C1 and C2 are both available in the 0603 package with an NP0 dielectric. Be sure to update the tolerance to 10% if you choose a X7R dielectric.

Using a metal film resistor can reduce the resistor's noise contribution, but a cheaper thick film resistor should work fine. In this example the resistor is a 1% thick film. This costs only a fraction of a cent more than a 5% tolerance part, but significantly reduces the phase margin variations in production for lower bandwidth filters.

The footprint size of the components is not critical and is usually determined by the production limitations. Ideally, smaller components are better to reduce the filter circuit area and the associated sensitivity to radiated noise. Surface mount components make RF design much easier with reduced lead inductance and they do not interfere with solid ground planes.

**FIGURE 6: MEASURING FILTER BANDWIDTH ON SPECTRUM ANALYZER**



### Board Layout

The PLL loop filter may look like a DC voltage, but it is very sensitive to noise and leakage. Very small signals can be induced on top of the DC level and converted to frequency variations by the VCO. They will appear as noise spurs in the RF output spectrum. For example, Figure 6 shows two spurs about ±100 kHz from the carrier which are caused by the internal rfHCS362 oscillator.

A dirty circuit board will let charge bleed off the capacitor and require extra current spikes from the phase detector to keep up the voltage. This extra ripple at the crystal reference frequency will appear on the output spectrum as spurs at the carrier frequency plus and minus multiples of the reference frequency. The leakage is not typically a problem until you get to filter capacitors below 20 pF where 100 kΩ of leakage can increase spurs by more than 10 dB.

Start your layout by keeping any other traces out of the filter area. Stay especially far away from high current traces like power and the antenna. Keep the filter traces as short as possible to pick up less noise. Provide a good solid ground plane on the back side of the board. Wrapping ground traces around the filter on the component side with several low impedance vias to the ground plane can also reduce radiated noise from being captured, but too close and the board will be more susceptible to leakage. One final tip that applies to any high frequency design is to eliminate or minimize the area of loops. Any traces and components in series that make a complete loop at RF frequencies create an antenna that is both susceptible to noise and transmits noise.

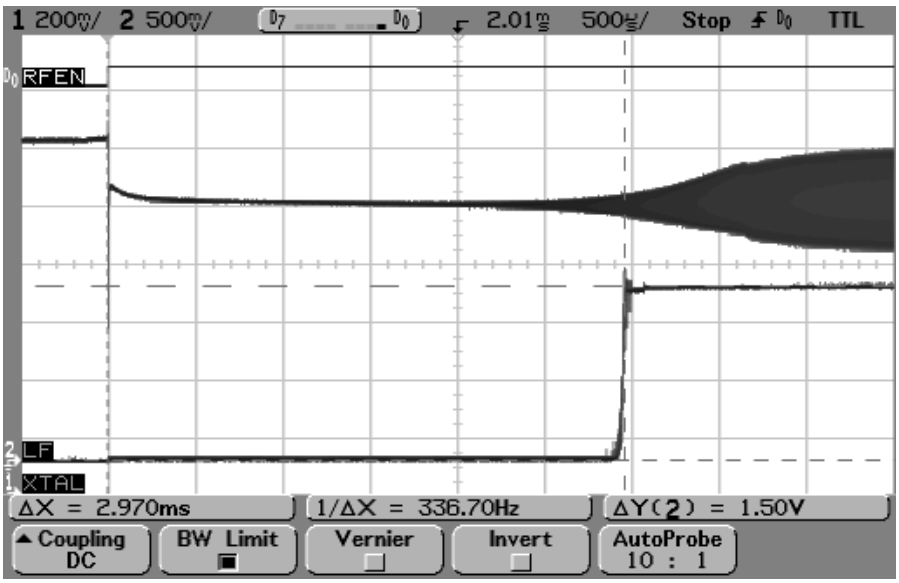
### Testing

The min and max values calculated by the spreadsheet indicate variability, but do not guarantee your design will work. You should test the worst case boards over temperature and voltage ranges to verify your filter design is acceptable.

With an oscilloscope you can measure the phase margin from the transient response on the LF pin as the chip powers up, or when switching between frequencies in FSK operation. With a spectrum analyzer you can compare the spectrum of the transmitted carrier to the desired bandwidth and look for other sources of noise. Modify your circuit to test with a steady unmodulated RF signal. Your results may be clearer if you eliminate some resonances by detuning the antenna. Once the circuit is working and the transmit spectrum looks right, then turn on the modulation and test for filter response times and ringing on FSK designs.

A high logic level on RFEN$_{IN}$ pin enables the reference crystal oscillator and the voltage controlled oscillator. The difference between the two oscillator frequencies causes the charge pump to quickly charge up the filter caps as shown in Figure 7. The PLL can lock onto the frequency faster than the starting up crystal oscillator can stabilize. When the LF pin reaches 0.8V the RF frequency is close to locked on the crystal frequency. This initiates an internal 150 microsecond delay to ensure that the PLL settles. After the delay the PS/DATA$_{ASK}$ bias current and power amplifier are enabled to start transmitting.

**FIGURE 7: TRANSMITTER START-UP WAFEFORM**



To verify that the phase angle matches your design target, zoom in on the PLL filter voltage as the PLL locks on the crystal reference frequency. Measure the peak, valley, and settled voltages and times as shown in Figure 8. Plug them into Step 3 on the spreadsheet to get your measured phase margin and natural frequency. Even with a high impedance, low capacitance scope probe there can be significant measurement error. However, if the scope capacitance is much smaller than the filter capacitance, this simple test can get results within a couple percent of your design target. For large capacitance the response will be slew rate limited by the 260 µA charge pump.

A 20 MHz spectrum analyzer could be used to further analyze the loop filter noise, but it is faster just to skip over to the RF output with an RF spectrum analyzer. These RF tests have to be done anyway to pass radiation regulations and they do not modify the PLL filter with probe loading. The loop bandwidth can be seen in Figure 6, as approximately the distance from the carrier frequency in the center to the noise shoulder on either side.

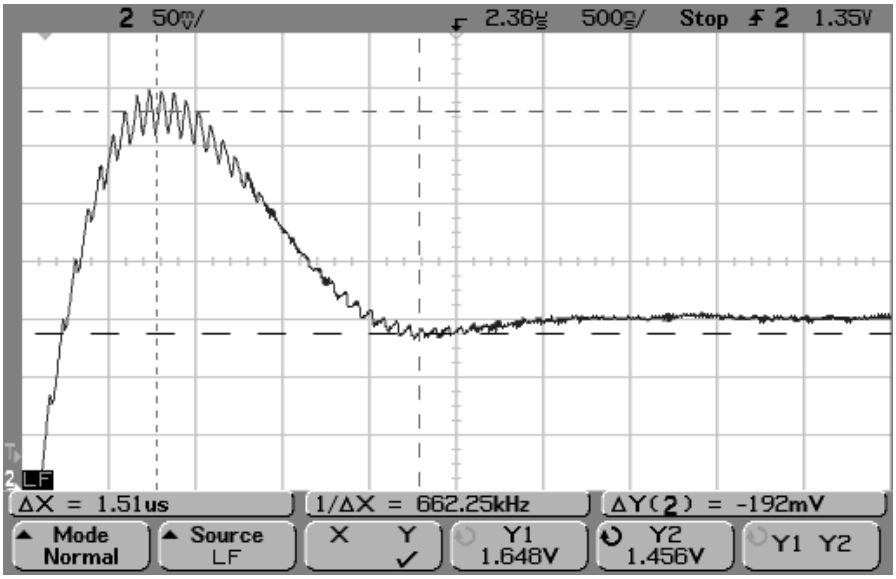
This setup can also reveal other noise sources that create unwanted spurs. The difference of the noise spur frequency from the carrier is the frequency of the noise source on your circuit board. For example, there will be spurs at integer multiples of the crystal frequency which are amplified by board leakage. To see this effect put a 100 kΩ resistor in parallel with either C1 or C2. There may also be spurs at multiples of the crystal frequency divided by 4 from the CLKOUT signal.

To find the source of the noise spur measure the frequency offset from the carrier and probe your circuit for other traces carrying that frequency. Disable or modify the frequency of that signal to see if the RF spur changes. Once you identify the source of the noise you can reduce it to acceptable levels with solutions like moving traces, shielding with ground traces, filtering, by-pass capacitors, or modifying its frequency.

The PLL filter will determine the transmitted phase noise and spurs near the carrier frequency. Microchip has other application notes such as AN826 and AN831 to help with the crystal selection and antenna matching.

If your transmitter circuit is working satisfactorily then you are ready to get it packaged and tested for regulatory compliance. The next section lists some resources for studying PLL filters in more depth. There is also lots of free material available online with a little search of the web.

**FIGURE 8: MEASURING PHASE MARGIN FROM OVERSHOOT WITH AN OSCILLOSCOPE**



### Additional Information

Phase-Locked Loops, Design, Simulations, &Testing 3rd Ed; Roland E Best; McGraw-Hill; ISBN 0-07-006051-7

PLL Performance, Simulation, and Design, Dean Banerjee, ISBN 0-9708207-0-4

“Radio Systems, Part 1, Design of Short-Range Radio Systems”, (Microwaves & RF [September 2001] 73-80)

“Radio Systems, Part 2, Understanding Regulations”, (Microwaves & RF [October 2001] 79-96)

“Radio Systems, Part 3, Constructing Circuits”, (Microwaves & RF [February 2002] 59-74)

“Radio Systems, Part 4, Tracking Phase Noise”, (Microwaves & RF [March 2002] 57-64),
Penton Media, www.mwrf.com

## APPENDIX A: MATHEMATICAL DERIVATIONS

This appendix will show how the equations for R1, C1, and C2 are derived. The solution will be described physically, where possible, to avoid losing anyone in the Laplace transforms. For greater detail, read the references given in the previous section.

The open loop gain of the PLL circuit will be the product of the phase detector gain ($K_\phi$), filter impedance ($X_{total}$), and VCO gain ($K_{vco}$) divided by N. The large frequency error detected in the open loop case causes the charge pump to push its maximum current. This current, times the filter impedance, is the voltage seen by the VCO input. The VCO then converts the voltage back to a frequency. The open loop frequency response poles and zeros are the same as for $X_{total}$ because N and $K_\phi$ are constant and $K_{vco}$ is approximately constant near the desired output frequency.

**EQUATION 1:**

$$Gain_{openloop} = \frac{K_\phi \cdot X_{total} \cdot K_{vco}}{N}$$

The combined impedance of the three filter components in the loop filter are:

**EQUATION 2:**

$$X_{total} = \frac{1}{\frac{1}{X_{C2}} + \frac{1}{R1 + X_{C1}}} = X_{C2} \cdot \frac{(R1 + X_{C1})}{(R1 + X_{C2} + X_{C1})}$$

The impedance can be defined in terms of frequency by replacing $X_c$ with $1/j\omega C$, and then grouping the zero and poles:

**EQUATION 3:**

$$X_{total}(\omega) = \frac{1 + j \cdot \omega \cdot R1 \cdot C1}{j \cdot \omega \cdot (C1 + C2) \cdot \left(1 + j \cdot \omega \cdot R1 \cdot \frac{C1 \cdot C2}{C1 + C2}\right)}$$

The time constant for the zero will be defined as:

**EQUATION 4:**

$$\tau_z := R1 \cdot C1$$

The first pole is at zero and the time constant for the second pole will be defined as:

**EQUATION 5:**

$$\tau_p := R1 \cdot \frac{C1 \cdot C2}{C1 + C2}$$

Substituting Equation 4 and Equation 5 into Equation 3 simplifies it to:

**EQUATION 6:**

$$X_{total}(\omega) := \frac{1 + j \cdot \omega \cdot \tau_z}{j \cdot \omega \cdot (C1 + C2) \cdot (1 + j \cdot \omega \cdot \tau_p)}$$

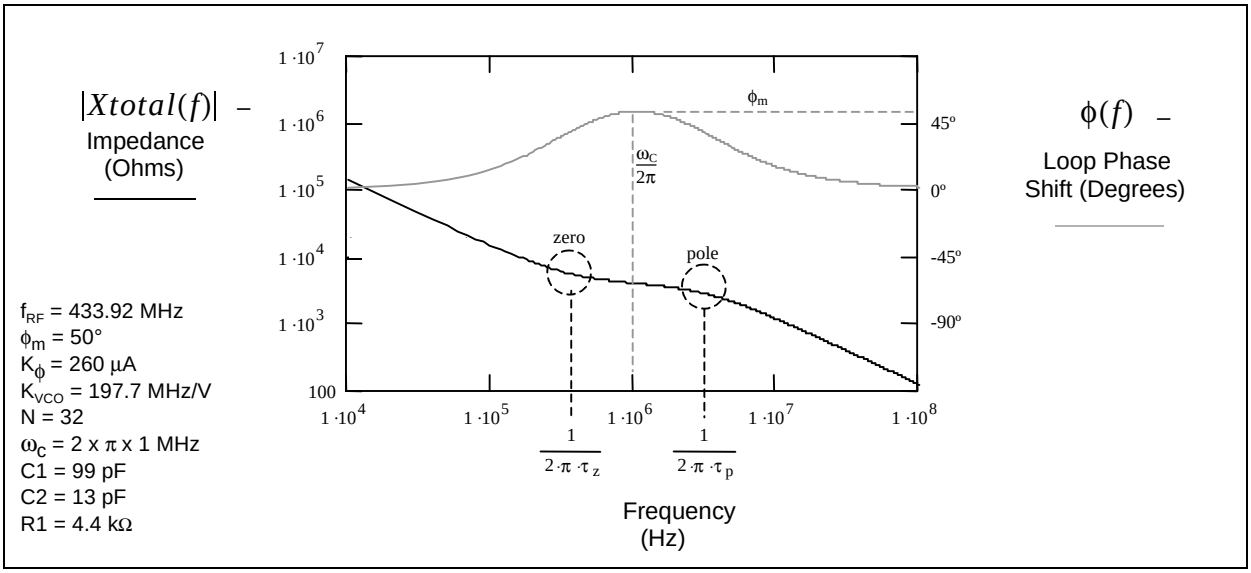
Phase margin is the difference between 180 degrees and the actual phase shift at the frequency where the open loop gain equals 1. The phase response can be written as the sum of the vector angles originating at the poles minus the vector angle originating from the zero:

**EQUATION 7:**

$$\phi(\omega) := \pi + \operatorname{atan}(\omega \cdot \tau_z) - \operatorname{atan}(\omega \cdot \tau_p)$$

Figure 9 should make everything a little clearer. The graph is plotted against the frequency of the filter and not the final RF output frequency.

**FIGURE 9:**




Solving for the maximum phase margin by finding where the derivative of $\phi_m(\omega_c)$ equals 0 results in:

**EQUATION 8:**

$$\omega_c \cdot \tau_z = \frac{1}{\omega_c \cdot \tau_p}$$

Substituting Equation 8 back into Equation 7 and solving for $\tau_p$ finds the time constant of the pole in terms of the 3 dB loop bandwidth ($\omega_c$) and maximum phase margin ($\phi_m$):

**EQUATION 9:**

$$\tau_p = \frac{-\tan(\phi_m) + \sqrt{\tan(\phi_m)^2 + 1}}{\omega_c} = \frac{\sec(\phi_m) - \tan(\phi_m)}{\omega_c}$$

The time constant is easily derived from Equation 8 using Equation 9:

**EQUATION 10:**

$$\tau_z = \frac{1}{\omega_c \cdot \sec(\phi_m) - \omega_c \cdot \tan(\phi_m)}$$

The value of the sum of the 2 capacitors is found by setting the open loop gain to 1 and substituting Equation 9 and Equation 10 into Equation 1:

**EQUATION 11:**

$$C1 + C2 = \frac{K_\phi \cdot K_{vco} \cdot \tau_z}{N \cdot \omega_c}$$

Equation 5 can now be used to find all the component values with the time constants from Equation 9 and Equation 10:

$$C2 = \frac{(C1 + C2) \cdot \tau_p}{\tau_z} = \frac{K_\phi \cdot K_{vco}}{N \cdot \omega_c} \cdot \tau_p$$

**EQUATION 12:**

$$C1 = \frac{K_\phi \cdot K_{vco}}{N \cdot \omega_c} \cdot (\tau_z - \tau_p)$$

**EQUATION 13:**

$$R1 = \frac{\tau_z}{C1}$$

**NOTES:**

**Note the following details of the code protection feature on PICmicro® MCUs.**

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