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Understanding the MCP250XX Devices

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INTRODUCTION

In the past, product offerings for Controller Area Network (CAN) controllers have trended towards the more complex. These increasingly complex devices fit very well in CAN systems where a lot of decision making requires CAN nodes to contain a programmable processor to handle the tasks.

While the trend has been towards complex and expensive systems, CAN lends itself very well to less complex systems due to its relatively low cost robust data transfer capabilities. There is a growing interest in distributing control on systems that would, at first glance, seem cost prohibitive or otherwise out of reach.

The MCP250XX family of devices are simple CAN I/O expanders that are designed to address the growing needs of system designers to distribute simple control and/or extend the reach of a centralized processor.

This application note discusses the operation of the MCP250XX and details some of the features and capabilities of the device that are not normally discussed in the data sheet. This application note assumes familiarity with the MCP250XX data sheet (DS21664), however, some discussion may be repeated. Each of the modules in the block diagram (Figure 5) are discussed in detail and loosely follows the layout of the data sheet. Together with the data sheet, this application note will provide the information needed to fully understand Microchip's CAN I/O expander solution.

DEFINITION OF TERMS

The following definitions are used throughout this document:

I/O Expander - used in this document to refer to the Integrated Circuit device being described (MCP250XX).

Command Messages - refers to the predefined messages that make up Input Messages, Output Messages, and Information Request Messages.

Input Message (IM) - term given to messages that are received by the MCP250XX and cause the internal registers to be modified. Once the register modification has been performed, the MCP250XX transmits a 'Command Acknowledge' message to indicate that the command was received and processed.

Command Acknowledge Message - term given to the message that is automatically transmitted by the MCP250XX after receiving, and processing, an input message.

Information Request Message (IRM) - term given to Remote Request messages that are received by the MCP250XX which subsequently generate an output message (data frame) in response.

Output Message (OM) - term given to the message that the MCP250XX sends in response to a Information Request message.

On Bus Message - term given to the message that the MCP250XX transmits after completing the power-on/self configuration sequence and at timed intervals if enabled.

Self Configuration - term used to describe the process of transferring the contents of the EPROM memory array to the SRAM memory array.

On Bus - term used to describe the condition when the MCP250XX is fully configured and ready to transmit or receive on the bus. On bus is the only state in which the MCP250XX can transmit on the bus.

Change-of-State - in this document this term is used generically to describe conditions on the digital or analog inputs that occur which meets a specified set of criteria. For example; a change-of-state occurs if a high-to-low transition occurs on a GPIO pin that is configured as an input and has the associated polarity bit set to a '0'. If the polarity bit is set to a '1' (low-to-high transition) then no change-of-state occurs. For analog channels a change-of-state only occurs if a conversion results in a value that is above or below (again determined by the polarity bit) the associated compare value. In this way this is not a true change-of-state in which *any* change on the input is considered to be a change-of-state.

Digital Input Edge Detection (DIED) - refers to the ability of the MCP250XX to automatically transmit a message due to a predefined edge occurring on a specified digital input.

Analog Input Threshold Detection (AITD) - refers to the ability of the MCP250XX to automatically transmit a message due to a predefined analog level being reached on a specified analog channel.

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DEVICE OVERVIEW

The MCP250XX devices operate as I/O expanders for a Controller Area Network (CAN) system, supporting CAN V2.0B active with bus rates up to 1 Mb/s, The MCP250XX allows a simple CAN node to be implemented without the need for a microcontroller.

The devices are identical, with the following exceptions:

Device	A/D	One-wire CAN
MCP25020	No	No
MCP25025	No	Yes
MCP25050	Yes	No
MCP25055	Yes	Yes

THEORY OF OPERATION

In the simplest terms, CAN I/O expanders provide remote input and output capabilities using the CAN bus as the communications medium. Outputs can be modified and inputs can be read by transmitting predefined CAN messages. These predefined messages can be either requests made by another node for information from the I/O expander or can be a command from another node to modify one or more outputs.

The MCP2502X/5X Datasheet (DS21664) contains more details on the command messages.

The MCP250XX CAN I/O Expanders

In addition to simple I/O functionality, MCP250XX devices have some intelligence to perform other basic functions/capabilities:

- Custom User Defaults
- Scheduled Transmission
- Digital Input Edge Detection
- Analog Input Threshold Detection
- Command Acknowledge capability
- Sleep Mode and Wake-up From Sleep
- Command Messages to Read and Modify Peripherals and Registers

Custom User Defaults

The MCP250XX can be customized to the user's needs by configuring the User Registers to the application. The User Registers are contained in EPROM and become the user defaults on power-up and/or reset. On power-up or after reset, these user registers are transferred to SRAM and can be dynamically changed during operation via special CAN messages.

In addition, there are sixteen 8-bit registers (USERID0 - USERID15) that can contain any data. These registers can be used to indicate node identification such as serial numbers, model numbers, bar codes, etc. These registers are not transferred to SRAM on power-up.

CONFIGURING USER DEFAULTS

There are three methods used to configure the custom user defaults:

1. MPLAB® IDE 5.50 or later and PRO MATE® II device programmer. Together with two files (MCP250XX.asm and MCP250XX.inc) included with MPLAB, the MCP250XX devices can be quickly configured. Read the comments in the *.inc* file for help with modifying the *.asm* file.

2. MCP250XX CAN Developer's Kit - There is a PC interface that allows the MCP250XX devices to be configured with defaults. The software can configure the devices directly on the board, or it can create a HEX file that PRO MATE II can use through MPLAB to configure the devices. The software ships with the development kit or can be downloaded from Microchip's website.

3. Custom system or third party system which operates to the MCP250XX Programming Specification (DS20072).

Scheduled Transmission

Allows the device to send a CAN message at regular intervals. This message can be used as a heartbeat to the system indicating that the module is still functioning. The message can be configured to contain either zero data or the digital input and A/D status.

The MCP250XX will send a single "on-bus" message after power-up regardless if scheduled transmissions are enabled or not. This first message contains zero data bytes and serves as an indicator to the network that the MCP250XX node has successfully powered up and is communicating on the bus. See Figure 1.

Refer to the CAN Protocol Module section for details about the transmit message IDs and contents.

FIGURE 1:   ON BUS MESSAGE AND SCHEDULED TRANSMISSIONS
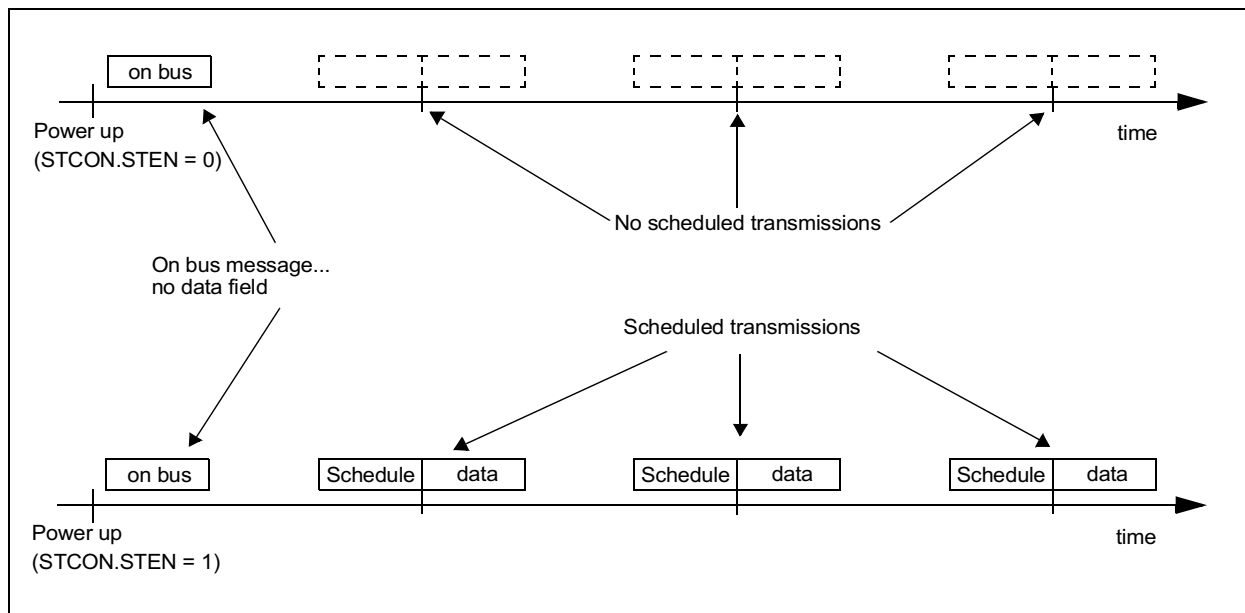
Digital Input Edge Detection (DIED)

All GPIO pins have an edge detection feature that will automatically transmit a message when an edge with the proper polarity occurs on any of the digital inputs. Only pins configured as inputs and enabled for this function via control registers IOINTEN and IOINTPO will perform this operation. The transmitted message contains the digital status in the data field.

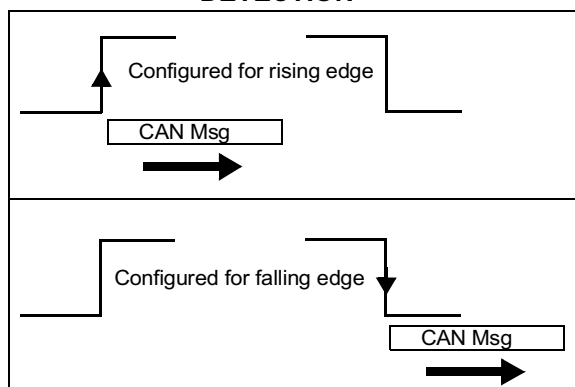DIED is individually configurable for each pin configured as a digital input.

Refer to the CAN Protocol Module section for details about the transmit message IDs and contents.

FIGURE 2:   DIGITAL INPUT EDGE DETECTION

Analog Input Threshold Detection (AITD)

Each GPIO pin that has been configured as an analog input can be individually configured to automatically transmit a message when a predefined threshold is exceeded. The configuration can be for either going above or below the predefined threshold. The transmitted message contains the A/D values in the data field.

Refer to the CAN Protocol Module section for details about the transmit message IDs and contents.

HYSTERESIS FUNCTION

This function is automatic and will insure that an analog value that is on the compare edge (i.e., toggling LSb) does not fill the CAN bus with continuous A/D message transmissions. Figure 3 demonstrates how the hysteresis function works.

FIGURE 3:   HYSTERESIS FUNCTION
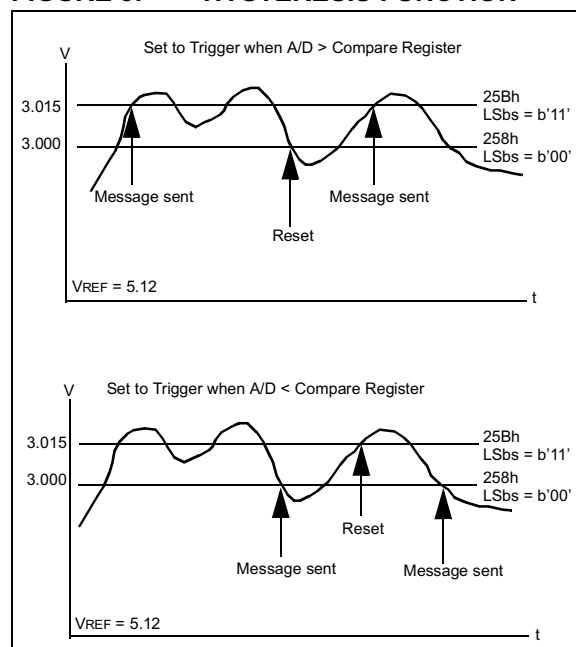
Command Acknowledge Capability

When configured, the MCP250XX will transmit a message to acknowledge an "Input Message" was received and processed (i.e, internal registers were modified).

The command acknowledge can be viewed as a handshake to insure that the receiving MCP250XX received and processed an Input Message.

Example:

4. MCP250XX receives an Input Message to change the GP latches.
5. The MCP250XX processes the message and changes the latches.
6. The MCP250XX transmits the Command Acknowledge message.

Sleep Mode and Wake-up from Sleep

The MCP250XX has a low power sleep mode and can wake-up under several conditions.

SLEEP MODE

If configured, the MCP250XX will automatically enter a low power state after a long bus idle time (minimum of 1408 consecutive recessive bit times).

The following operations do not function while in sleep mode:

• A/D conversion
• Auto-conversion mode
• Auto-messaging (scheduled transmissions)
• PWM module and outputs
• Clock Output

The digital ports remain unchanged during sleep mode.

WAKE-UP FROM SLEEP MODE

The device will then wake-up under any of the following conditions, if configured:

• External reset input on $\overline{RST}$ pin
• Edge detection on digital input (if DIED is enabled)
• CAN bus activity (the first message is ignored)

Command Messages to Read and Modify Peripherals and Registers

The MCP250XX is accessed via the CAN bus. The peripherals, configuration, and status can be read via "Information Request Messages" (IRMs) that are received by the MCP250XX on the CAN bus. These same peripherals can be modified, as can the device's configuration, by receiving "Input Messages" (IMs). IRMs and IMs are both receive messages and are differentiated by the buffer they are received into. In addition, the MCP250XX implements "Output Messages" in response to IRMs.

The command message functions are covered in detail in the data sheet, however, the following overview is supplied:

RESERVED ID BITS

There are four reserved bits in the ID field which are used to implement the command message functions. Three bits determine the message type and one bit is referred to as the direction bit (Figure 4).

Message Type Bits

The MCP250XX determines the message type of the command messages by checking the value of the three LSbs of the arbitration field.

Direction Bit

The ID is identical for both the IRM and the responding OM except for the direction bit:

• Information Request Messages: Direction bit = 1
• Output Messages: Direction bit = 0

The location of the direction bit in the ID field can be either in the RTR bit position or bit three of the arbitration field. See the next two sections for more information.

Information Request Messages (IRM)

Information Request Messages (IRM) are messages that the MCP250XX receives into Receive Buffer 0 (matches Filter 0) and then responds to by transmitting a message (Output message) containing the requested data.

The IRM can be implemented as either remote frames or as data frames:

IRM as Remote Frame - If the IRM is implemented as a remote frame, the RTR bit is the direction bit. The IRM sets the RTR bit (remote frame) and the OM clears the RTR bit (data frame) and sends the requested data.

Note:	When using remote frames for IRMs, the data length code (DLC) must be set to the expected returning data length. When using data frames for IRMs, the data length code (DLC) must equal 0.

IRM as Data Frame - If the IRM is implemented as a data frame, bit 3 of the ID is reserved as the direction bit. The IRM sets bit 3 and clears the DLC to zero. The responding OM will clear bit 3 and return a data frame with the correct data length.

The MCP250XX supports the following IRMs:

• Read A/D Regs - Used to request A/D information and GPIO status.
• Read Control Regs - Requests the value of seven controls registers including A/D , pin, scheduled transmission, and interrupts configurations.
• Read Config Regs - Requests pin data direction, digital input levels, and CAN bit timing settings.

- Read CAN Error - Requests the error flag register and error counters value.
- Read PWM Config - Requests all PWM configuration settings.
- Read User Mem (banks 1 and 2) - Two messages request the sixteen user defined bytes.

Output Messages (OM)

Output Messages are messages transmitted by the MCP250XX in response to IRMs. These messages contain the requested information as requested by the IRM.

The OM messages are same as the IRMs except OMs contain the requested data in the data field and the direction bit is cleared to zero.

OM in Response to Remote IRM - If the IRM was implemented as a remote frame, the resulting OM will be a data frame (RTR bit = 0).

OM in Response to a Data Frame - If the IRM was implemented as a data frame, the resulting OM will be a data frame with bit 3 (direction bit) of the ID field cleared to a zero.

Input Messages (IM)

The primary purpose of Input messages is to reconfigure MCP250XX parameters (if needed) while in an operating CAN system. IMs are received into buffer 1 and are used to modify the registers in SRAM. The MCP250XX supports the following IMs:

- Write Register - performs bit manipulation to addressed SRAM locations using a "mask" byte with a "value" byte
- Write to the three TXIDs - reconfigures the three transmit IDs (one message for each TXID buffer)
- Write I/O Configuration - writes to a group of configuration registers
- Write Mask and Filters (three messages) - Three messages to change mask and filters. The MCP250XX temporarily switches to configuration mode
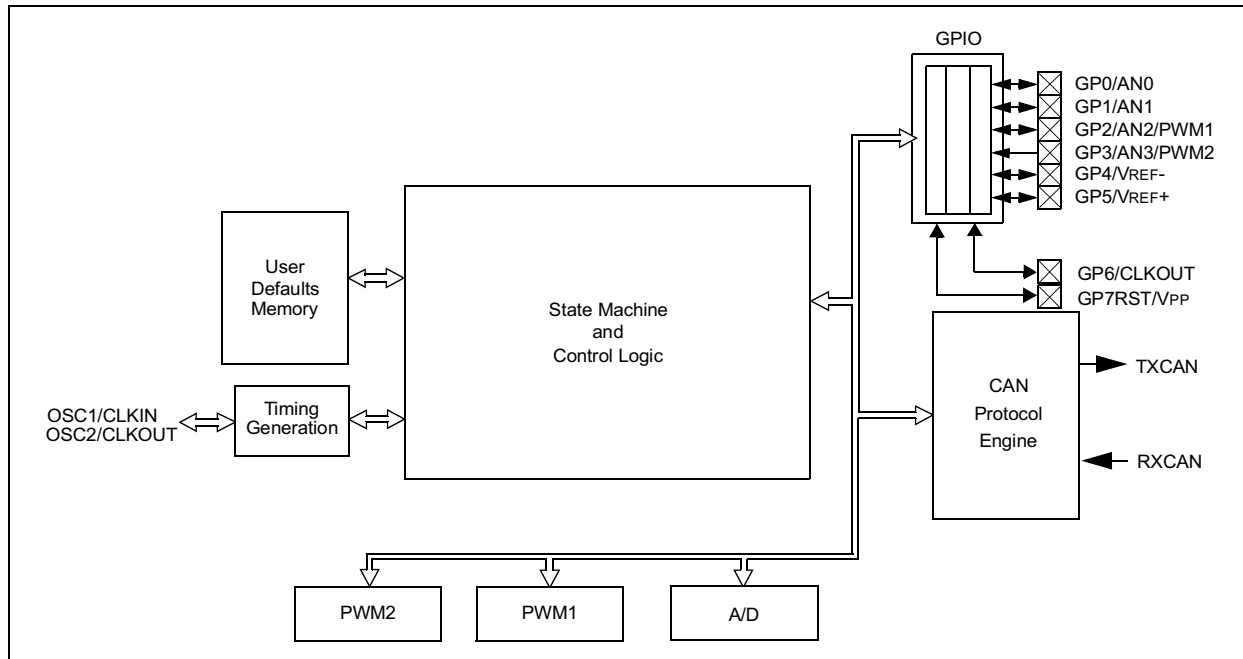
FIGURE 4:   COMMAND AND DIRECTION BITS
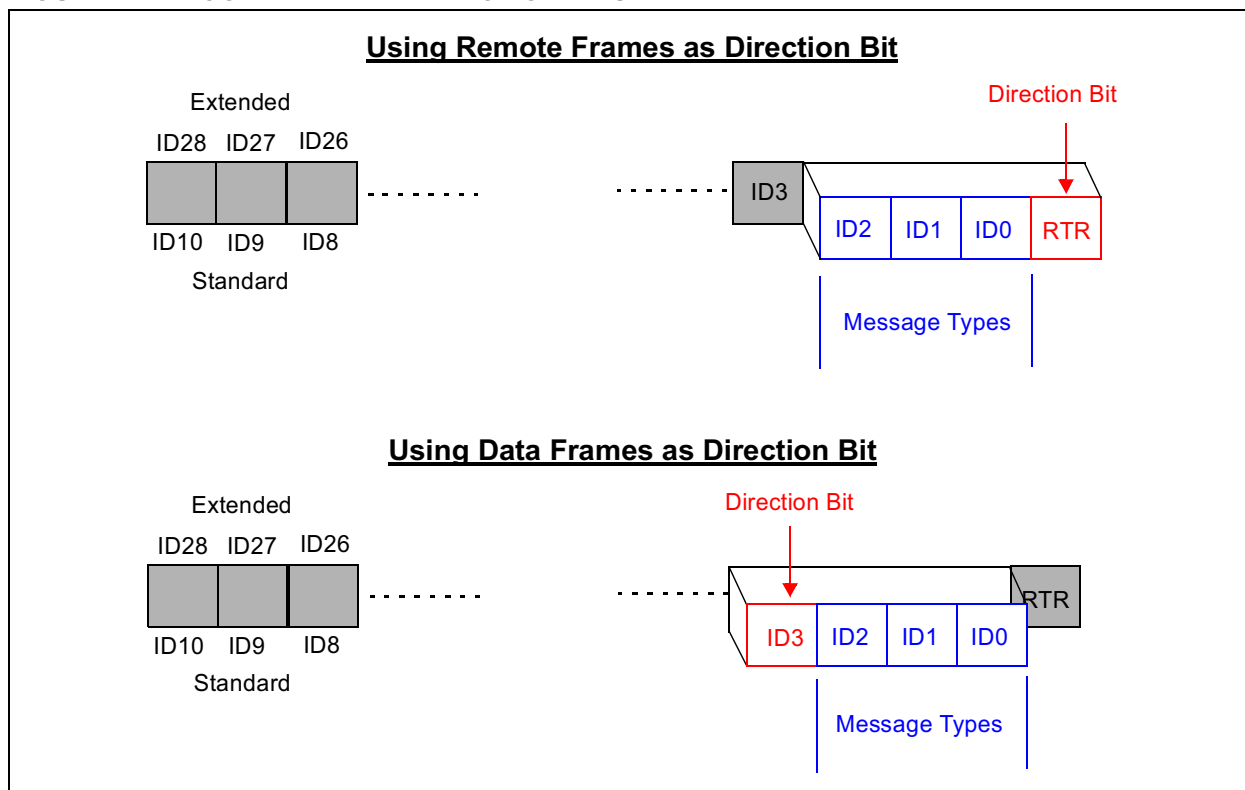
MCP250XX BLOCK DIAGRAM

The MCP250XX features a number of peripherals which surround the control logic (Figure 5). The following sections discuss how to configure each peripheral.

FIGURE 5:   MCP250XX BLOCK DIAGRAM

CONTROL LOGIC

The Control Logic performs the interface functions between the other modules and controls the data flow and operation beginning with initial power-up.

The block is discussed first in order to cover functions/features that are not covered in any of the other modules or are worth repeating in this section. Discussions are limited to these functions and features.

Clockout Function

The MCP250XX can configure GP6 as a clock-out pin. This feature can be used to clock another device. The clock-out is controlled in the OPTREG1 register ($\overline{\text{CLKEN}}$ and CLKPS1:CLKPS0) and can be prescaled for:

• Fosc / 1
• Fosc / 2
• Fosc / 4
• Fosc / 8

Changing CAN Modes of Operation

The CAN mode of operation can be changed between Listen Only mode and Normal mode by configuring the OPTREG1.CMREQ via the "Write Register" Input Message.

> **Note:** The OPTREG1.CMREQ must be cleared (zero) in the default configuration or the device may unexpectedly enter Listen Only mode on the first IM.

Error Recovery

The MCP250XX can be configured to recover from bus-off condition to either Listen Only or Normal mode by configuring the OPTREG2.ERREN bit.

Command Acknowledge vs. Receive Overflow

The MCP250XX can be configured to utilize either "Command Acknowledge" or "Receive Overflow" by configuring OTREG2.CAEN. Both functions cannot be enabled at the same time. TXID1 is the identifier for both messages and neither message contains a data field.

COMMAND ACKNOWLEDGE

Command Acknowledge is sent by the MCP250XX after an Input Message is received and processed and is used to provide a handshake to the master node sending the Input Message.

0.0.1 RECEIVE OVERFLOW

If enabled, a Receive Overflow message is transmitted by the MCP250XX if a receive buffer is overrun by an incoming message. A receive overflow can only occur if a second message is destined for the same receive buffer before the first message is processed (e.g., two IRMs are sent to the MCP250XX back-to-back and the first one is not processed before the second one comes in).

Transmit on Error Counter Exceeding Limit

The transmit and receive error counters (TEC and REC) reflect CAN communication errors. If the counters exceed specific values, the CAN module transitions error states and the MCP250XX will send a message, if enabled.

If enabled (OPTREG2.TXONEN), TXID1 will be sent with TEC and REC count values for the following conditions:

- REC or TEC > 95
- REC or TEC > 127

This is covered in more detail in the TXID1 section.

Power-up Mode

The MCP250XX can be configured to power-up in Listen Only mode or Normal mode via OPREG2.PUNRM.

POWER-UP IN LISTEN ONLY MODE

When the MCP250XX is configured to power-up in Listen Only mode, it will automatically switch to Normal mode after seeing the first error-free message.

SLEEP MODE FROM LISTEN ONLY MODE

The MCP250XX can be configured to automatically transition to Sleep mode while in Listen Only mode after power-up (OPTREG2.PUSLP). This allows the MCP250XX to transition to low power mode while waiting for a valid message on the bus.

> **Note:** Devices in Listen Only mode cannot acknowledge CAN messages. In the event there are only two CAN devices on the bus (e.g., one master node and one MCP250XX), the MCP250XX will not be able to switch from Listen Only mode to Normal mode. This is because a message transmitted by the only other node (master) is not acknowledged, which is defined as an errored message.

CAN PROTOCOL MODULE

The CAN module is a protocol controller that converts between raw digital data and CAN message packets. The main functional block of the CAN module are:

- CAN protocol engine
- Buffers, Masks, and Filters

The module features are as follows:

- Implementation of the CAN protocol
- Two separate receive buffers
- One full acceptance mask (standard and extended)
- Two full acceptance filters (standard and extended)
- One filter for each receive buffer
- Three prioritized transmit ID buffers for transmitting predefined message types
- Low power SLEEP mode
- Automatic wake-up on bus traffic function
- Error management logic for transmit and receive error states

Mask and Filters

There is one mask associated with the two filters. Identifiers matching filter 0 go into buffer 0 while filter 1 matches go to buffer 1.

RESERVED MASK AND FILTER BITS

Certain bits in the mask and filters are reserved for implementing the Command Messages. Which bits are reserved depends an a few factors including if receiving standard or extended frames, and whether the device filters on remote frames or data frames.

Figure 6 shows the mask and filter settings for standard *remote* and standard *data* frame formats. The filter bits are effectively turned off where the mask bits are forced to zero.

As discussed earlier, the main difference between implementing remote frames and data frames is the position of the "direction" bit. The direction bit refers to the direction of the message and differentiates IRMs from OMs.

If using remote frames for IRMs and OMs, the direction bit is the RTR bit:

- RTR bit set = received IRM
- RTR bit cleared = resulting transmitted Output message

If using data frames (i.e., not remote frames) for IRMs and OMs, the direction bit is bit 3 of the ID field:

- Bit 3 = set = received IRM
- Bit 3 = cleared = resulting transmitted Output message

If you want to...

Use *Remote Frames* for Command Messages, specifically IRMs.

You must...

- Reserve ID bits 2 - 0 for Command Message functions
- Use *remote frames* as IRMs (i.e., the node transmitting to the MCP250XX must transmit a remote frame). The RTR bit is set for IRMs and is cleared for Output Messages. The RTR bit can be considered a direction bit with respect to the MCP250XX (RTR bit set = received message)
- Set data length code (DLC) to expected data length of responding "Output Message" (see data sheet for details)

If you want to...

Use *data frames* for Command Messages (i.e., not use remote frames).

You must...

- Reserve ID bits 3 - 0 for Command Message functions. Bit three takes the role of direction bit (i.e., Bit 3 is set for IRMs and cleared for Output Messages)
- Use data frames for IRMs with bit 3 equals set
- For IRMs set the data length code to zero because by definition, IRMs contain no data field. The responding Output Message will clear bit 3 and contain the appropriate data and DLC

FIGURE 6:   STANDARD FRAME FILTERING

Preliminary
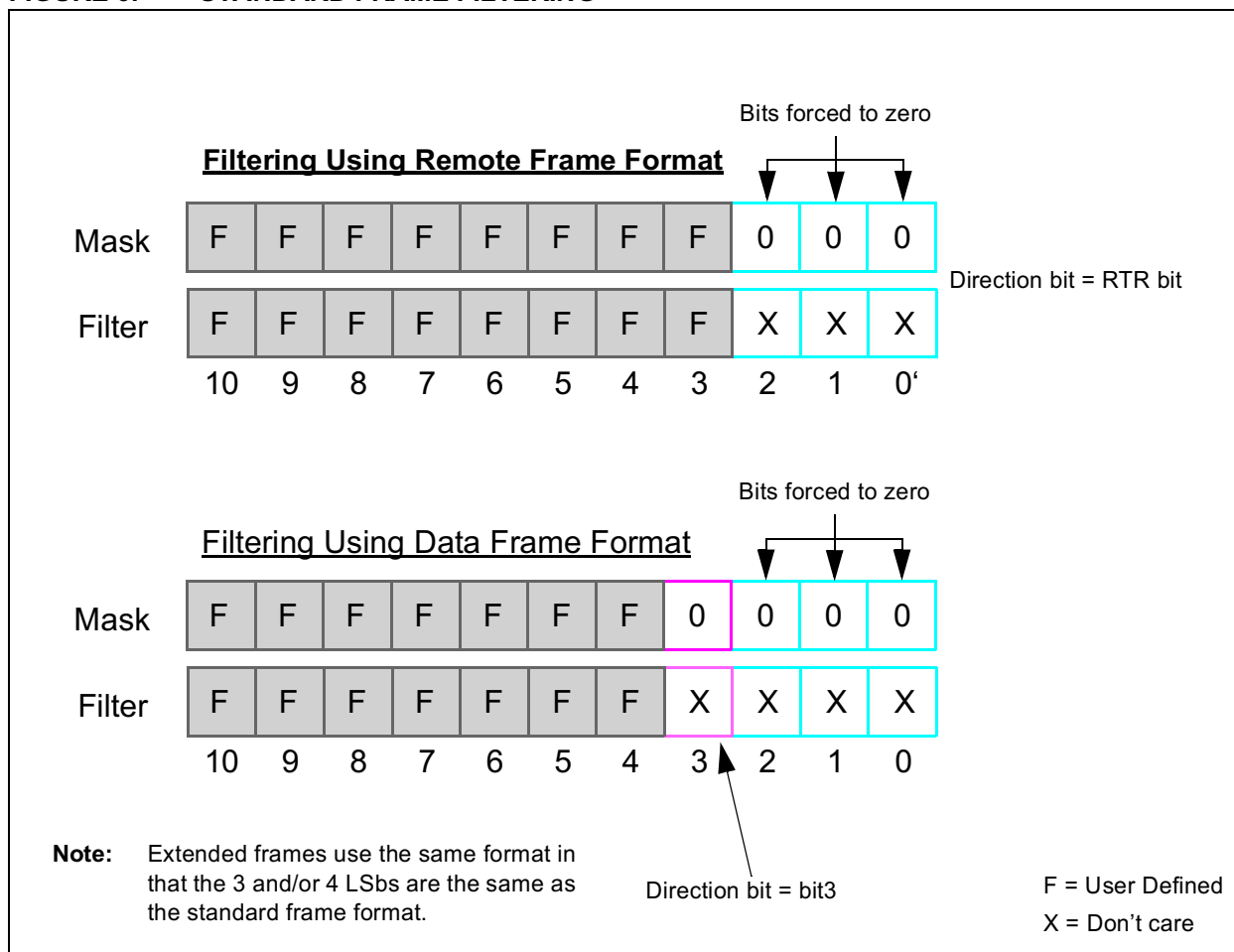
FIGURE 7:   REGISTERS ASSOCIATED WITH MASK AND FILTERS

RXMEID8 - Acceptance Filter Mask Extended Identifier Mid

EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8

RXMEID0 - Acceptance Filter Mask Extended Identifier Low

EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0

EID3 - is forced to '0' when using extended data frames as IRMs (OPTREG2.MTYPE = 1).
EID2:EID0 - always forced to logic '0'.

RXFnSIDH - Acceptance Filter n Standard Identifier High

SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3

SID3 - becomes "direction bit" when using standard data frames as IRMs (OPTREG2.MTYPE=1 -> SID3=X).

RXFnSIDL - Acceptance Filter n Standard Identifier Low

SID2	SID1	SID0	—	EXIDE	—	EID17	EID16

SID2:SID0 - lower 7-bits of standard ID
EXIDE - depending on mask bit, will filter on IDE bit in CAN message
EID17:EID16 - upper 2 bits of extended ID

RXFnEID8 - Acceptance Filter n Extended Identifier Mid

EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8

RXFnEID0 - Acceptance Filter Mask Extended Identifier Low

EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0

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Transmit Message IDs (TXID)

The MCP250XX device contains three separate transmit message ID's: TXID0, TXID1, and TXID2. The data length code is predefined for each of the various output messages and the data that is transmitted comes directly from the contents of the device's peripheral registers.

TABLE 1: TRANSMIT MESSAGE IDS

TXID#	Name	Data	Comment	Controlled via Register
TXID0	On-bus	No data	On-bus message (first message sent).	Cannot be disabled
	Scheduled transmission	Can contain the same data as the "Read A/D Regs" message or zero data bytes.	The intervals are configurable from (4096)Tosc through (268.4*10^6)Tosc.	STCON
TXID1	Command Acknowledge	No data	Used as a handshake to indicate an IM was received and processed.	OPTREG2.CAEN - Can be disabled by enabling "Receive Overflow"
	Receive Overflow	No data	Indicates an incoming message overflowed the receive buffer due to a previous unserviced message residing in the buffer.	OPTREG2.CAEN - Can be disabled by enabling "Command Acknowledge"
	Error Condition	TEC, REC, and EFLG	Indicates either error counter reached error warning or error passive.	OPTREG2.TXONEN
TXID2	Digital Input Edge Detection	GPDDR and GPIO (input state)	This message is sent when a predefined edge is detected on any enabled digital input.	IOINTEN - Enables function IOINTPO - Configures polarity. GPDDR - Corresponding pin must be an input. ADCON1 - PCFG bits configure pin as analog or digital.
	Analog Input Threshold Detection	Contains the same data as the "Read A/D Regs" message	Message is sent when a predefined analog threshold is exceeded.	IOINTEN - Enables function IOINTPO - Configures polarity. GPDDR - Corresponding pin must be an input. ADCON1 - PCFG bits configure pin as analog or digital. ADCMPnH and ADCMPnL - Configures the 10-bit threshold.

Preliminary

TXID0

Transmit ID0 contains the identifier that is used when transmitting the 'On Bus' message and/or scheduled transmissions.

A zero data length 'On Bus' message is the first message transmitted by the MCP250XX after power-up and is transmitted regardless of scheduled transmission enable status.

Scheduled transmissions can contain either zero data bytes or the GPIO and A/D information.

The data field is the same as the "Read A/D Regs" "Output Message".

If you want to...

Use Schedule transmissions and send GPIO and data information.

You must...

Setup the STCON register:

• Configure the base transmission frequency (STCON.STBF1:STBF0) and the transmission multiplier (STCON.STM3:STM0).
• Configure the transmission message select for sending GPIO and A/D data (STCON.STMS = 1).
• Enable scheduled transmissions (STCON.STEN = 1).

TXID1

Transmit ID1 contains the identifier (if enabled) that is used when the MCP250XX sends:

"Command Acknowledge" message

or

"Receive Overflow" message

and/or

"Error Condition" message

COMMAND ACKNOWLEDGE

This message is sent in response to the MCP250XX receiving and processing an "Input" message which re configures the registers. This message can be thought of as a handshake for the CAN node requesting the MCP250XX modify its register(s). No data bytes are associated with Command Acknowledge messages.

RECEIVE OVERFLOW

This message is transmitted if the MCP250XX receives a message into the same buffer that a previous message was received and has not processed (e.g., the MCP250XX receives a second valid "Input" message before the first "Input" message can be processed). There is no data associated with Receive Overflow.

ERROR CONDITION

Error condition refers to the transmit and receive error counters (TEC and REC). If enabled, Error Condition is sent when TEC or REC reach "Error Warning" or "Error Passive".

The data format is the same as the "Read CAN Error" Output Message.

A seventeen count hysteresis is implemented to prevent multiple Error Condition messages from being transmitted due to the error counters hovering around the error warning or error passive trigger points (See Figure 8).

If you want to...

Enable "Command Acknowledge" and "Error Condition".

You must...

• Configure command acknowledge enable (OPTREG2.CAEN = 1)
• Configure transmit on error condition (OPTREG2.TXONEN = 1)

If you want to...

Enable "Receive Overflow" and disable "Error Condition".

You must...

• Configure command acknowledge enable (OPTREG2.CAEN = 0)
• Configure transmit on error condition (OPTREG2.TXONEN = 0)

FIGURE 8: ERROR CONDITION HYSTERESIS

	HEX	DEC	
Send Message	80	128	
	...	...	Hysteresis
	...	...	
Re-arm	6F	111	
	...	...	
	...	...	
Send Message	60	96	
	...	...	Hysteresis
	...	...	
Re-arm	79		

TXID2

Transmit ID2 contains the identifier that is used when transmitting auto-conversion initiated messages, including digital input edge detection (DIED) and/or analog input threshold detection (AITD).

DIGITAL INPUT EDGE DETECTION (DIED)

Each GPIO pin that has been configured as a digital input can be individually configured to automatically transmit a message when a predetermined edge occurs.

If you want to...

Enable automatic transmission for a falling edge on GP3.

You must...

- Configure GP3 as input (GPDDR.DDR3 = 1)
- Enable transmit on change for GP3 (IOINTEN.GP3TXC = 1)
- Set the polarity for GP3 (IOINTPO.GP3POL = 0)
- Configure ADCON1.PCFG3 = 1 for digital input

ANALOG INPUT THRESHOLD DETECTION (AITD)

Each GPIO pin that has been configured as an analog input can be individually configured to automatically transmit a message when a predefined analog threshold is reached.

If you want to...

Enable threshold detection on AN0 for going above threshold.
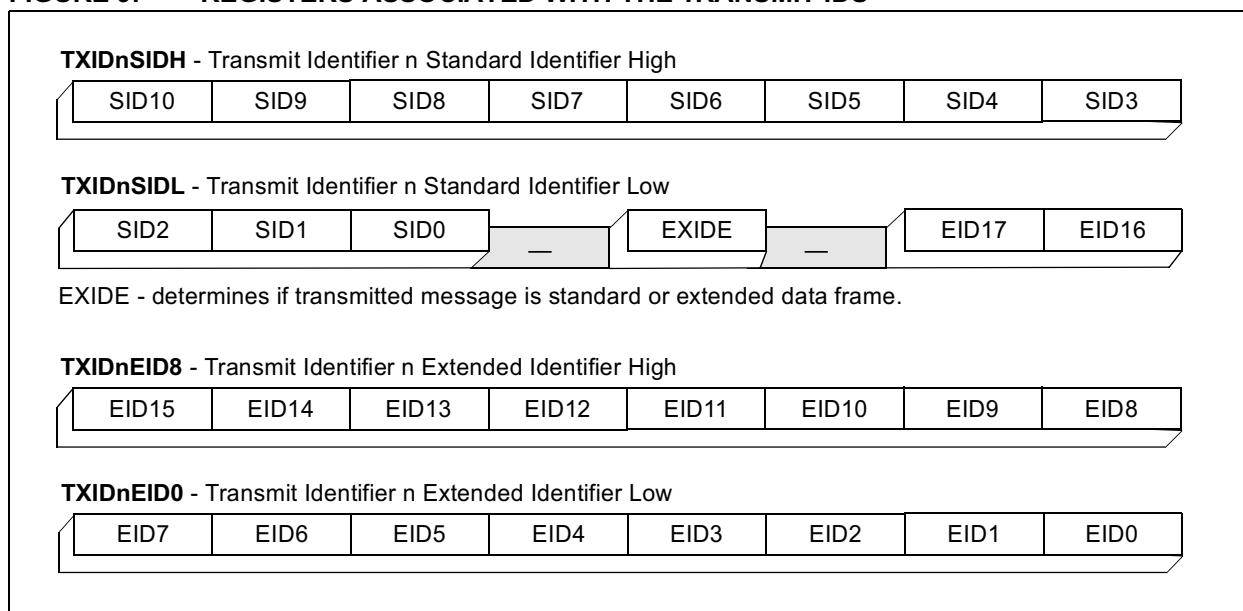
You must...

- Configure GP0 as input (GPDDR.DDR0 = 1)
- Configure GP0 as AN0 (ADCON1.PCFG0 = 0)
- Set threshold polarity to trigger on going above threshold (ADCMP0L.ADPOL = 1)
- Set threshold level (ADCMP0H and ADCMP0L)
- Set the remaining A/D configuration parameters

Transmit Message Priority

If multiple messages are pending transmission, they must be sent in order of priority. The transmit message priority is as follows:

1. "Output Messages" are in response to IRMs and have the highest transmit priority.
2. TXID2 is used when transmitting auto-conversion messages and has the second highest priority.
3. TXID1 sends the Command Acknowledge, Receive Overflow, and/or Error Condition and has the third highest priority.
4. TXID0 is used for scheduled transmissions and has the lowest priority.

FIGURE 9: **REGISTERS ASSOCIATED WITH THE TRANSMIT IDS**

TXIDnSIDH - Transmit Identifier n Standard Identifier High

SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3

TXIDnSIDL - Transmit Identifier n Standard Identifier Low

SID2	SID1	SID0	—	EXIDE	—	EID17	EID16

EXIDE - determines if transmitted message is standard or extended data frame.

TXIDnEID8 - Transmit Identifier n Extended Identifier High

EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8

TXIDnEID0 - Transmit Identifier n Extended Identifier Low

EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0

USER MEMORY

The MCP250XX allows the user to pre-program registers pertaining to CAN module and device configuration into non-volatile EPROM memory. In this way the device is initialized to a default state after power-up. The user registers are transferred to SRAM during the power-up sequence, and many of the registers are accessible via the CAN bus after the device establishes a connection with the bus. In addition, there are 16 user-defined registers that can be used to store information about the part (e.g., serial number, node identifier, etc.). The registers are summarized in Table 2. In addition, there are several registers that are not in the User Memory map but can still be read via the "Read Register" IRM (see Table 3).

There are a few things to consider with regards to the User Memory:

1. The register addresses are offset by 1Ch when transferred to SRAM after power-up.
2. The bit timing registers (CNF1, CNF2, and CNF3) cannot be modified from the original default values.
3. The GPDDR register is not offset by 1Ch. GPDDR is mapped to 1Fh after power-up.
4. The sixteen user memory registers located at addresses 35h - 44h are not transferred to SRAM at power-up and can only be read via the "Read User Mem" IRMs. These registers cannot be modified from the default conditions.
5. Changing the mask or filter registers will cause the MCP250XX to temporarily disconnect from the bus which may result in lost messages.
6. Registers associated with the mixed signal devices (MCP2505X) are not implemented on the digital only devices (MCP2502X) and will read 00h. The only exception is ADCON1 which reads 0Fh to maintain compatibility between the two device types.

If you want to...

Write to the GPLAT register

You must...

• Use address 0x1E while using the "Write Register" command

If you want to...

Read User ID bank 1.

You must...

Send an IRM with the lower three ID bits = b'101'. The MCP250XX will respond with the contents of USERID0 - USERID7 in the data field.

If you want to...

Change the bit CAN timing.

You must...

The bit timing registers cannot be modified from the default settings.

TABLE 2:   USER MEMORY MAP

Address	SRAM Address	Name	Address	SRAM Address	Name
00h	1Ch	IOINTEN	1Bh	37h	RXF0EID0
01h	1Dh	IOINTPO	1Ch	38h	RXF1SIDH
02h	1Eh	GPLAT	1Dh	39h	RXF1SIDL
03h	1Fh	Note 1	1Eh	3Ah	RXF1EID8
04h	20h	OPTREG1	1Fh	3Bh	RXF1EID0
05h	21h	T1CON	20h	3Ch	TXID0SIDH
06h	22h	T2CON	21h	3Eh	TXID0SIDL
07h	23h	PR1	22h	3Fh	TXID0EID8
08h	24h	PR2	23h	40h	TXID0EID0
09h	25h	PWM1DCH	24h	41h	TXID1SIDH
0Ah	26h	PWM2DCH	25h	42h	TXID1SIDL
0Bh	27h	CNF1 [3]	26h	43h	TXID1EID8
0Ch	28h	CNF2 [3]	27h	44h	TXID1EID0
0Dh	29h	CNF3 [3]	28h	45h	TXID2SIDH
0Eh	2Ah	ADCON0 [4]	29h	46h	TXID2SIDL
0Fh	2Bh	ADCON1 [4]	2Ah	47h	TXID2EID8
10h	2Ch	STCON	2Bh	48h	TXID2EID0
11h	2Dh	OPTREG2	2Ch	49h	ADCMP3H [4]
12h	2Eh	—	2Dh	4Ah	ADCMP3L [4]
13h	2Fh	—	2Eh	4Bh	ADCMP2H [4]
14h	30h	RXMSIDH	2Fh	4Ch	ADCMP2L [4]
15h	31h	RXMSIDL	30h	4Dh	ADCMP1H [4]
16h	32h	RXMEID8	31h	4Eh	ADCMP1L [4]
17h	33h	RXMEID0	32h	4Fh	ADCMP0H [4]
18h	34h	RXF0SIDH	33h	50h	ADCMP0L [4]
19h	35h	RXF0SIDL	34h [1]	N/A	GPDDR
1Ah	36h	RXF0EID8	35h-44h [2]	N/A	USER[0:F]

Note 1: GPDDR is mapped to 1Fh is SRAM and not offset by 1Ch.

2: User memory (35h-44h) is not transferred to RAM on powerup and can only be accessed via "Read User Mem" and "Write Register" commands.

3: Cannot be modified from initial programmed values.

4: Unimplemented in digital only devices (MCP250XX) and read 00h with the exception of ADCON1 = 0Fh.

TABLE 3:   ACCESSIBLE REGISTERS NOT IN THE USER MEMORY MAP

Addr*	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Value on POR	Value on RST
18h	EFLG	ESCF	RBO	TXBO	TXEP	RXEP	TXWAR	RXWAR	EWARN	0000 0000	0000 0000
19h	TEC	Transmit Error Counters								0000 0000	0000 0000
1Ah	REC	Receive Error Counters								0000 0000	0000 0000
50h	ADRES3H	AN3.9	AN3.8	AN3.7	AN3.6	AN3.5	AN3.4	AN3.3	AN3.2	xxxx xxxx	uuuu uuuu
51h	ADRES3L	AN3.1	AN3.0	—	—	—	—	—	—	xx-- ----	uu-- ----
52h	ADRES2H	AN2.9	AN2.8	AN2.7	AN2.6	AN2.5	AN2.4	AN2.3	AN2.2	xxxx xxxx	uuuu uuuu
53h	ADRES2L	AN2.1	AN2.0	—	—	—	—	—	—	xx-- ----	uu-- ----
54h	ADRES1H	AN1.9	AN1.8	AN1.7	AN1.6	AN1.5	AN1.4	AN1.3	AN1.2	xxxx xxxx	uuuu uuuu
55h	ADRES1L	AN1.1	AN1.0	—	—	—	—	—	—	xx-- ----	uu-- ----
56h	ADRES0H	AN0.9	AN0.8	AN0.7	AN0.6	AN0.5	AN0.4	AN0.3	AN0.2	xxxx xxxx	uuuu uuuu
57h	ADRES0L	AN0.1	AN0.0	—	—	—	—	—	—	xx-- ----	uu-- ----

* These addresses are used when using the "Read Register" command (i.e., no offset)

GPIO MODULE

The MCP250XX has eight general purpose input/output (GPIO) pins (GP0 to GP7) collectively labeled GPIO. All GPIO port pins have TTL input levels and full CMOS output drivers, with the exception of GP7, which is input only.

All of the pins are multiplexed with an alternate function, including analog-to-digital conversion on up to four of the GPIO pins, analog VREF inputs on up to two pins, PWM outputs on up to two pins, clock out function, and external reset (Figure 10). The operation of each pin is selected by clearing or setting control bits in various control registers. GPIO pin functions are summarized in Table 4.

TABLE 4: GPIO FUNCTIONS

Name	Bit#	Function
GP0/AN0	bit0	I/O or analog input
GP1/AN1	bit1	I/O or analog input
GP2/AN2/PWM2	bit2	I/O, analog input, or PWM out
GP3/AN3/PWM3	bit3	I/O, analog input, or PWM out
GP4/VREF-	bit4	I/O or analog voltage reference
GP5/VREF+	bit5	I/O or analog voltage reference
GP6/CLKOUT	bit6	I/O or Clock output
GP7/nRST/VPP	bit7	Input, external reset input, or programming voltage input

There are several functions/capabilities of the GPIO module while configured as digital I/O (see Figure 11):

Digital Input or Digital Output

With the exception of GP7 which is input only, each pin can be individually configured as digital input or digital output.

Internal Pull-up Resister

Each pin has a weak internal pull-up resistor. All pull-up resistors can be turned on/off for all pins configured as a digital inputs. The resistors are automatically turned off for each pin configured as an output.

Digital Input Edge Detection

As discussed previously, all pins configured as a digital input can be configured to initiate a CAN transmission when a predefined edge occurs.
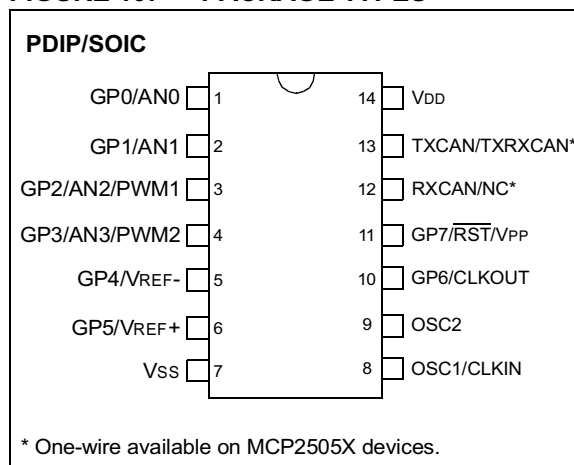
If you want to...

- Configure GP7 - GP4 as digital inputs and GP3 - GP0 as digital outputs.
- Enable pull-up resistors
- Default all outputs to logic zero
- Use edge detection for GP7 and GP6.
  GP7 = rising edge and GP6 = falling edge.

You must...

- Configure GPDDR = b'x111 0000'
- Configure OPTREG1.$\overline{GPPU}$ = 0
- Configure GPLAT = b'xxxx 0000'
- Configure IOINTEN = b'1100 0000'
- Configure IOINTPO = b'10xx xxxx'

FIGURE 10: PACKAGE TYPES

PDIP/SOIC

GP0/AN0	1	14 VDD
GP1/AN1	2	13 TXCAN/TXRXCAN*
GP2/AN2/PWM1	3	12 RXCAN/NC*
GP3/AN3/PWM2	4	11 GP7/$\overline{RST}$/VPP
GP4/VREF-	5	10 GP6/CLKOUT
GP5/VREF+	6	9 OSC2
VSS	7	8 OSC1/CLKIN

* One-wire available on MCP2505X devices.

FIGURE 11: REGISTERS ASSOCIATED WITH THE GPIO FUNCTIONS

GPDDR - Data Direction Register

--	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0

GPLAT - Latch Register

--	GP6	GP5	GP4	GP3	GP2	GP1	GP0

IOINTEN - Edge Detection Enable Register

GP7TXC	GP6TXC	GP5TXC	GP4TXC	GP3TXC	GP2TXC	GP1TXC	GP0TXC

IOINTPO - Edge Detection Polarity Register

GP7POL	GP6POL	GP5POL	GP4POL	GP3POL	GP2POL	GP1POL	GP0POL

OPTREG1 - Option 1 Register

GPPU	CLKEN	CLKPS1	CLKPS0	--	CMREQ	AQT1	AQT0

GPPU - Enables/Disables the weak internal pull-up resistors. Only used with digital inputs.

ADCON1 - A/D Control Register 1

ADCS1	ADCS0	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0

PCFG3:PCFG0 - Configures GP3 - GP0 as analog or digital. Set bits = 1 for digital

PWM MODULES

There are two Pulse Width Modulation (PWM) modules that generate up to 10-bit resolution. Each PWM can be separately enabled and each has its own timer, duty cycle, and period registers.

PWM States at Power-up

The PWM outputs are disabled during power-up to prevent invalid signals from occurring on the PWM outputs. The PWM outputs enable after successful power-up (i.e., after the default user configuration is transferred to SRAM).

PWM State After Lost CAN Communication

The PWM outputs can be forced to their default POR states if CAN communication is lost, and more specifically, if communication with the master control node is lost. This function is enabled via OPTREG2.PDEFEN and by setting scheduled transmissions via the STCON register.

If enabled, the MCP250XX will set the PWMs back to the power-up default states if a message is not received by the MCP250XX for a predefined time. This includes if the bus is still active, however, the MCP250XX is not receiving any messages, or if all CAN communication is lost.

Configuring the PWM Modules

Two parameters must be configured for the PWMs to function as desired:

1. PWM Period.
2. PWM Duty Cycle.

PWM PERIOD

The PWM period is specified by writing to the 8-bit period (PRn) register. The PWM period is calculated using the following equation:

$$PWM\ period\ =\ [(PRn) + 1] \times 4T_{OSC} \times (TMRn\ prescale\ value)$$

$$PWM\ frequency\ =\ \frac{1}{(PWM\ period)}$$

where:

> *PRn* = 8-bit period register (0 - 255)
>
> *TMRn prescale* = 1, 4, or 16 as defined in TnCON.TnCKPS1:TnCKPS0
>
> *TOSC* = clock period on OSC1 pin

PWM DUTY CYCLE

The PWM Duty Cycle is specified by writing to the 8-bit PWMnDCH and 2-bits of the TnCON registers for up to 10-bits of resolution. The upper eight bits are contained in PWMnDCH and the lower two bits are contained in TnCON. The PWM duty cycle is calculated using the following equation:

$$PWM\ DC\ =\ (PWMnDC) \times T_{OSC} \times (TMRn\ prescale\ value)$$

where:

> *PWMnDC* = PWMnDCH + TnCON.DCnB1:DCnB0 (0 - 1023)
>
> *TMRn prescale* = 1, 4, or 16 as defined in TnCON.TnCKPS1:TnCKPS0
>
> *TOSC* = clock period on OSC1 pin

If you want to...

- Configure PWM1 period = max
- Configure PWM1 DC = 0.5PWMperiod
- Enable return to defaults on lost CAN communication

You must...

- Configure PR1 = FFh
  T1CON.T1CKPS1:T1CKPS0 = b'1x' (prescaler = 16)
- Configure PWM1DCH = 7Fh
  T1CON.DC1B1:DC1B0 = b'11'
- Enable the return to default feature:
  OPTREG2.PDEFEN = 1
- Setup the STCON register
  Configure the base transmission frequency (STCON.STBF1:STBF0) and the transmission multiplier (STCON.STM3:STM0)

> **Note:** Scheduled transmissions must be enabled for the PWM return to defaults feature to function. Therefore, the MCP250XX will transmit messages at regular intervals.

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FIGURE 12: REGISTERS ASSOCIATED WITH THE PWM MODULES

GPDDR - Data Direction Register

--	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
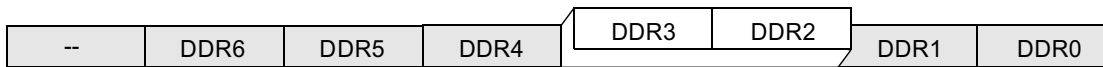
DDR3:DDR2 - configure as outputs for PWM

TnCON - PWM Control Registers 1 and 2

TMRnON	--	TnCKPS1	TnCKSP0	--	--	DCnB1	DCnB0

TMRnON - on/off
TnCKPS1:TnCKPS0 - Timer prescaler
DCnB1:DCnB0 - Two lowest bits of the 10-bit duty cycle.

PRn - Period Register

PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
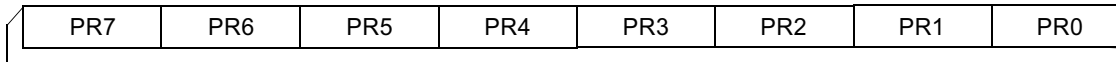
PWMnDCH - Upper 8-bits of 10-bit Duty Cycle Register

DCnB9	DCnB8	DCnB7	DCnB6	DCnB5	DCnB4	DCnB3	DCnB2

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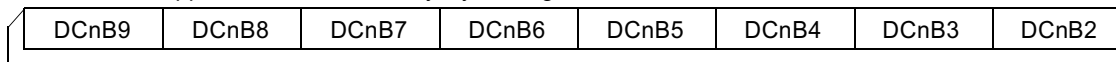
A/D MODULE

The analog-to-digital (A/D) module is a four channel, 10-bit successive approximation type of A/D. The A/D allows conversion of an analog input signal to a corresponding 10-bit number. This module is available on the MCP250XX devices only (MCP25050 and MCP25055).

Configuring the A/D Module

To configure an A/D channel:

• Configure appropriate pin to input (GPDDR)
• Configure port configuration control bits (ADCON1.PCFG3:PCFG0)
• Configure the conversion rate (ADCON0.T0PS2:T0PS0)
• Configure the voltage reference (ADCON1.VCFG1:VCFG0)
• Configure the conversion clock for the acquisition time (ADCON1.ADCS2:ADCS0)
• Enable/disable analog threshold detection (IOINTEN)
• Configure the polarity if needed (IOINTPO)
• Setup compare registers for threshold detection as needed (ADCMPnH and ADCMPnL)

A/D Operation

There are three modes of operation that can be individually selected for each enabled analog channel.

1. Auto-Conversion Mode.
2. Conversion-on Request Mode.
3. Scheduled Transmission Mode.

AUTO-CONVERSION MODE

Auto-conversion mode is automatically enabled if any A/D channel is enabled and is used for Analog Input Threshold Detection.

An A/D conversion is sequentially performed for each pin that is configured as an analog input. The conversion sequence is AN0, AN1, AN2, and AN3.

The conversion rates are determined by a timer and a prescaler. The timer value is based on the prescaler configuration and is not directly configurable. The formula for the auto conversion rate is:

$$Auto\ Conversion\ Rate\ =\ 1024 \times T_{OSC} \times Prescale\ Rate$$

The prescaler is configured in ADCON0.T0PS2:T0PS0. Some typical conversion rates are shown in Table 5.

CONVERSION-ON REQUEST MODE

A Conversion-On Request occurs when an A/D conversion is preformed in response to a "Read A/D Regs" IRM. This mode operates independently of auto-conversion mode.

When a "Read A/D Regs" IRM is received, the MCP250XX performs an A/D conversion on all enabled channels and sends the result.

Analog Input Threshold Detection

As discussed in the Device Overview section, the MCP250XX can detect if a predefined analog threshold is exceeded (both magnitude and polarity) and transmit a message.

SCHEDULED TRANSMISSION MODE

The MCP250XX can send A/D converted data using the Scheduled Transmission function (STCON) and configuring STCON.STMS = 1.

TABLE 5: **TYPICAL AUTO CONVERSION RATES**

T0PS[2:0]	Prescale Rate	Auto-Conversion Rate (ms)				
		4 MHz	8 MHz	10 MHz	16 MHz	20 MHz
000	1:32	0.255	0.127	0.102	0.064	0.051
001	1:64	2	1	0.820	0.500	0.410
010	1:128	10	5	4	2.5	2
011	1:256	35	17	14	8.5	7
100	1:512	1300	650	52	32	26
101	1:1024	2630	1300	105	65	52
110	1:2048	5250	2630	210	132	105
111	1:4096	10500	5250	420	262	210

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FIGURE 13:   REGISTERS ASSOCIATED WITH THE A/D MODULE

GPDDR - Data Direction Register

--	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0

DDR3:DDR0 - must be set as input for each enabled analog channel

IOINTEN - Threshold Detection Enable

GP7TXC	GP6TXC	GP5TXC	GP4TXC	GP3TXC	GP2TXC	GP1TXC	GP0TXC

GP3TXC:GP0TXC - Enables/disables the threshold detection.
          0 = triggers when A/D goes below the threshold.

IOINTPO - Threshold Detection Polarity

GP7POL	GP6POL	GP5POL	GP4POL	GP3POL	GP2POL	GP1POL	GP0POL

GP3POL:GP0POL - Determines the threshold polarity. 0 = triggers when A/D goes below the threshold

ADCON0 - A/D Control Register 0

--	T0PS1	T0PS1	T0PS0	--	--	--	--

T0PS1:T0PS0 - Prescale select bits for A/D conversion loop

ADCON1 - A/D Control Register 1

ADCS1	ADCS0	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0

PCFG3:PCFG0 - Configures GP3 - GP0 as analog or digital. Cleart bits = 0 for analog.
VCFG1:VCFG0 - Voltage reference select bits.
ADCS1:ADCS0 - A/D conversion select bits.

ADCMPnH - Upper 8-bits of the A/D Compare Register

ANnCMP.9	ANnCMP.8	ANnCMP.7	ANnCMP.6	ANnCMP.5	ANnCMP.4	ANnCMP.3	ANnCMP.2

Configures the digital representation of the analog compare value used for Analog Threshold Detection.

ADCMPnL - Lower 2-bits of the 10-bit A/D Compare Register

ANnCMP.1	ANnCMP.0	--	--	--	--	--	--

ANnCMP.1:ANnCMP.0 - Configures the lower 2-bits of the digital representation of the analog compare
          value used for Analog Threshold Detection.

SUMMARY

Microchip's CAN I/O expanders are an effective solution for many applications where a simple remote CAN node is needed. The MCP250XX is configured with a set of user defaults. No firmware needs to be written or debugged, making the MCP250XX a quick solution as well as a cost effective solution compared to MCU based CAN nodes.

NOTES:

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