
Power Considerations for the TC4864 Audio Power Amplifier

*Author: Jack Braden
Microchip Technology Inc.*

INTRODUCTION

Power is one of the major considerations in portable, battery-powered applications because of battery life and heat. Since the Audio Power Amplifier (APA) is an important power dissipating building block used in end applications such as cellular telephones, notebook computers, Personal Data Assistants (PDAs), Compact Disc (CD) and Digital Video Disc (DVD) Players, it is worth gaining a clearer understanding of its limitations and ability to deliver power to a load. Once these limitations and abilities are clearly understood, one will be better equipped in determining important parameters such as output power and the resulting Output Sound Pressure Level (SPL) produced by a speaker, input power and the resulting power supply requirements, and package power dissipation and the resulting die junction temperature.

This application note quantifies each of these important parameters and provides supporting empirical data acquired using the TC4864 in the Bridge Tied Load (BTL) topology and the Single-Ended Capacitively Coupled Load (SECCL) topology. The BTL topology, as will be shown, is the preferred topology because it can deliver more output power to the load before clipping occurs. This is especially useful in low voltage portable systems where the necessary peak-to-peak voltage swing across the load is greater than the available system power supply voltage. The SECCL APA topology is necessary for applications, such as headsets, that contain a speaker (or speakers) and microphone that share the same ground return.

TC4864 AUDIO POWER AMPLIFIER OVERVIEW

The TC4864 is a Class AB Bridged APA capable of delivering a continuous average output power, P_{OUT} , of 300 mW ($V_{DD} = 5V$, $T_A = +25^{\circ}C$, $f = 1$ kHz) into an 8 Ω BTL with a maximum Total Harmonic Distortion Plus Noise (THD+N) of 1%. The maximum P_{OUT} is only slightly greater and is approximately 307 mW and is a consequence of the package power dissipation, P_D , of 595 mW that results in a maximum die junction temperature, T_{JMAX} , of $150^{\circ}C$ assuming a typical junction-to-

ambient thermal resistance, θ_{JA} , for a board mounted MSOP-8 package of approximately $210^{\circ}C/W$. The relationship between output power and package power dissipation will be presented and discussed in detail later in this application note.

The TC4864 has a shutdown pin that can be used to put the part in an extremely "low power" shutdown mode where the quiescent power supply current, I_{DDQ} , drops from a typical value of 4.1 mA to a typical value of $0.1 \mu A$ ($V_{DD} = 5V$, $T_A = +25^{\circ}C$, $V_{IN} = 0V$, no load). Depending on the system requirements, a microcontroller can put the part in shutdown mode during periods of "audio inactivity", thereby conserving battery power and reducing heat dissipation. This quiescent power supply current must and will be considered later on in this application note when input power, power dissipation, efficiency and die junction temperature calculations are discussed.

SPEAKER IMPEDANCE

Before moving on to a discussion of the output power, it is beneficial to gain a fundamental understanding of the load impedance presented by a typical speaker since it is this impedance that is ultimately used in the calculation to determine the output power.

There are many types of speaker technologies available with moving coil: (a.k.a. dynamic), electromechanical, and piezoelectric (pressure electricity) being the three most popular. Of these three, the moving coil speaker is probably the most widely used and will, therefore, be discussed in some detail.

An equivalent circuit model can be used to represent the load impedance presented by a typical speaker. In general, this equivalent circuit model contains multiple inductors, resistors and capacitors. Most speaker manufacturers do not specify what the equivalent circuit model should be in order to properly model the speaker's actual impedance vs. frequency. Some of these impedance vs. frequency curves are fairly complicated looking because they can have multiple mechanical and electrical resonant frequencies (especially the piezoelectric speakers).

Piezoelectric speakers basically look like a big capacitor ranging from a few nF up to a hundred nF or so. Basically, a dynamic voltage is applied across a crystal or ceramic material that results in a mechanical strain

AN794

or deflection. One of the benefits of the Piezoelectric speaker is that it does not create a magnetic field, which might be unacceptable in some applications.

Electromechanical speakers look like a complex impedance whose magnitude ranges from a few ohms up to several hundred ohms or so. The electromechanical speaker is composed of a stationary ferrite or ceramic magnet, a stationary coil, and a cone made up of some type of magnetic material. A dynamic voltage is applied across the stationary coil creating a dynamic magnetic field that basically modulates the static magnetic field created by the stationary magnet. The resulting magnetic field then mechanically deflects the magnetic cone material.

The moving coil speaker also looks like a complex impedance whose magnitude ranges from a few ohms up to a hundred ohms or so. The moving coil speaker is composed of a stationary ferrite or ceramic magnet, a moving coil, and a cone that can be made of a plethora of materials. A dynamic voltage is applied across the moving coil via a pair of small, flexible conductors creating a dynamic magnetic field that interacts with the static magnetic field created by the stationary magnet. This magnetic field interaction deflects the moving coil in addition to the cone since the two are mechanically connected together.

The impedance of a moving coil speaker is made up of four parts:

1. The Moving Coil Resistance, R_{COIL} .
2. The Moving Coil Inductive Reactance, X_{COIL} .
3. The Motional Resistance, R_{MOT} .
4. The Motional Reactance, X_{MOT} .

The sum of R_{COIL} and X_{COIL} is referred to as the Moving Coil Impedance, Z_{COIL} , and the sum of R_{MOT} and X_{MOT} is referred to as the Motional Impedance, Z_{MOT} . The sum of Z_{COIL} and Z_{MOT} is the Moving Coil Speaker Equivalent Impedance, Z_E .

The Moving Coil Speaker Equivalent Circuit Model is shown in [Figure 1](#).

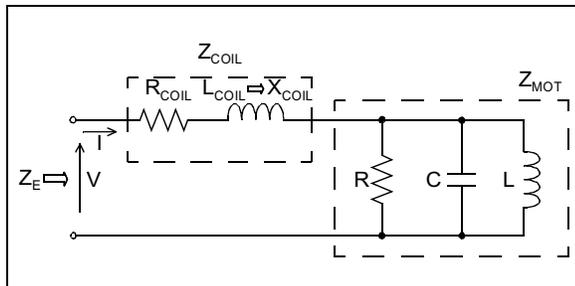


FIGURE 1: Moving Coil Speaker Equivalent Circuit Model.

The equations describing this Equivalent Circuit Model are given by:

Moving coil speaker equivalent impedance:

$$Z_E = \frac{V}{I} = Z_{COIL} + Z_{MOT} \quad [1]$$

Moving coil impedance:

$$Z_{COIL} = R_{COIL} + jX_{COIL} \quad [2]$$

Motional impedance:

$$Z_{MOT} = R_{MOT} + jX_{MOT} \quad [3]$$

Motional resistance:

$$R_{MOT} = \frac{1/R}{\frac{1}{R^2} + \left(\omega C - \frac{1}{\omega L}\right)^2} \quad [4]$$

Motional reactance:

$$X_{MOT} = \frac{\omega C - \frac{1}{\omega L}}{\frac{1}{R^2} + \left(\omega C - \frac{1}{\omega L}\right)^2} \quad [5]$$

A detailed discussion of each of the components in the equivalent circuit model and the terms in these equations is beyond the scope of this application note; however, the following qualitative statements are worth mentioning:

- R_{COIL} is the resistance and L_{COIL} is the inductance of the very long, thin wire making up the moving coil.
- R , C and L making up $Z_{MOT} = R_{MOT} + jX_{MOT}$ are extremely complicated and depend on many factors such as frequency, mass and stiffness of the moving coil and cone, radius of the cone, the static magnetic field produced by the stationary magnet, the length of wire making up the voice coil, etc.

A typical plot of the magnitude of the moving coil speaker equivalent impedance, $|Z_E|$, vs. frequency, f , for the CUI Stack, P/N GF0501M, is shown in [Figure 2](#). Notice from this plot that there is a sudden rise in the impedance at a frequency of about 540 Hz. This sudden rise is due to the speaker's mechanical resonance, and f_o denotes the mechanical resonance frequency. As the frequency increases beyond f_o , the rise in impedance is due to the inductance of the moving coil. As a rule of thumb, the rated impedance of a moving coil speaker is near the frequency where electrical resonance occurs. Electrical resonance occurs at a frequency beyond f_o where the impedance is at a minimum. This electrical resonance frequency is denoted by f_R and, from the plot in [Figure 2](#), occurs at a frequency of about 1 kHz. The speaker's impedance

for a narrow bandwidth around f_R is fairly constant, and because of this constancy, most manufacturers of moving coil speakers do not specify the exact frequency (sometimes they do) at which the speaker has its rated impedance. In general, a speaker's rated impedance is measured at a frequency somewhat above f_R and is normally larger than the moving coil resistance, R_{COIL} . Most people are familiar with these values because they are fairly standard - 4 Ω , 8 Ω , 16 Ω , 32 Ω , etc. R_{COIL} is slightly less than these values and is typically around 5 Ω or so for a speaker with a rated impedance of 8 Ω .

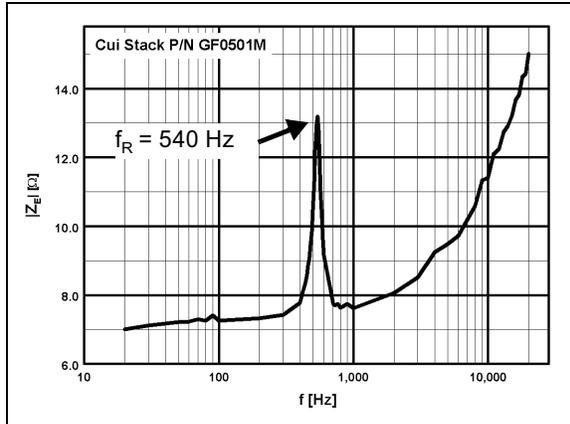


FIGURE 2: $|Z_E|$ vs. f for the CUI Stack, P/N GF0501M moving coil speaker.

What does one do with all of this information? It is important to understand that it is the moving coil speaker's equivalent impedance, Z_E , which will be used as the load, R_L , to calculate the TC4864's output power later on in this application note. Although not shown here, Z_E is mostly resistive (real) for the majority of frequencies less than f_R for moving coil speakers. It is this reason that most manufacturers of APAs perform testing and characterization using simple resistive loads. The simple resistive load is fairly standard among the audio community when specifying and characterizing an APA.

DROPOUT VOLTAGE

An important consideration for an APA is its ability to apply an undistorted voltage across a load. One of the parameters that limits this ability is the APA's ability to drive the output voltage as close as possible to either power supply rail without clipping, which can result in significant distortion.

The dropout voltage is a measure of an APA's "Head-room" and is typically defined as the magnitude of the difference between the positive or negative supply voltage rail and output voltage when clipping occurs such that the Total Harmonic Distortion Plus Noise (THD+N) of the voltage across the load is less than or equal to 1%. In equation form, these definitions are:

Positive supply voltage rail dropout voltage:

$${}^+V_D = \left| {}^+V - {}^+V_C \right| \quad [6]$$

Negative supply voltage rail dropout voltage:

$${}^-V_D = \left| {}^-V - {}^-V_C \right| \quad [7]$$

Where:

- ${}^+V \equiv$ Positive Supply Voltage Rail (V_{DD} for the TC4864)
- ${}^-V \equiv$ Negative Supply Voltage Rail (0V for the TC4864)
- ${}^-V_C \equiv$ Positive Output Clipping Voltage ($<V_{DD}$ for the TC4864)
- ${}^-V_C \equiv$ Negative Output Clipping Voltage ($>0V$ for the TC4864)

Of course, a perfect APA has dropout voltages of 0V. Dropout voltages greater than 0V are the result of voltage drops across the output stage transistors. For the TC4864, ${}^+V_D$ and ${}^-V_D$ are approximately equal and increase as the supply voltage increases. See the TC4864 data sheet for typical plots of the "Dropout Voltage vs. Supply Voltage". The data sheet plots labeled "Top Side" and "Bottom Side" are the same as ${}^+V_D$ and ${}^-V_D$ respectively. The data for these plots was gathered for a differential voltage gain, A_{VD} , of 2 with an 8 Ω BTL. The input signal level was increased until the V_{O1} output voltage just begins to start clipping and then the dropout voltages were calculated using equations 6 and 7. For a supply voltage of 5V, ${}^+V_D$ is typically around 1V, and ${}^-V_D$ is typically around 0.9V. Since ${}^+V_D$ is greater than ${}^-V_D$ for the TC4864, "Top Side" clipping will occur first and then the input signal level will need to be increased slightly to get "Bottom Side" clipping to occur.

A couple of typical V_{O1} time domain output voltage waveforms are shown in Figures 3 and 4 for clipping levels that result in THD+Ns of 1% and 10%, respectively. V_{O1} as viewed by a spectrum analyzer in the frequency domain for each of these output voltage waveforms can be seen in Figures 5 and 6, respectively.

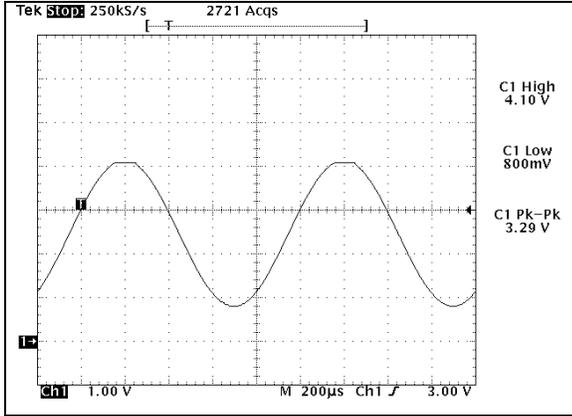


FIGURE 3: V_{O1} vs. t . for the TC4864 ($V_{DD} = 5V$, $A_{VD} = 2$, 8Ω BTL, $f = 1$ kHz, $THD+N = 1\%$).

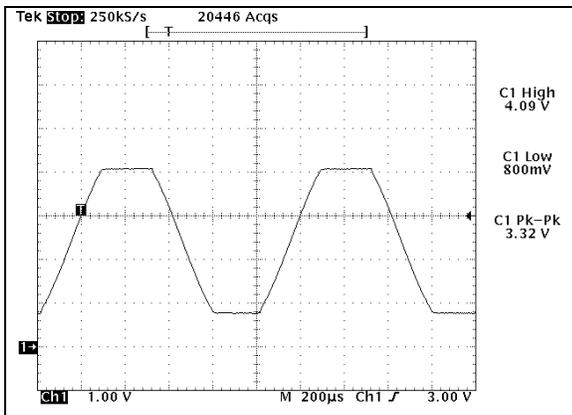


FIGURE 4: V_{O1} vs. t . for the TC4864 ($V_{DD} = 5V$, $A_{VD} = 2$, 8Ω BTL, $f = 1$ kHz, $THD+N = 10\%$).

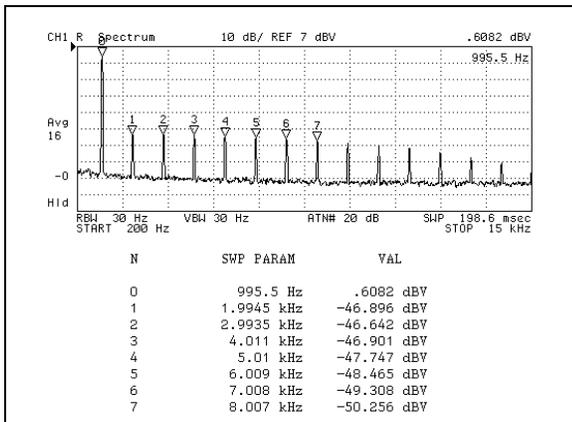


FIGURE 5: V_{O1} vs. f . for the Time Domain waveform in Figure 3 ($THD+N = 1\%$).

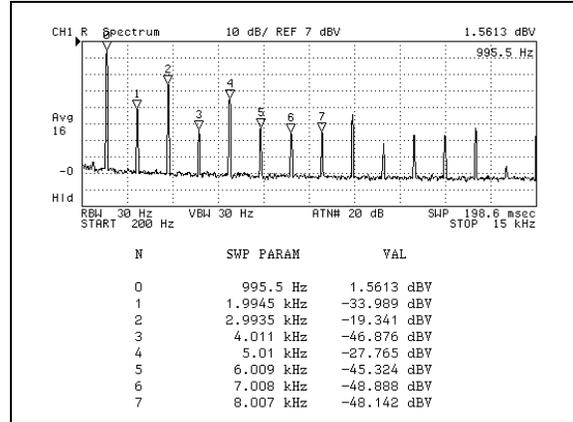


FIGURE 6: V_{O1} vs. f . for the Time Domain waveform in Figure 3 ($THD+N = 10\%$).

The definitions for Total Harmonic Distortion (THD) and Total Harmonic Distortion Plus Noise, $THD+N$, are given by:

$$\% THD = \frac{\sqrt{H_2^2 + H_3^2 + \dots + H_N^2}}{\sqrt{H_1^2 + H_2^2 + H_3^2 + \dots + H_N^2}} \times 100 \quad [8]$$

$$\%(THD + N) = \frac{\sqrt{H_2^2 + H_3^2 + \dots + H_N^2 + e_n^2}}{\sqrt{H_1^2 + H_2^2 + H_3^2 + \dots + H_N^2 + e_n^2}} \times 100 \quad [9]$$

Where:

$H_1^2 \equiv$ Mean Squared Voltage of Fundamental Frequency

$H_N^2 \equiv$ Mean Squared Voltage of N^{th} Harmonic Frequency

$e_n^2 \equiv$ Mean Squared Noise Voltage

The %THD can be estimated from the frequency domain plots in Figures 5 and 6 and can be calculated using the amplitudes for markers 1-7 (2nd - 8th order harmonics respectively). The results yield a %THD of 0.998% for Figure 5 and 9.764% for Figure 6. The slight deviations from the expected $THD+N$ values of 1% and 10%, respectively are due to the fact that the remaining higher order harmonics and noise were not included in the calculations. Most audio analyzers, such as the Agilent 8903B, measure $THD+N$ and have selectable bandwidth limiting, low-pass filters. For example, the 8903B has a 30 kHz or 80 kHz low-pass filter that can be selected to allow the user to reduce the number of harmonics used in the measurement.

The human ear is capable of detecting a THD as low as 0.6% due to only the 2nd order harmonic and 0.25% due to only the 3rd order harmonic. As odd as it might seem, distorted signals containing only a small amount of 2nd order harmonic distortion are actually perceived as being more "musical" by the human ear. It is the

higher order harmonics such as the 7th, 9th, 11th and 13th that are perceived as more objectionable by the human ear. These higher order harmonics are referred to as the "Dissonant Harmonics", and it is these harmonics that contribute to the deterioration of sound quality resulting from output signal clipping.

It is important that the designer clearly understand dropout voltages and the range of the input signal level, so the TC4864's gain can be adjusted accordingly to avoid excessive clipping of the output signal. Also, dropout voltages will increase with temperature, so appropriate heatsinking measures should be taken to reduce the TC4864's die junction temperature, T_J . This will be discussed later in this application note.

OUTPUT POWER

Calculating the output power, P_{OUT} , for the BTL and SECCL topologies is fairly straightforward. Typical BTL and SECCL topologies using the TC4864 can be seen in Figure 9, and the output voltage waveforms for these topologies can be seen in Figures 7 and 8, respectively. For both topologies, the input signal, V_{IN} was set to $0.5V_p$ ($1V_{P-P}$), and the external gain setting resistors, R_F and R_I were made equal to $20\text{ k}\Omega$. For the BTL topology, this yields a differential voltage gain of $A_{VD} = -2(R_F/R_I) = -2$, and for the SECCL topology, this yields a voltage gain of $A_V = -R_F/R_I = -1$.

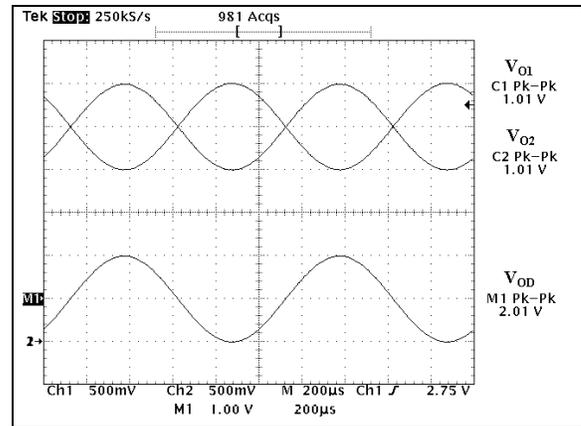


FIGURE 7: Output voltage waveforms for the typical BTL Topology in Figure 9.

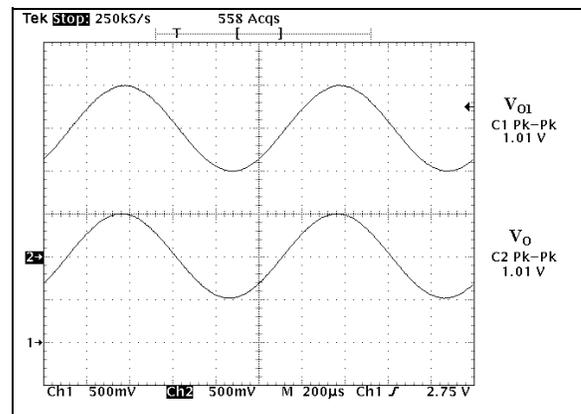


FIGURE 8: Output voltage waveforms for the typical SECCL topology in Figure 9.

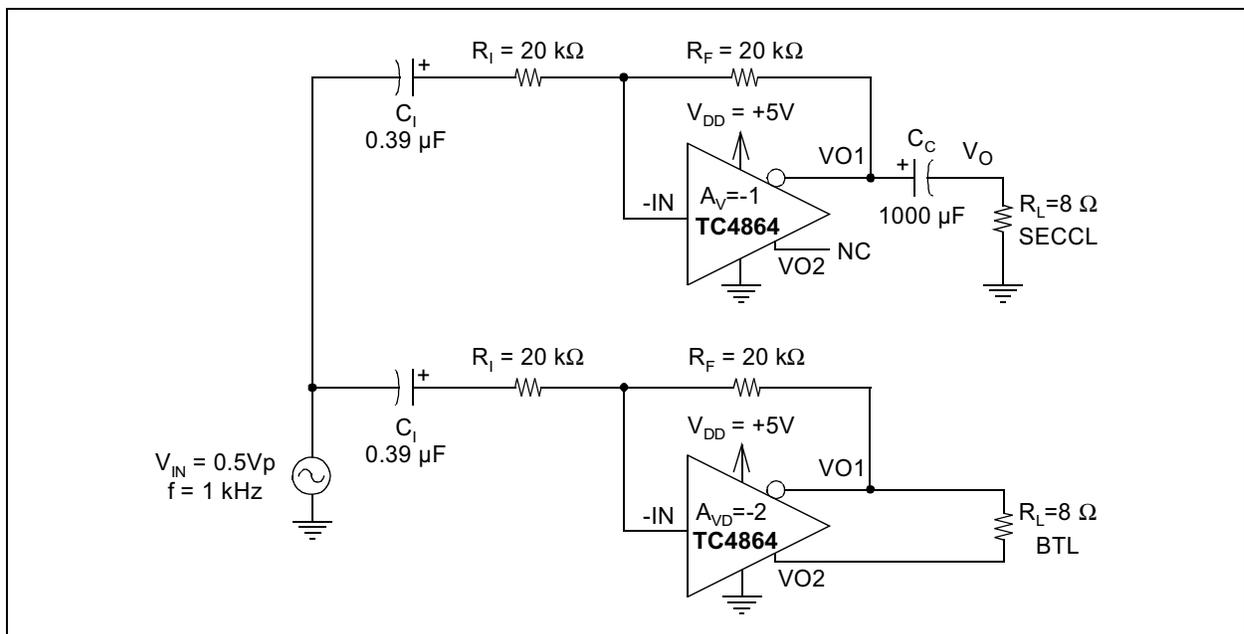


FIGURE 9: Typical BTL and SECCL topologies using the TC4864.

AN794

The equations for calculating P_{OUT} for both topologies are:

BTL:

$$P_{OUT} = \frac{\left(\frac{A_{VD}V_{IN_p}}{\sqrt{2}}\right)^2}{R_L} + \frac{V_{OS}^2}{R_L} = \frac{A_{VD}^2V_{IN_p}^2}{2R_L} + \frac{V_{OS}^2}{R_L} \quad [10]$$

SECCL:

$$P_{OUT} = \frac{\left(\frac{A_VV_{IN_p}}{\sqrt{2}}\right)^2}{R_L} = \frac{A_V^2V_{IN_p}^2}{2R_L} \quad [11]$$

Where:

$V_{IN_p} \equiv$ Peak Input Voltage

Differential Voltage Gain:

$$A_{VD} = \frac{V_{O1} - V_{O2}}{V_{IN}} = \frac{V_{OD}}{V_{IN}} = -2\frac{R_F}{R_I}$$

Voltage Gain:

$$A_V = \frac{V_O}{V_{IN}} = -\frac{R_F}{R_I}$$

The additional term in the P_{OUT} equation for the BTL topology is due to the differential output offset voltage, V_{OS} . V_{OS} is defined as the difference between the V_{O1} and V_{O2} DC output voltages when the input voltage, $V_{IN} = 0V$. For the TC4864, V_{OS} is typically only 5 mV, so it only contributes slightly to P_{OUT} when a practical load is connected. For an 8 Ω load, this term would typically only be 3.125 μW , which can basically be ignored; however, it will contribute to the quiescent power supply current, I_{DDQ} , as will be discussed in more detail in the section on input power. Notice that the P_{OUT} equation for the SECCL topology does not include this V_{OS} term because of the AC coupling (DC blocking) output capacitor, C_C .

Some comments regarding the BTL and SECCL topologies are in order. As can be seen from Figure 9, the SECCL topology requires a very large coupling capacitor, C_C . This capacitor is needed to remove the TC4864's DC bias voltage of $V_{DD}/2$ that appears at V_{O1} (see Figure 8). If C_C were not used, then large DC currents would flow through the speaker resulting in a large moving coil and cone displacement. This displacement will have an impact on the speaker's dynamic range of motion before severe distortion occurs. Also, depending on the speaker's maximum input power, this large DC current could permanently damage the speaker's moving coil. Of course, C_C increases cost, takes up PCB real estate, and creates a low frequency breakpoint, f_L , given by $1/(2\pi R_L C_C)$. Large values of C_C are normally required in order to set f_L at some reasonable value. For example, for an R_L of 8 Ω , a C_C of 1000 μF is required for an f_L of 20 Hz, or for an f_L of 200 Hz, C_C need only be 100 μF . Unfortunately, some applications require the SECCL topology,

such as headsets which contain a speaker (or speakers) and microphone that share the same ground return. Careful study of equations 10 and 11 will show that the BTL topology results in twice the voltage swing across the load and four times the power delivered to the load before clipping of the output voltage occurs. This is especially useful in low voltage portable systems where the necessary peak-to-peak voltage swing across the load is greater than the available system power supply voltage.

In conclusion of this section, P_{OUT} is important for a couple of reasons. First, the package power dissipation, P_D , is a function of P_{OUT} . Understanding this relationship is important when calculating the die junction temperature, as we shall see later on. Second, P_{OUT} is the input power to the speaker being driven. This input power must be appropriate so as not to damage the speaker, and it is also important because the Output Sound Pressure Level, SPL, produced by the speaker is usually specified at some input power. For example, the CUI Stack P/N GF0501M mentioned earlier, is rated for a maximum input power of 1 W and a nominal input power of 0.5 W. The SPL at a distance 50 cm away from the speaker is specified as 84 dB \pm 3 dB at this nominal input power of 0.5 W. Understanding how this SPL relates to P_{OUT} and how P_{OUT} depends on the input signal, V_{IN} , is important in determining the gain for the TC4864.

INPUT POWER

The input power, P_{IN} , is the power delivered to the TC4864 by the V_{DD} system power supply and must first be determined before one can calculate the APA's efficiency, η , which will be discussed shortly. Also, knowing the P_{IN} requirements assists in determining the overall V_{DD} system power supply requirements.

For the typical BTL and SECCL topologies presented earlier in Figure 9, waveforms for the power supply current, I_{DD} , in relation to the output voltage waveforms can be seen in Figures 10 and 11.

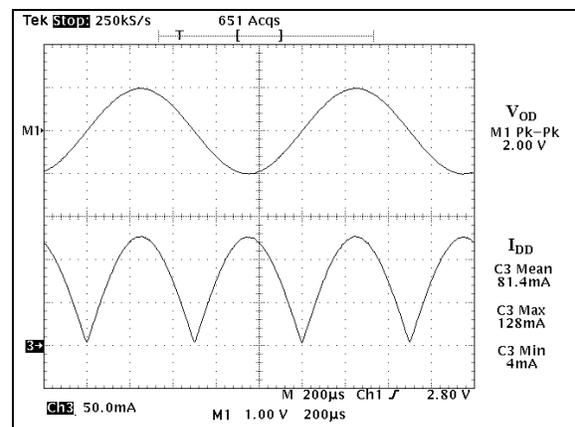


FIGURE 10: Power supply current waveform for the typical BTL topology in Figure 9.

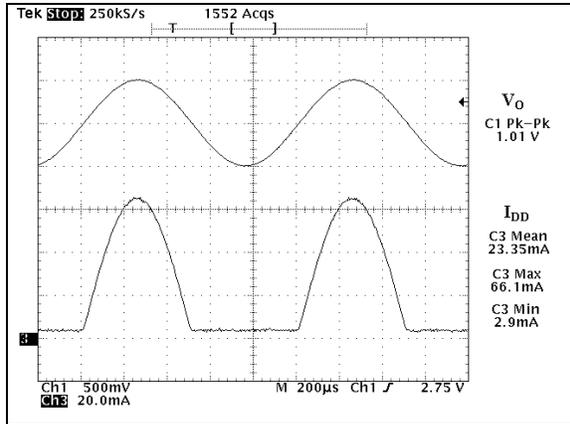


FIGURE 11: Power supply current waveform for the typical SECCL topology in Figure 9.

The equations for calculating the peak power supply current, I_{DDp} , and average power supply current, $\overline{I_{DD}}$, for both topologies are:

BTL: Peak V_{DD} power supply current

$$\text{Where: } I_{DDp} = \frac{V_{ODp}}{R_L} = \frac{|A_{VD}|V_{INp}}{R_L} \quad [12]$$

$V_{ODp} \equiv$ Peak Differential Output Voltage

BTL: Average V_{DD} power supply current

$$\overline{I_{DD}} = \frac{2I_{DDp}}{\pi} \quad [13]$$

SECCL:

$$\text{Where: } I_{DDp} = \frac{V_{Op}}{R_L} = \frac{|A_V|V_{INp}}{R_L} \quad [14]$$

$V_{Op} \equiv$ Peak Output Voltage

SECCL:

$$\overline{I_{DD}} = \frac{I_{DDp}}{\pi} \quad [15]$$

These relationships are useful when determining the V_{DD} system power supply requirements.

The equations for calculating P_{IN} for both topologies are:

BTL:

$$P_{IN} = V_{DD}\overline{I_{DD}} = V_{DD}\frac{2|A_{VD}|V_{INp}}{\pi R_L} + V_{DD}I_{DDQ} \quad [16]$$

SECCL:

$$P_{IN} = V_{DD}\overline{I_{DD}} = V_{DD}\frac{|A_V|V_{INp}}{\pi R_L} + V_{DD}I_{DDQ} \quad [17]$$

Where:

$I_{DDQ} \equiv$ Quiescent Power Supply Current

The additional term in the P_{IN} equations is due to the quiescent power supply current, I_{DDQ} . I_{DDQ} is the additional power supply current needed to power circuitry internal to the TC4864 such as the bias current for the output stage transistors, and for the BTL topology, it includes any additional load current resulting from the differential output offset voltage, V_{OS} . Since V_{OS} is typically 5 mV, the contribution to I_{DDQ} for an 8 Ω load is approximately 0.625 mA. This additional load current does not exist for the SECCL topology because of the AC coupling (DC blocking) output capacitor; therefore, I_{DDQ} for the BTL topology will always be greater than it is for the SECCL topology. This can be seen by looking at the minimum values for I_{DDQ} in Figures 10 and 11.

Studying equations 16 and 17 and ignoring the terms containing I_{DDQ} shows that for the same V_{DD} , V_{INp} , R_F and R_i , the BTL topology results in four times the input power. In reality, since I_{DDQ} is not equal to zero, this ratio will be less than four. This can be empirically verified from Figures 10 and 11. From Figure 10, $P_{IN} = (5V)(81.4 \text{ mA}) = 0.407 \text{ W}$ for the BTL topology, and from Figure 11, $P_{IN} = (5V)(23.35 \text{ mA}) = 0.117 \text{ W}$ for the SECCL topology; therefore, this ratio is more typically around $0.407 \text{ W}/0.117 \text{ W} \approx 3.5$.

A concluding point needs to be made concerning I_{DDQ} . Since the TC4864 has a shutdown pin, the part can be put in an extremely "low power" shutdown mode where I_{DDQ} drops from a typical value of 4.1 mA to a typical value of 0.1 μA ($V_{DD} = 5V$, $T_A = +25^\circ\text{C}$, $V_{IN} = 0V$, no load). Depending on the system requirements, a microcontroller can put the part in shutdown mode during periods of "audio inactivity", thereby conserving battery power and reducing heat dissipation for power sensitive portable applications.

PACKAGE POWER DISSIPATION

The package power dissipation, P_D , is the power actually dissipated by the TC4864 and is simply the difference between the input power, P_{IN} , and output power, P_{OUT} . Calculation of this parameter is necessary in determining the die junction temperature, T_J , to see if it falls within an acceptable range. This will be discussed in detail later in the section entitled "Die Junction Temperature Calculations".

The equations for P_D are found by subtracting equations 10 from 16 for the BTL topology and equations 11 from 17 for the SECCL topology. The results are:

BTL:

$$P_D = \frac{2\sqrt{2}V_{DD}}{\pi\sqrt{R_L}}\sqrt{P_{OUT} - \frac{V_{OS}^2}{R_L}} - P_{OUT} + V_{DD}I_{DDQ} \quad [18]$$

SECCL:

$$P_D = \frac{\sqrt{2}V_{DD}}{\pi\sqrt{R_L}}\sqrt{P_{OUT} - P_{OUT} + V_{DD}I_{DDQ}} \quad [19]$$

Theoretical typical plots of P_D vs. P_{OUT} can be seen in Figures 12 and 13 for the BTL and SECCL topologies respectively for several common resistive load values ($R_L = 4 \Omega$, 8Ω and 16Ω) at a $V_{DD} = +5V$. Also, typical values were used for the differential output offset voltage ($V_{OS} = 5 mV$) and the quiescent power supply current ($I_{DDQ} = 4.1 mA$).

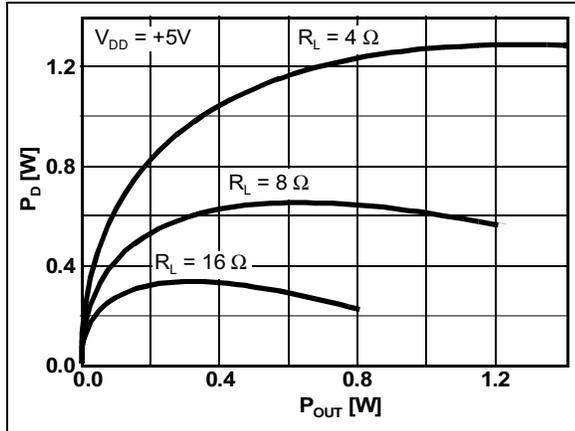


FIGURE 12: Theoretical typical plots of P_D vs. P_{OUT} for the BTL topology.

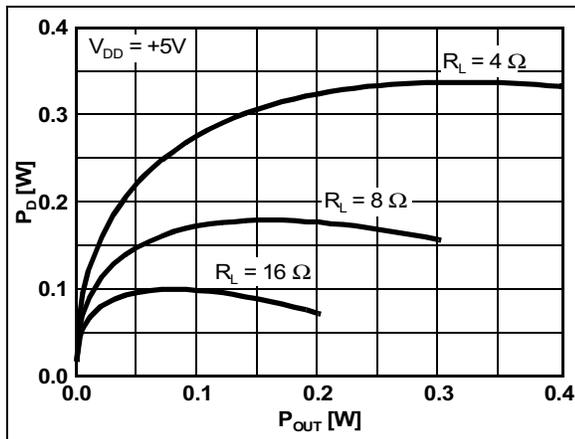


FIGURE 13: Theoretical typical plots of P_D vs. P_{OUT} for the SECCL topology.

Empirical data plots of P_D vs. P_{OUT} for the TC4864 can be seen in Figures 14 and 15 for the BTL and SECCL topologies respectively for several common resistive load values ($R_L = 4 \Omega$, 8Ω and 16Ω) at a $V_{DD} = +5V$. Appropriate heatsinking measures were taken in the acquisition of this empirical data so as not to exceed the TC4864's maximum die junction temperature, T_{JMAX} . More will be discussed about this topic in the section entitled "Die Junction Temperature Calculations".

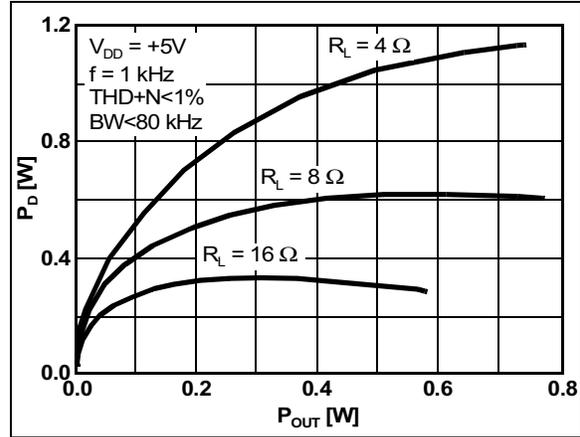


FIGURE 14: Empirical data plots of P_D vs. P_{OUT} for the TC4864 for the BTL topology.

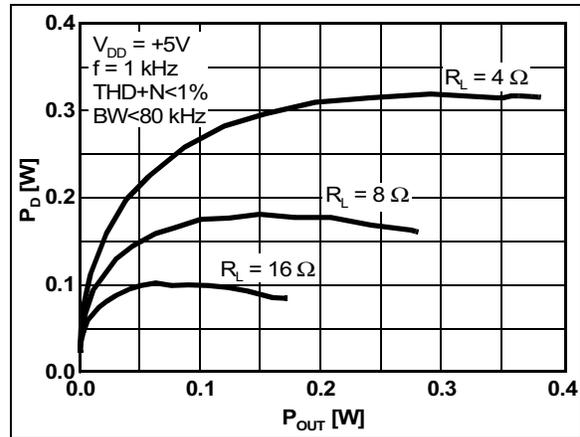


FIGURE 15: Empirical data plots of P_D vs. P_{OUT} for the TC4864 for the SECCL topology.

As can be seen from the theoretical and empirical data plots of P_{OUT} vs. P_D , there is a value of P_{OUT} for which P_D is a maximum for each R_L . The theoretical values can be found by taking the partial derivative of P_D with respect to P_{OUT} , setting the partial derivative equal to zero and then solving for the maximum package power dissipation, P_{DMAX} . The results of performing this operation for both topologies are:

BTL:

$$P_{DMAX} = \frac{2V_{DD}^2}{\pi^2 R_L} + \frac{V_{OS}^2}{R_L} + V_{DD}I_{DDQ} \quad [20]$$

SECCL:

$$P_{DMAX} = \frac{V_{DD}^2}{2\pi^2 R_L} + V_{DD}I_{DDQ} \quad [21]$$

The P_{OUT} values corresponding to these $P_{D_{MAX}}$ values are:

BTL:

$$P_{OUT} = \frac{2V_{DD}^2}{\pi^2 R_L} + \frac{V_{OS}^2}{R_L} @ P_{D_{MAX}} \quad [22]$$

SECCL:

$$P_{OUT} = \frac{V_{DD}^2}{2\pi^2 R_L} @ P_{D_{MAX}} \quad [23]$$

As an example, for $V_{DD} = +5V$ and $R_L = 8 \Omega$, $P_{D_{MAX}} = 654 \text{ mW}$ with a resulting $P_{OUT} = 633 \text{ mW}$ for the BTL topology, and $P_{D_{MAX}} = 179 \text{ mW}$ with a resulting $P_{OUT} = 158 \text{ mW}$ for the SECCL topology. These values can be approximately verified by studying the theoretical typical plots in Figures 12, and 13 and the empirical data plots in Figures 14 and 15. Typically (no heatsinking) a P_{OUT} of 633 mW for the BTL topology and 158 mW for the SECCL topology will be difficult to achieve with the TC4864 due to excessive die junction temperature and clipping of the output voltage. As previously mentioned, appropriate heatsinking measures were taken in the acquisition of the empirical data so as not to exceed the TC4864's maximum die junction temperature, $T_{J_{MAX}}$. Heatsinking of the TC4864 will also increase the output voltage swing before clipping occurs.

What does one do with $P_{D_{MAX}}$? For input signals where the amplitude is uncontrolled or unpredictable, as is the case with most music or voice-band signals, the value obtained for $P_{D_{MAX}}$ from either equations 20 or 21 is the conservative value to use when calculating the die junction temperature. For input signals where the amplitude is controlled or predictable, as is the case with alert tones, the value obtained for P_D from either equations 18 or 19 is the appropriate value to use when calculating the die junction temperature. This calculation will be discussed in detail in the "Die Junction Temperature Calculations" section.

EFFICIENCY

The efficiency, η , of an APA is defined as the ratio of P_{OUT} to P_{IN} . This is easily accomplished by taking the ratio of equations 10 and 16 for the BTL topology and equations 11 and 17 for the SECCL topology. The results are:

BTL:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{|A_{VD}| V_{IN_p} \pi}{2V_{DD}} \quad [24]$$

SECCL:

$$\eta = \frac{|A_{V}| V_{IN_p} \pi}{2V_{DD}} \quad [25]$$

As counterintuitive as it might seem, manipulation of equations 16, 17, 24 and 25 will show that for the same input power, the SECCL topology is actually twice as efficient as the BTL topology. In other words, more power is being dissipated by the package, and less power is being delivered to the load. For this reason, when using the TC4864 in the BTL topology, it is especially important to be mindful of the die junction temperature as will be discussed in the next section.

DIE JUNCTION TEMPERATURE CALCULATIONS

The die junction temperature, T_J , is an extremely important parameter since operation at elevated temperatures for extended periods of time results in decreased device reliability which can eventually lead to complete device failure.

Also, reduction of T_J will increase the TC4864's output voltage swing before clipping occurs.

The ever so familiar die junction temperature equation is given by:

$$T_J = T_A + P_D \theta_{JA} \quad [26]$$

Therefore,

$$P_D = \frac{T_J - T_A}{\theta_{JA}} \quad [27]$$

For $T_J = T_{J_{MAX}} = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$ and $\theta_{JA} = 210^\circ\text{C/W}$, $P_D = 595 \text{ mW}$. The resulting P_{OUT} can be solved for in equation 18 and is fairly complicated, so the details are omitted. The "theoretical" result for the BTL topology under the conditions $V_{DD} = 5V$ and $R_L = 8 \Omega$ is:

$$8\Omega \text{ BTL: } P_{OUT} = 307 \text{ mW, and } 1.077 \text{ W}$$

As odd as it might seem, for the BTL topology, there are actually two "theoretical" solutions for P_{OUT} . This can be seen by studying Figure 12 in the "Package Power Dissipation" section. In practice, however, the TC4864 can never reach 1.077 W due to clipping of the output voltage. Therefore, for the BTL topology, $P_{OUT} = 307 \text{ mW}$ for a $T_{J_{MAX}} = 150^\circ\text{C}$. The SECCL topology was not considered since it is not possible for P_D to equal 595 mW under these conditions ($V_{DD} = 5V$ and $R_L = 8 \Omega$) as can be seen by studying Figure 13 in the "Package Power Dissipation" section.

It should be apparent that by decreasing θ_{JA} , $P_{D_{MAX}}$ and/or T_A can be increased. The easiest way to decrease θ_{JA} is by connecting large traces or power and ground planes to the device's V_{DD} and GND pins. A technique often overlooked or not even considered is removal of the solder mask from these traces and planes close to the device which allows them to dissipate power more efficiently which also aids in decreasing θ_{JA} .

CONCLUSIONS

The TC4864 APA is a small, cost effective solution for low voltage portable applications where the need for large, clean output drive voltages is needed. A clear understanding of the basic *"Powerful"* principles set forth in this application note are crucial for a high performance audio design that is both efficient and reliable.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, KEELoQ, SEEVAL, MPLAB and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

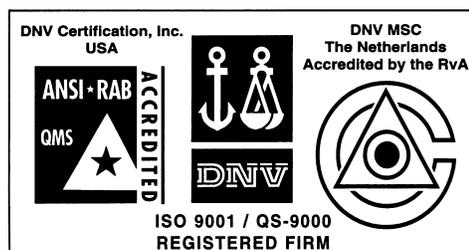
Total Endurance, ICSP, In-Circuit Serial Programming, Filter-Lab, MXDEV, microID, FlexROM, fuzzyLAB, MPASM, MPLINK, MPLIB, PICC, PICDEM, PICDEM.net, ICEPIC, Migratable Memory, FanSense, ECONOMONITOR, Select Mode and microPort are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Term Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2001, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



MICROCHIP

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta

500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Austin - Analog

8303 MoPac Expressway North
Suite A-201
Austin, TX 78759
Tel: 512-345-2030 Fax: 512-345-6085

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Boston - Analog

Unit A-8-1 Millbrook Tarry Condominium
97 Lowell Road
Concord, MA 01742
Tel: 978-371-6400 Fax: 978-371-0050

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Rm. 531, North Building
Fujian Foreign Trade Center Hotel
73 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7557563 Fax: 86-591-7557572

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong

Microchip Technology Hongkong Ltd.
Unit 901, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessy Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Germany - Analog

Lochamer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895650-0 Fax: 49-89-895650-22

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

06/01/01