

## Integrating Converter Analog Processor – TC500A

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### ADC PROVIDES FLEXIBLE PROGRAM CONTROL

Today, design engineers rely more on microprocessors and microcontrollers to support their applications. Compatible analog-to-digital (A/D) and digital-to-analog (D/A) converters have greatly increased the flexibility of interface and control circuits.

Most of the available converters, however, are “independent” and not subject to reconfiguration under software control — no matter how smart your processor. For example, if your task involves 8-bit conversions of battery voltage and 16-bit conversions of output voltage, you are required to use two different converters — or take 16 bits of time to measure your battery.

The TC500A converter from Microchip Technology, Inc. is not as independent as other converters. In fact, the TC500A only performs operations as instructed by your processor. If the initial circuit

configuration (component values and layout) is reasonable — using the rules of the data sheets for component and timing values — the TC500A converts an input to any resolution up to 16 bits (plus sign). The proper design can allow the processor to select and control the conversion parameters.

### TRADE-OFF

The usual trade-off for analog-to-digital (A/D) conversion is resolution versus speed. In many cases a low degree of accuracy is all that is necessary for a given conversion. For maximum flexibility, you need a single converter to speed up when low accuracy is required.

The TC500A is a converter that lets you control the resolution-speed trade-off. It is an analog processor that permits you to program the rate and resolution of A/D conversions. The TC500A performs the dual-slope portion of an A/D conversion and lets you write software so your microprocessor or computer can handle the digital tasks.

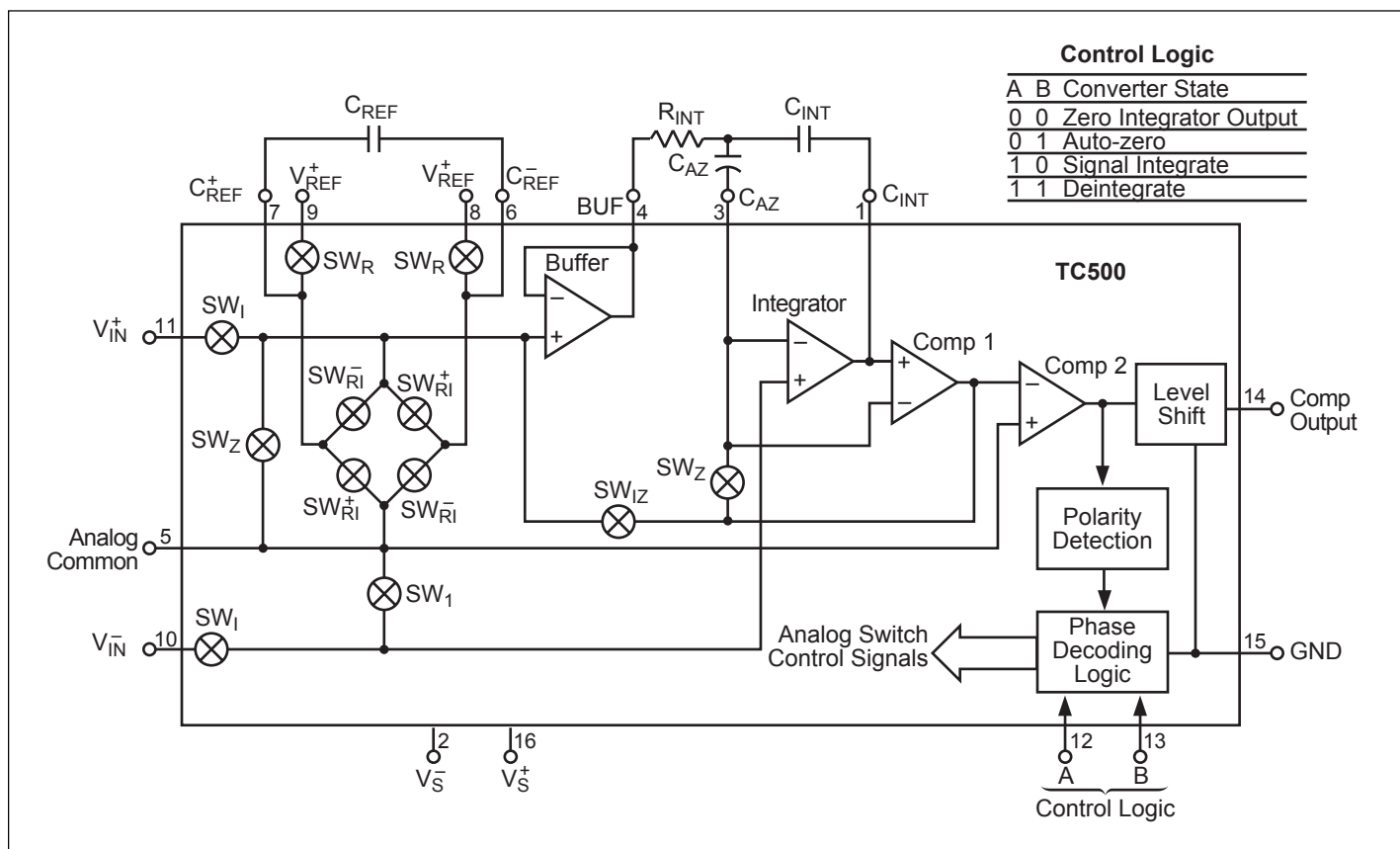


FIGURE 1: Functional diagram.

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In short, this low-power CMOS device lets your software program fearlessly trade-off between high resolution (16 bits plus sign) and speed of conversion.

## FOUR-PHASE CONVERSION FOR BUILDING AN APPLICATION

The TC500A incorporates four separate conversion phases. Two select pins on the TC500A control the timing and sequencing of these phases.

### Phase I — Input Integration

Causes the integration capacitor to charge at a rate determined by the input voltage. The duration of this phase is a fixed amount of time.

### Phase II — Reference Deintegration

Causes the integration capacitor to discharge at a rate determined by the reference voltage. A zero crossing signals the end of conversion and the comparator output goes low. The amount of time required for the zero crossing is proportional to the input voltage.

### Phase III — System Zero

Forces the integration capacitor to be restored to the ground reference potential. This phase may be used to correct cases where the input voltage of Phase I is so large that the Phase II does not have enough time to complete its cycle. This is an over-range condition. Also, the reference capacitor is charged to the reference voltage during this phase.

### Phase IV — Auto Zero

Causes the auto-zero capacitor to be charged to a value that represents the combination of all internal offset errors. The resulting error is then cancelled by the action of Phases I and II. The reference capacitor is also charged during this phase as in Phase III.

## OUTPUT

The output of the TC500A is from one pin (comparator output) that shows the phase of the input voltage (plus/minus) or indicates that Phase II is complete (the integration capacitor has discharged to the ground reference potential). This output also determines when Phase III is complete. The comparator switches back to the supply voltage when the excess charge has been removed.

## COMPLETING THE CONVERSION PROCESS

### Step I — System Zero

Select Phase III and wait for the comparator output to go positive. This tells you that the system is zeroed.

### Step II — Auto Zero

Select Phase IV for at least the same amount of time as Phase I, but for as long as you like. This charges the reference capacitor and establishes a conversion offset in opposition to the internal offsets.

This phase is the place to recall the count obtained in Step 4 (Phase II), then calculate and display the input voltage.

### Step III — Input Integration

Select Phase I for an exact amount of known time and read the comparator output just prior to ending the phase. If it is high, a positive voltage has been converted. If it is low, the input is negative.

### Step IV — Reference Deintegration

Select Phase II and count intervals. Stop counting as soon as the comparator output goes low. Save the count and go directly back to Step I (Phase III).

Calculation:

$$V_{IN} = V_{REF}$$

where:

$$\begin{aligned} T_{DEINT} &= \text{Reference voltage integration time (variable)} \\ T_{ITN} &= \text{Signal integration time (fixed)} \\ V_{REF} &= \text{Reference voltage} \end{aligned}$$

Note that  $T_{INT}$  must be exact and can be any value.  $T_{DEINT}$  is the variable that determines  $V_{IN}$ .

## DISPLAYING THE RESULTS

First, convert the Phase II count on BCD values, then convert the BCD values to ASCII characters. Finally, send the ASCII characters to the screen, the printer, the disk file, or some other device.

## RESOLUTION

The actual resolution (counts per deintegration period) available from the TC500A is a function of how many counts you can put into the Phase II cycle when converting the maximum input voltage. The rate of deintegration is determined by the reference voltage. A lower reference voltage reduces the deintegration slope and allows time for more counts.

## ACCURACY

Internal noise and time-dependent errors determine the conversion accuracy (signal-to-noise ratio) of the TC500A. The dominant source of error is the  $1/f$  noise of the buffer, integration amplifier and comparator. You can reduce some of the effect by increasing the integration time (Phase I) and the deintegration time (Phase II). You can reduce the errors caused by broadband (thermonic) noise by increasing  $V_{REF}$ . You can reduce errors caused by stray capacitance by "guarding" the integrating capacitor.

## A WORD OF CAUTION

Avoid using an edge-triggered interrupt in applications where you plan to convert very low input voltages. The output of the comparator may not have enough time to complete a full transition.

## COMPONENT SELECTION EXAMPLE

### Known

- Supply voltage for TC500A ( $V_{SUP}$ )
- Maximum input voltage ( $V_{IN(MAX)}$ )
- Integration time ( $T_{INT}$ )
- Output resolution (bits) ( $N$ )
- Clock period ( $t_{CLOCK}$ )

### Assume

- $V_{SUP} = \pm 5V$      $V_{SUP} = [V_{SUP}]$
- $V_{IN(MAX)} = \pm 2.5V$      $V_{IN(MAX)} = [V_{IN(MAX)}]$
- $T_{INT} = 40msec$
- $N = 14$  bits
- $t_{CLOCK} = 4\mu sec$

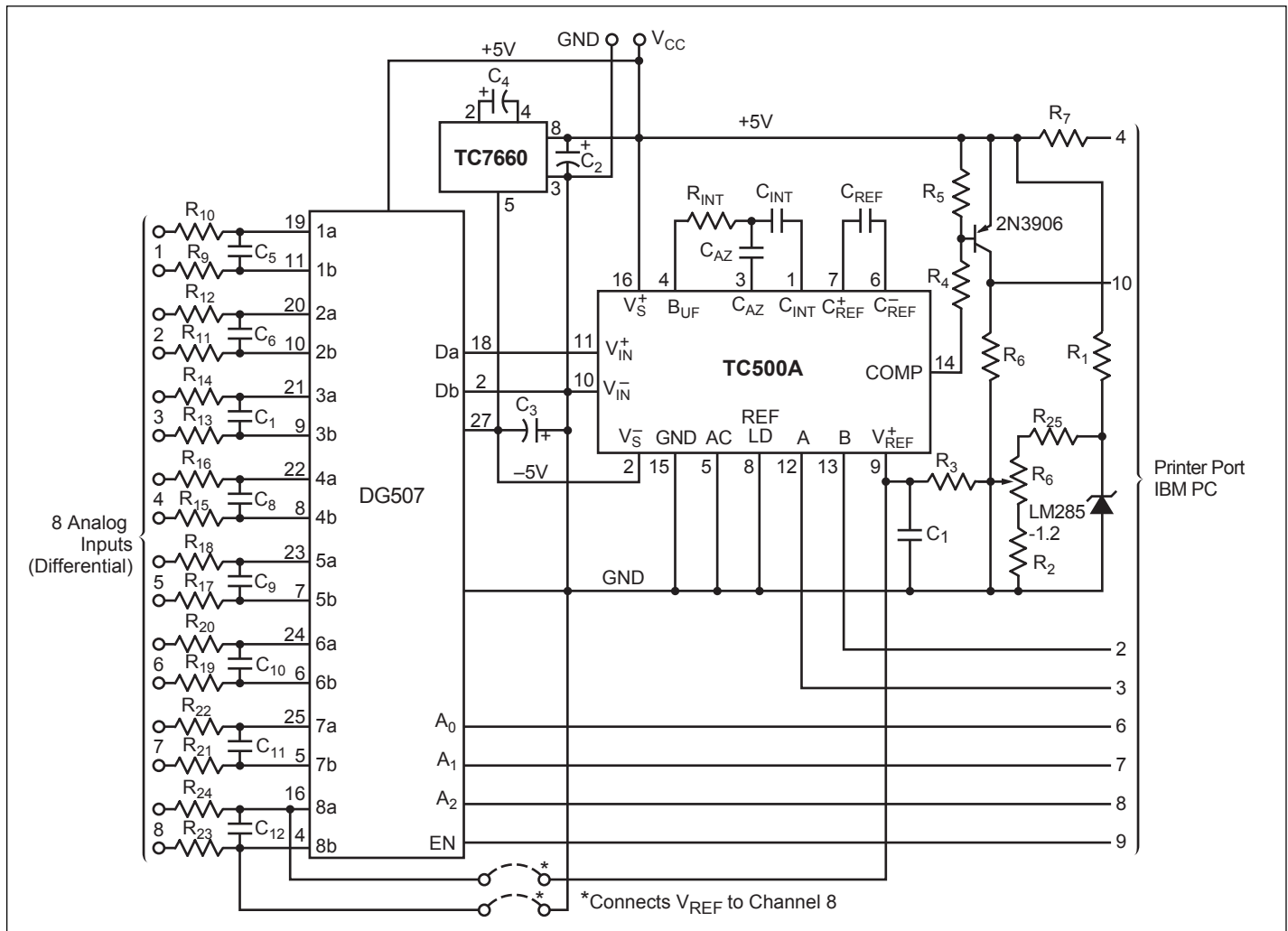


FIGURE 2: Applications.

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## Step 1 — Calculate $R_{INT}$

$$R_{INT} = \frac{V_{IN (MAX)}}{I_{BUF (MAX)}}$$

where:  $I_{BUF (MAX)} \approx 10\mu A$

$$R_{INT} = \frac{2.5V}{10\mu A} = 250K$$

## Step 2 — Calculate $C_{INT}$

$$C_{INT} = \frac{T_{INT} I_{BUF}}{V_{INT(MAX)}}$$

where:  $V_{INT} = V_{SUP} - 1V = 4V$

$$R_{INT} = \frac{40msec \ 10\mu A}{4V} = 0.1\mu F$$

## Step 3 — Calculate $V_{REF}$

$$V_{REF} = \frac{V_{INT} C_{INT} R_{INT}}{T_{DEINT}}$$

where:  $V_{DEINT} = 2^N t_{CLOCK}$

$$R_{INT} = \frac{4V \ 0.1\mu F \ 250K}{2^N t_{CLOCK}} = 1.525\dots V$$

## Step 4 — Calculate Integrate Count ( $K_{INT}$ )

$$K_{INT} = \frac{T_{INT}}{t_{CLOCK}}$$

$$K_{INT} = \frac{40msec}{4\mu sec} = 10,000 \text{ counts}$$

## Results

$$K_{DEINT} = V_{REF} \frac{K_{INT}}{V_{REF}} = V_{IN} \frac{10,000}{1.525\dots V}$$

where:  $K_{DEINT}$  = number of clock periods during  $T_{DEINT}$

## NORMALIZATION

The reference voltage can be adjusted to scale the deintegrate count to be directly equivalent to the input voltage.

Since:

$$\frac{K_{INT}}{V_{REF}} = \text{counts/volt},$$

if:  $V_{REF}$  is adjusted such that

$$V_{REF} = \frac{K_{INT}}{10,000 \text{ counts/volt}} = \frac{10,000 \text{ counts}}{10,000 \text{ counts/volt}} = 1V,$$

then:  $K_{DEINT} = \frac{V_{IN}}{100\mu V}$  and  $N \approx 14.61$  bits

Example: If  $K_{DEINT} = 18,357$  counts,  
then  $V_{IN} = 1.8357$  volts

## CONCLUSION

The TC500A is a very flexible analog-to-digital conversion tool. This converter gives control to the microprocessor (which should know more about what it should do than it does). The programming techniques presented here will allow you to develop the software to run the TC500A on any number of currently available processors.

## THE PROGRAM (MICROSOFT® MACRO ASSEMBLER)

The parallel printer port is used here for convenience. Its address is assumed to be 0378 Hex (SELECT).

- Bits 0 and 1 select the conversion phase
- Bit 3 is the comparator output from the TC500A (inverted)
- Bit 4 through 7 select the input channel

These routines are examples of 8088/86/286 source code. Here are the constants and variables:

SCALAR — Actual integration count determined by the resolution  
CNLSEL — Shifted high nibble that selects the channel  
VALUE — Value of the input voltage in binary format  
SIGN — Sign bit saved for evaluation comparator delay  
CORFAC — Correction factor that compensates for comparator delay

**Phase I — Input Integration Mode**

Charges the integrator capacitor at a rate determined by the input voltage for a fixed duration.

CX = Fixed duration reference count  
 AL = Select INT mode and channel (output to port)  
 DX = Port address

Exit mode when CX = 0  
 (Disable interrupts to prevent background routines from interfering.)

```

INTGRT:      CLI                                ;Disable interrupts
              MOV          CX,SCALAR          ;Get integration duration
              SUB          CX,CORFAC         ;Correct delay error
              MOV          AL,OF1H          ;Select INT mode
              ADD          AL,CNLSEL         ;Select channel
              MOV          DX,SELECT        ;Select output port
              OUT          DX,AL            ;Select Phase I
INTGLP:      LOOP          INTGLP           ;Decrease CX and continue until CX = 0
              IN           AL,DX            ;Read sign bit
              MOV          SIGN,AL          ;Save sign
  
```

FIGURE 3: Phase I.

**Phase II — Reference Deintegration (DEINT)**

Discharges the integrator capacitor at a rate determined by the reference voltage.

CX = Countdown timer (determines value of input)  
 AL = Select DEINT mode and channel (output to port)  
 DX = Port address

Exit mode when bit 3 = 1 or CX decrements to 0 (interrupts remain disabled)

```

DEINTG:      MOV          CX,0              ;Maximum duration
              MOV          AL,OF3H         ;Select DEINT mode
              ADD          AL,CNLSEL         ;Select channel
              MOV          DX,SELECT        ;Select output port
              OUT          DX,AL            ;Select Phase II
DILOOP:      IN           AL,DX            ;Read port
              TEST         AL,8             ;Test comparator bit (bit 3)
              LOOPZ        DILOOP           ;Decrease CX, continue if CX > 0 or save bit 3 = 0
              MOV          CXVAL,CX         ;Save count for later evaluation
  
```

FIGURE 4: Phase II.

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## Phase III — System Zero (IZ)

Remove excess charge from the integrator capacitor and the auto-zero capacitor.

CX = Maximum duration

AL = Select IZ mode and channel (output to port)

DX = Port address

Exit mode when bit 3 = 0 or CX decrements to 0.

```
INTZRO:      MOV          AL,OF0H          ;IZ selection
              ADD          AN,CNLSEL      ;Select channel
              MOV          DX,SELECT      ;Select output port
              OUT          DX,AL          ;Select Phase III
              MOV          CX,7FFFH       ;Load up CX so the loop will loop
IZLOOP:      IN           AL,DX           ;Get TC500A comparator
              TEST         AI,8           ;Test if bit 3 is 0
              LOOPNZ       IZLOOP         ;Decrease CX, continue if CX > 0 or bit 1 = 3
```

FIGURE 5: Phase III.

## Phase IV — Auto Zero (AZ)

Charges the auto-zero capacitor to the input offset voltage and charges the reference capacitor to the reference voltage.

AL = Select AZ mode (system interrupts may be re-enabled) and channel (output to port)

DX = Port address

Puts the TC500A in auto-zero mode and exits.

```
AUTZRO      MOV          AL,OF2H          ;AZ selection
              ADD          AL,CNLSEL      ;Select output
              MOV          DX,SELECT      ;Select output port
              OUT          DX,AL          ;Select Phase IV
```

The binary-to-ASCII conversion and screen display of the actual program take more than enough time for proper offset correction.

```
CALCXX:      MOV          CX,CXVAL        ;Recall count
              CMP          CX,0           ;Test if count = 0
              JNE          NOTOVF        ;If count not 0, then no over-range
```

Set up over-range message for display:

```
      SETOVF;      MOV          DX,OFFSET OVFMMSG
      MOV          MSGOUT,DX
      JMP          SAVECX
```

Phase II uses CX as a down-counter, so CXVAL is the complement of the true count.

```
NOTOVF:      XOR          CX,OFFFH        ;Complement CXVAL
SAVECX:      MOV          VALUE,CX        ;Save it in VALUE (0 if over-range)
```

FIGURE 6: Phase IV.

(Depend on specific applications)		
CALL	XFORM	;Modify the transform function...
CALL	BIN2BCD	;Convert VALUE to BCD...
CALL	ASCII	;Convert BCD to ASCII characters...
CALL	DISPLAY	;Display the results...
CALL	KEYBRD	;Test if there's input on the keyboard...
JMP	INTGRT	;...and start all over again

**FIGURE 7:** *Optional subroutines.*

The comparator delay factor can be adjusted out with the reference voltage in systems that are designed for fixed resolution. This application has several different levels of resolution and the delay represents a different percentage for each level. CORFAC is selected to have the same percentage relationship to SCALAR as the delay has to the deintegration period.

The SCALAR value is the reference count that determines the resolution of the conversion process. As this value is increased or decreased, more or fewer counts are available during the deintegrate phase. The ratio of the two counts (SCALAR and VALUE) is still directly proportional to the input voltage for any fixed  $V_{REF}$ .

If SCALAR is divided by 2, for example, the input voltage is equal to VALUE times 2. Of course, the significance of the LSB is lost and the resolution is reduced by 1 bit. Divide SCALAR by 4, multiply VALUE by 4 and two LSBs are lost. The advantage is that the conversion time would be four times faster.

A keyboard input routine permits changing the SCALAR value by a multiple of 2 and corrects VALUE by the same amount. No changes to the circuit values are needed because only the reference voltage is part of the conversion equation and its effect has not changed.

## TRANSFER FUNCTION TRANSFORMATION

The program could be expanded to include a routine (or several routines) that would modify or linearize the transfer function(s) per input channel. A simple lookup table or more complex algorithm could be implemented.

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NOTES:



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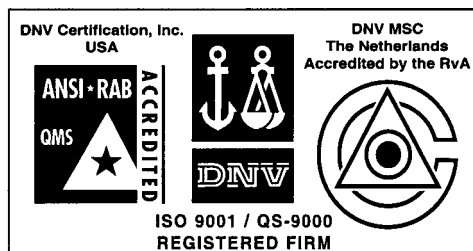
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