AN788

Numerical-Integration Techniques Speed Dual-Slope A/D Conversion

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INTRODUCTION

By using low-cost microprocessors and a program-controlled numerical-integration technique, you can achieve good noise rejection and take full advantage of the higher speeds offered by recently developed dual-slope A/D converters such as the TC7109.

This and similar converters overcome the speed limitations imposed by logic-gate and analog comparator delays in earlier dual-slope devices, and the modern units can operate at rates as high as 30 to 100 samples/sec. Nevertheless, operating them at their maximum conversion rates often makes it difficult or impossible to achieve the high normal-mode line-frequency rejection that dual-slope A/D converters inherently offer at slower conversion rates. Thus, noise considerations have often precluded use of these converters at their rated speeds — especially in industrial environments, where line-frequency and other low-frequency noise components can be a particular problem.

NORMAL-MODE LINE-FREQUENCY REJECTION

To understand normal-mode line-frequency rejection in dual-slope A/D converters, consider a typical 12-bit converter (Figure 1a) and its timing diagram (Figure 1b) for one conversion cycle. Note that the conversion depends on charging the integrating capacitor during a fixed time interval; the number of counts necessary to discharge the capacitor to zero is proportional to the input voltage.

The integrating A/D converter integrates the signal only in a certain time window, as Figure 1b shows. This limited integration period results in normal-mode noise rejection only when the integration period is equal to one or more periods of the noise signal (Figure 2a). The time integral of this noise over integer multiples of the noise period is, of course, zero.

Normal-mode noise-rejection performance can thus be represented as a function (Figure 2b) that reaches peaks at the fundamental and harmonic frequencies of the period defined by the signal-integrate time T. The minimum period T, which must equal the noise period, has been the limiting factor for conversion speed. At 60Hz, for example, the minimum signal-integrate time is 16.7msec; at 50Hz, it's 20msec.

Because the signal-integrate time is only a portion of the total conversion time, conversion rates are significantly less than 1/T. A standard, high-performance, dual-slope A/D converter includes a reference deintegrate phase, typically 2T long, and an autozero period equal to the signal-integrate period T. The total conversion time is thus 4T, which, for 60Hz rejection, yields a maximum conversion rate of 15 samples/sec; for 50Hz, it yields 12.5 samples/sec.

The most serious constraint arises when you want to offer an instrument for international use that can reject both 60 and 50Hz. This feature is attainable only when the signal-integrate period T can contain six cycles of 60Hz noise and five cycles of 50Hz noise. The resulting 100msec signal-integrate period dictates a 2.5 conversion/sec rate.

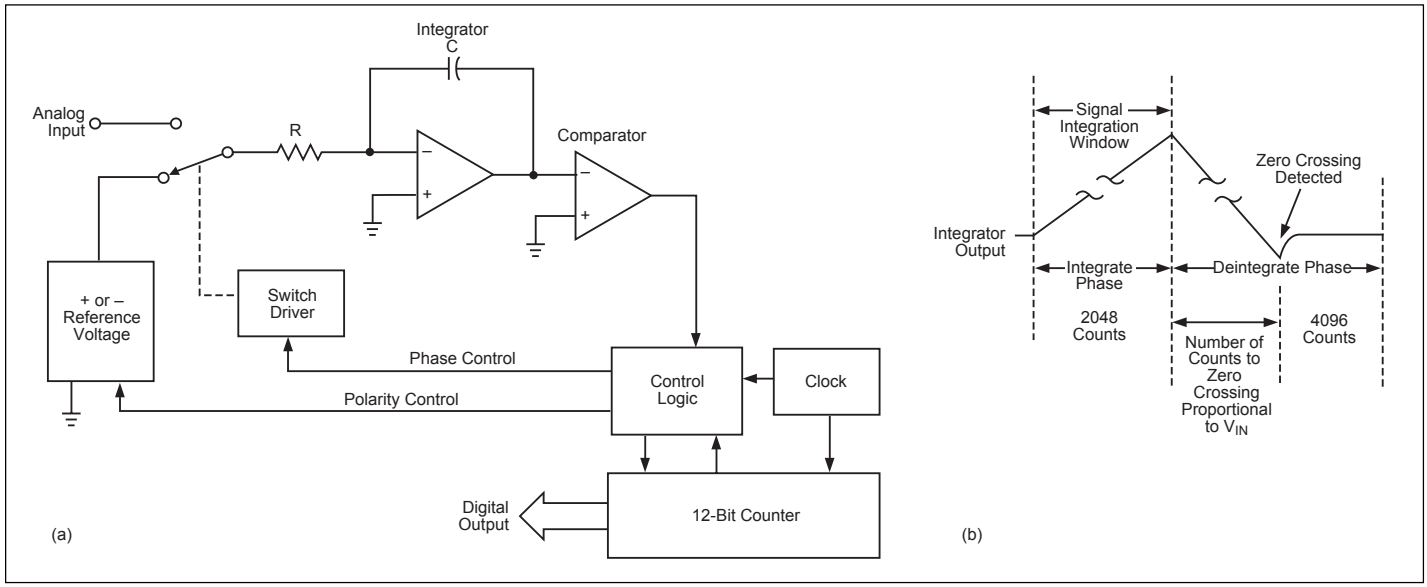


FIGURE 1: A dual-slope A/D converter operates by charging a capacitor from the input voltage during a fixed time, then discharging it to zero. The number of clock periods in the discharge time corresponds to the analog input voltage. The size of the integrating time window determines which normal-mode noise signals are rejected.

You can, however, overcome the inherent conversion-speed limitation of integrating A/D converters. A microprocessor with program-controlled numerical integration that complements the A/D converter's analog integration will speed dual-slope conversion considerably.

You can achieve high normal-mode rejection for specific frequencies with this method if three conditions are met. First, the signal-integrate period must be defined such that noise integration takes place on a segmented basis. In Figure 3a, for example, the integrate window opens on a noise-wave-form segment that's one-third of a period long.

Next, the second signal-integrate period must be at a point corresponding exactly to the point at which the first one ended, and the third's beginning must correspond to the point at which the second ended. This condition can be met only if the A/D converter has a fixed conversion time, irrespective of the signal input. Finally, the microprocessor must sum all three conversions to achieve the total integration of a cycle of noise. A consideration of all these constraints for the TC7109 A/D converter, for example, leads to the relationship:

$$f_{NOISE} = \frac{1}{XT} = \frac{4C}{X}$$

where C is the conversion rate, f the noise frequency and X the number of conversion results added. X must be an odd number; Figure 3b shows why X cannot be an even number. A frequency that would require an even number of samples is one at which the integrate window is locked in phase with the signal (i.e., the converter and signal periods are synchronized). For CV = (f_{NOISE}) (X/4) and X=2 (as in Figure 3b), the result is two times the error of one conversion.

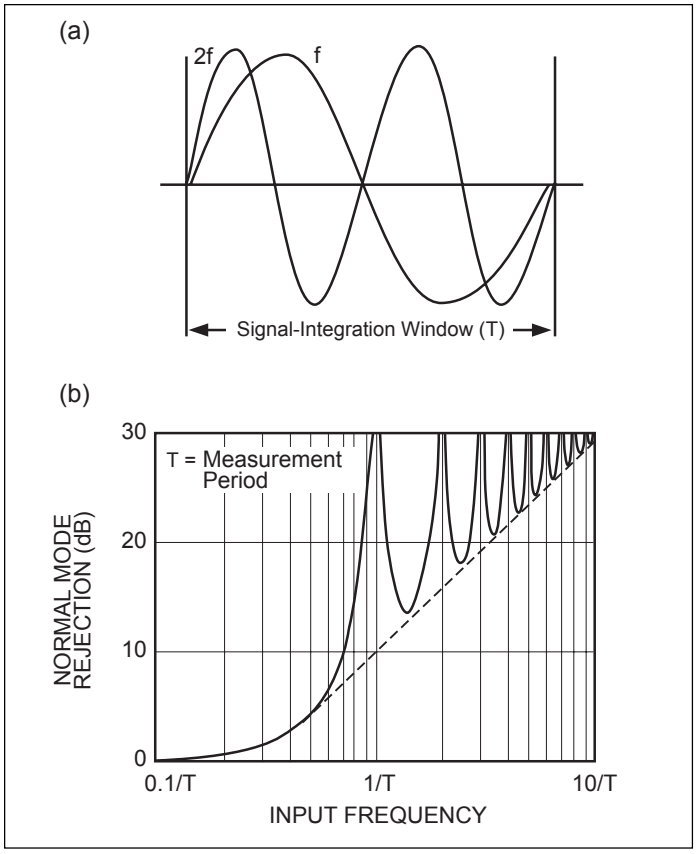


FIGURE 2: In a dual-slope A/D converter, high normal-mode noise rejection occurs when the integration period is a multiple of the noise signal's period.

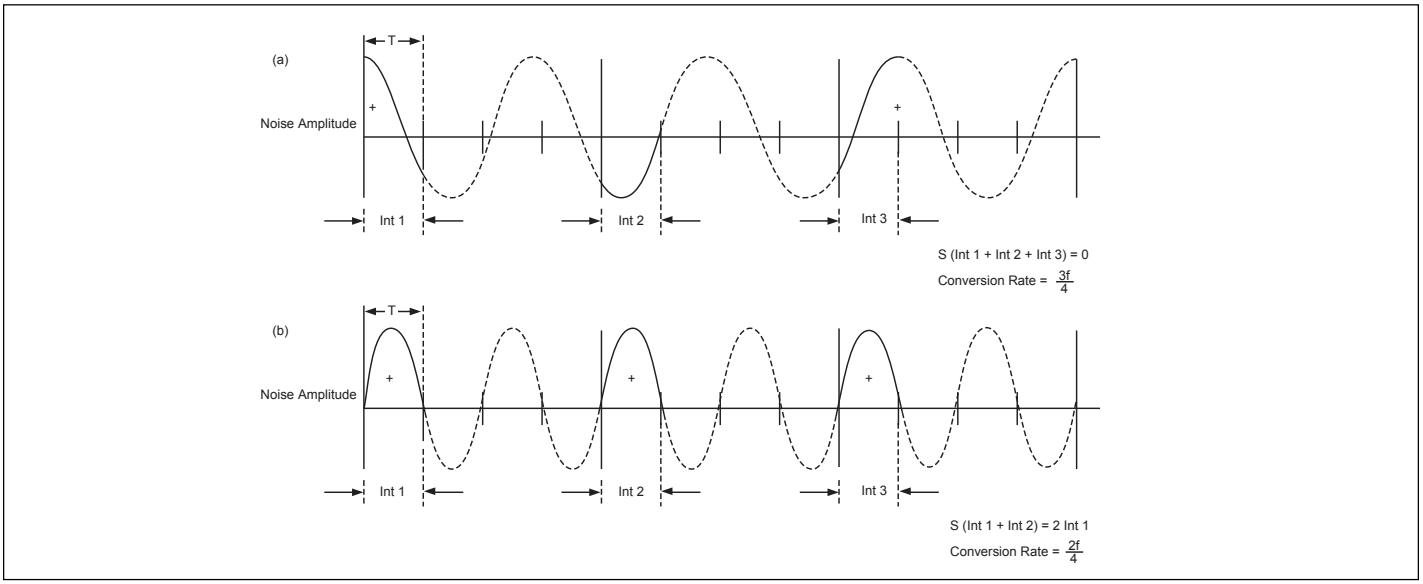


FIGURE 3: Data-conversion systems employing a numerical-integration technique furnish noise rejection when an odd number of samples are summed (a). Adding the results of two conversions, though, can yield twice as much error as does one conversion (b) if the A/D converter and noise frequency are synchronized.

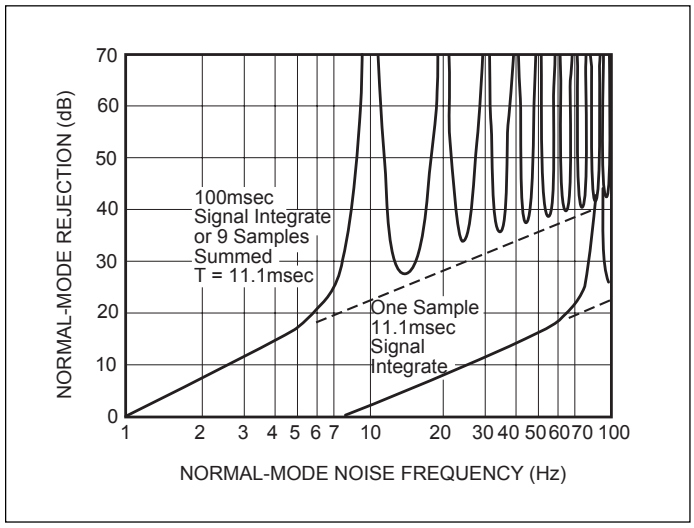


FIGURE 4: The normal-mode-rejection capability illustrated by the upper curve here demonstrates the effectiveness of taking nine conversion samples; the system that the curve represents rejects noise at all multiples of 10Hz. The lower curve shows the result of acquiring only one sample and employing an 11.11msec signal-integration period.

To achieve the desired normal-mode rejection, you must, therefore, sum an odd number of A/D converter results. You can accomplish this summation with firmware or with user-interaction software. Consider an example using a TC7109 A/D converter operating at 22.5 samples/sec. The equation yields the results in Table 1.

As Table 1 indicates, an A/D converter operating at 22.5 samples/sec can reject harmonics of 10Hz if you maintain a rolling average of nine samples. This technique rejects 50 and 60Hz; it's equivalent to one sample taken at the rate of 2.5 samples/sec. The curves in Figure 4 show the normal-mode rejection resulting from 1- and 9-sample averages at the rate of 22.5 conversions/sec (or one sample at 2.5 conversions/sec).

f_{NOISE} (Fundamental) In Hz	X Samples Summed
90	1
30	3
18	5
12.8	7
10	9

TABLE 1: TC67109 at 22.5 sample/sec.

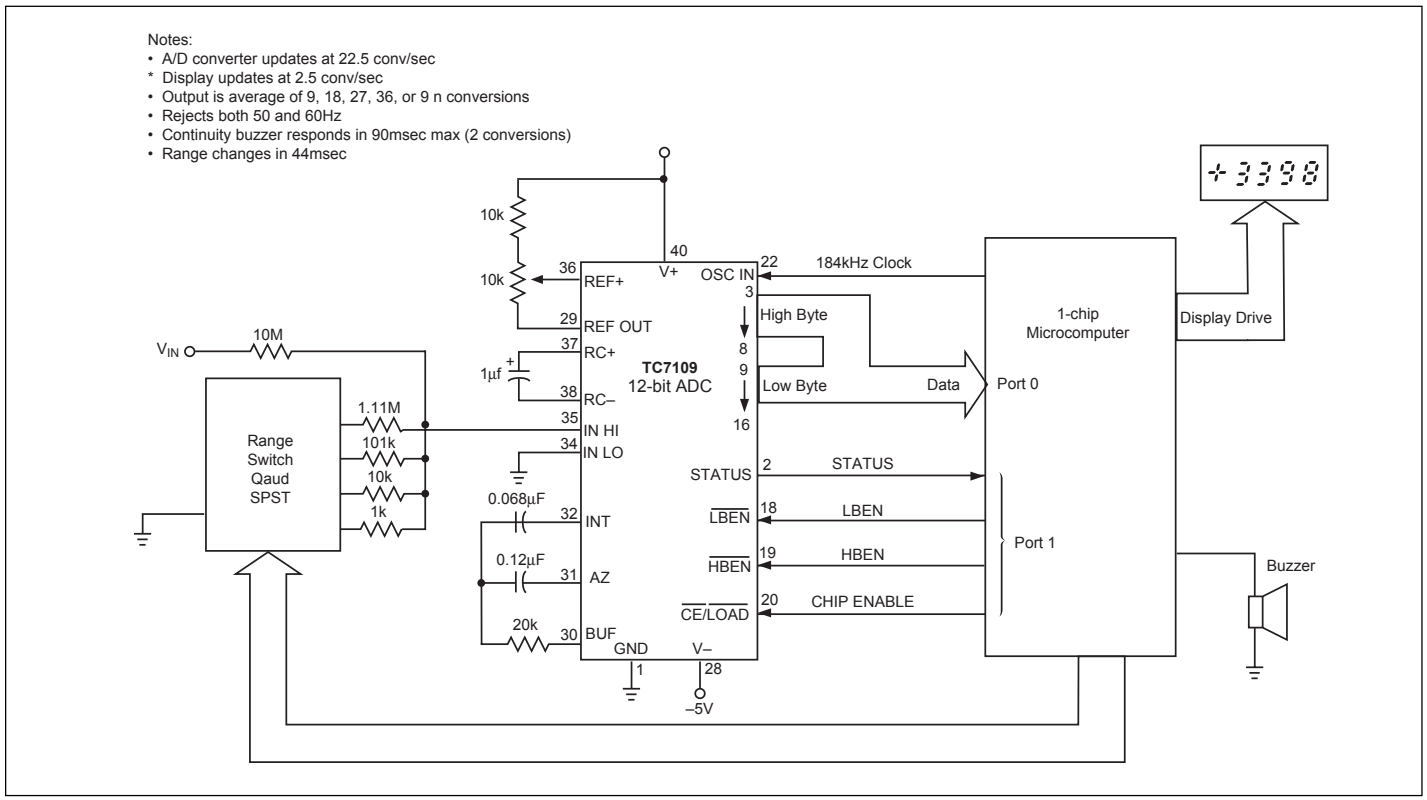


FIGURE 5: This 3 3/4-digit multimeter uses a numerical-integration technique to reject both 50 and 60Hz normal-mode noise. Although the DMM's display updates at 2.5 samples/sec, conversions take place at 22.5 samples/sec.

What's the point, you may ask, of sampling at the higher rate if you must wait for the result during a 9-period numerical integration? After the first 9-period wait, the system's pipeline is full and you may then obtain a new result for each cycle at the 22.5 samples/sec rate.

The numerical-integration technique has many practical applications. The Figure 5 circuit, for example, is a 3 3/4 digit DMM that uses a TC7109 13-bit A/D converter. The DMM updates the display at a 2.5 sample/sec rate for easy readability, yet it converts at a 22.5 samples/sec rate for fast response during autoranging and continuity checking.

Because the circuit averages nine samples, it rejects both 50 and 60Hz noise. Because it can carry a rolling average, the µP is capable of changing the number of conversions summed; it can therefore accommodate specific, user-programmable rejection frequencies.

Figure 6 shows connections for a system using the TC7109 in conjunction with a 6502 processor and 6522 peripheral interface adapter. The adapter's programmable timer provides the A/D converter's clock, thereby simplifying testing of noise rejection with different clock frequencies. This circuit allows you to evaluate numerical-integration-based designs using either a general-purpose µP-development system or a prototyping board. Figure 7 shows the assembly-language listing for the system; the flowchart appears in Figure 8.

X	Channels Scanned
3	13
5	16
7	15
9	10

TABLE 2: 16-channel multiplexer.

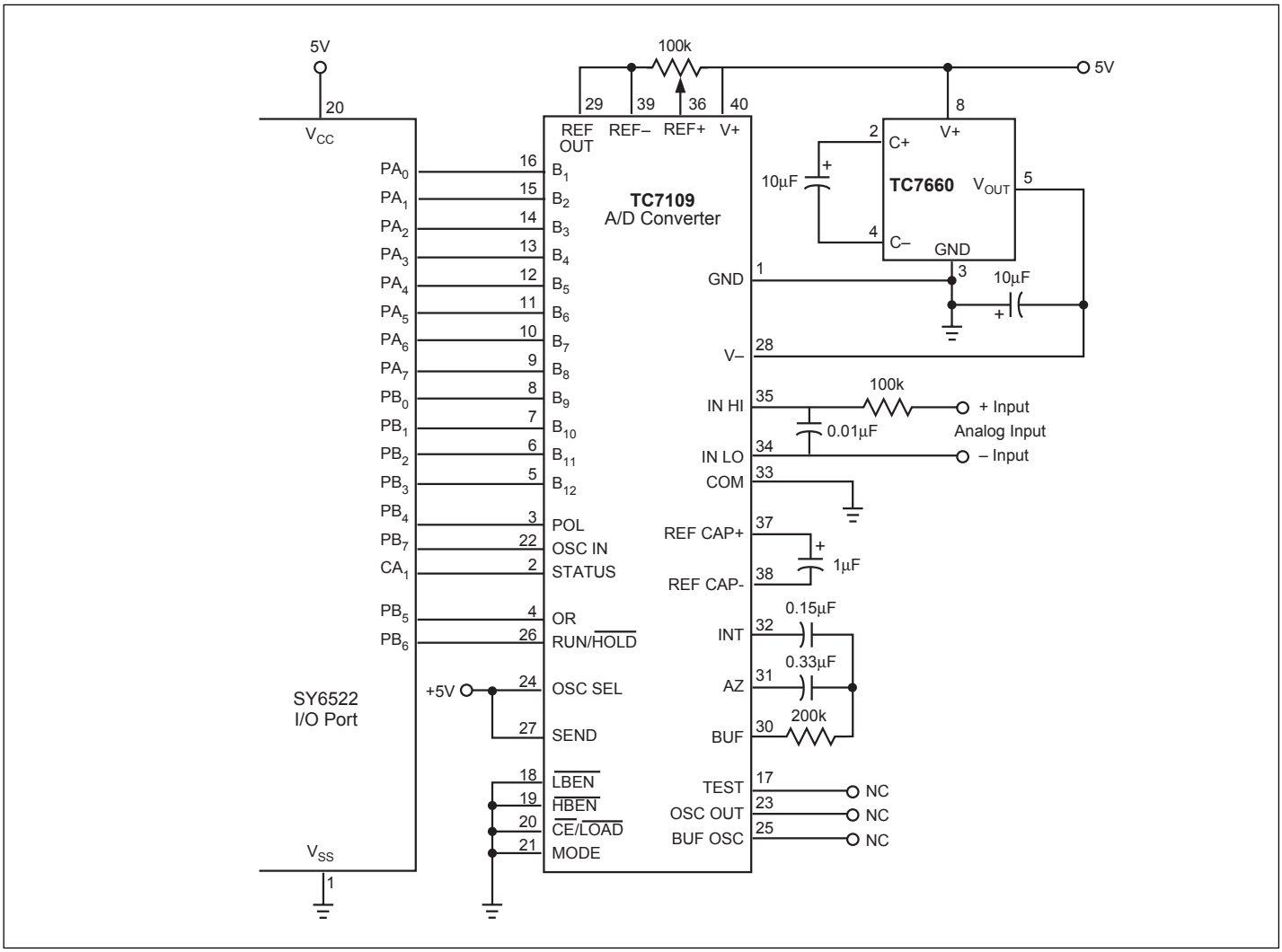


FIGURE 6: You can evaluate numerical integration with the circuit detailed in this schematic. The 6522 peripheral-interface adapted provides clocking and the µP interface for the dual-slope A/D converter.

```
094D.ASM

000D                                ;-----------------------------------------------
000D                                ; SOFTWARE TO DEMONSTRATE NUMERICAL INTEGRATION
000D                                ;    USING THE TC7109 INTERFACED TO A 6502
000D                                ;      MICROPROCESSOR VIA A 6522 I/O PORT
000D                                ; RESULTS STORED AT 'RESLT' IN ZERO-PAGE MEMORY
000D                                ; USER MUST PROVIDE INTERRUPT VECTOR FROM THE
000D                                ;    6522'S CA1 INTERRUPT TO SVC ROUTINE AT "INTSVC"
000D                                ;-----------------------------------------------
000D                                ;SYSTEM EQUATES
A800         10PT    EQU  A800H     ;ADDRESS OF 6522 I/O PORT
0080                 ORG  80H       ;RESERVE ZERO-PAGE MEMORY
0080         RESLT   DS   3         ;16-BIT ACCUMULATOR FOR RESULTS, 1 BYTE FOR SIGN
0083         STORX   DS   1         ;STORAGE FOR LOOP COUNTER
0084         STORHI  DS   1         ;SAVE HIGH BYTE
0280                 ORG  0280H     ;SET UP I/O PORT TO CONTROL TC7109
0280 A9C0    CLOCK   LDA  #0C0H     ;PB6 & PB7 ARE OUTPUTS,
0282 8D00A8          STA  IOPT      ; PB7 IS THE TIMER 1 OUTPUT
0285 8D02A8          STA  IOPT+2    ;    (FOR 7109 CLOCK)
0288 8D0BA8          STA  IOPT+0BH  ;SQUARE WAVE OUTPUT ON PB-7
028B A912            LDA  #12H      ;LOAD THE CONSTANT FOR
028D 8D04A8          STA  IOPT+4    ;    CLOCK TIMER
0290 20FA02          JSR  SETREG    ;ININTIALIZE MEMORY REGISTERS
0293 8D05A8          STA  IOPT+5    ;    START THE 7109 CLOCK
0296 A982            LDA  #82H      ;ENABLE INTERRUPT FROM
0298 8D0EA8          STA  IOPT+0EM  ;    6522 CA1 INPUT
029B 4C2303          JMP  MAINPRG   ;I/O PORT SETUP COMPLET, SO
029E                                ; JUMP TO O.S. OR TO MAIN PROGRAM
029E                                ;INTERRUPT SERVICE ROUTINE
02B0                 ORG  0280H
02B0 AD00A8  INTSVC  LDA  IOPT      ;GET HIGH BYTE
02B3 AA              TAX            ;SAVE IT
02B4 290F            AND  #0FH      ;ZERO MSBs FOR ARITHMATIC
02B6 8584            STA  STORHI    ;SAVE IT
02B8 8A              TXA            ;GET SIGN BIT BACK
02B9 2910            AND  #10H      ;ANALOG INPUT NEGATIVE?
02BB F017            BEQ  SUBTR     ; YES, SO SUBTRACT
02BD 18              CLC            ;RESULT POSITIVE SO ADD
02BE A580            LDA  RESLT     ;GET LS BYTE OF THIS CONVERSION
02C0 6D01A8          ADC  IOPT+1    ; ADD TO PREVIOUS READINGS
02C3 8580            STA  RESLT     ;    SAVE LS BYTE
02C5 A581            LDA  RESLT+1   ;GET MS BYTE OF CONVERSION
02C7 6584            ADC  STORHI    ; ADD TO SUM
02C9 8581            STA  RESLT+1   ;    SAVE MS BYTE
02CB A582            LDA  RESLT+2   ;GET SIGN
02CD 6900            ADC  #00       ; ADD CARRY BIT, IF ANY
02CF 8582            STA  RESLT+    ;    AND SAVE
02D1 4CE802          JMP  LOOPCNT   ;JUMP TO TEST FOR 9 CONVERSIONS
02D4 38      SUBTR   SEC            ;SET CARRY FOR SUBTRACTION
02D5 A580            LDA  RESLT     ; POLARITY OF THIS CONVERSION
02D7 ED01A8          SBC  IOPT+1    ;    IS NEGATIVE, SO DO A
02DA 8580            STA  RESLT     ;       DOUBLE-PRECISION
02DC A581            LDA  RESLT+1   ;          SUBTRACTION
02DE E584            SBC  STORHI    ;
02E0 8581            STA  RESLT+1
02E2 A582            LDA  RESLT+2   ;
02E4 E900            SBC  #00       ;
02E6 8582            STA  RESLT+2   ;
02E8 C683    LOOPCNT DEC  STORX     ;HAVE WE DONE 9 CONVERSIONS?
02EA F001            BEQ  DIVID     ;    YES, SO NOW DIVIDE BY 9
02EC 40              RTI            ;    NO, SO RETURN
02ED                 PAGE
```

FIGURE 7: This assembly-language listing for the µP A/D converter system in Figure 6 provides for 9-sample numerical integration, thereby eliminating normal-mode noise at frequencies that are multiples of 10Hz.

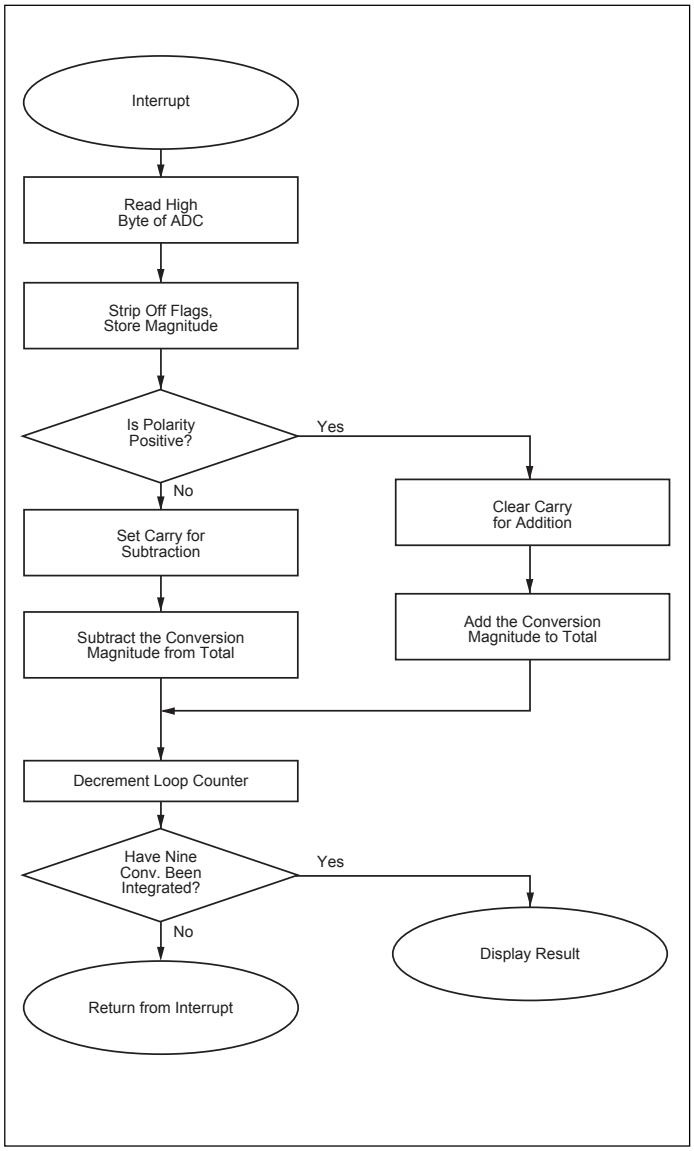


FIGURE 8: This flowchart for Figure 7's assembly-language routine summarizes the code necessary to control the Figure 6 evaluation circuit.

Adding Channels

By using analog multiplexers, you can take advantage of these speed-improvement techniques in multichannel systems. Solving the equation given earlier for X and using X to determine the scan length (or number of channels), you keep the noise-segment alignment in proper phase. This segmented approach (for a 16-channel system that requires the summation of three conversion) is shown in Figure 9. The scan length is found by dividing the number of available channels by X, taking the integer value, and then multiplying it by X and adding 1. Table 2 shows the relationship between the number of samples summed and the number of channels scanned for a 16-channel multiplexer.

A data-acquisition system using a 16-channel multiplexer could use a TC7109 running at 25 conversions/sec to reject all harmonics of 20Hz (including, of course, 60Hz), with a 5-sample average taken in the microprocessor. The system would still respond to large signal deviations in a single conversion.

The change from analog signal integration of noise to hybrid analog/numerical integration entails some trade-offs. The quantization error, for example, is always present; to can lead to a significant reduction in normal-mode rejection if the noise period is carved into too many segments. In addition, timing instability can create other error sources. For maximum stability, you must control the A/D converter's timing with a crystal oscillator.

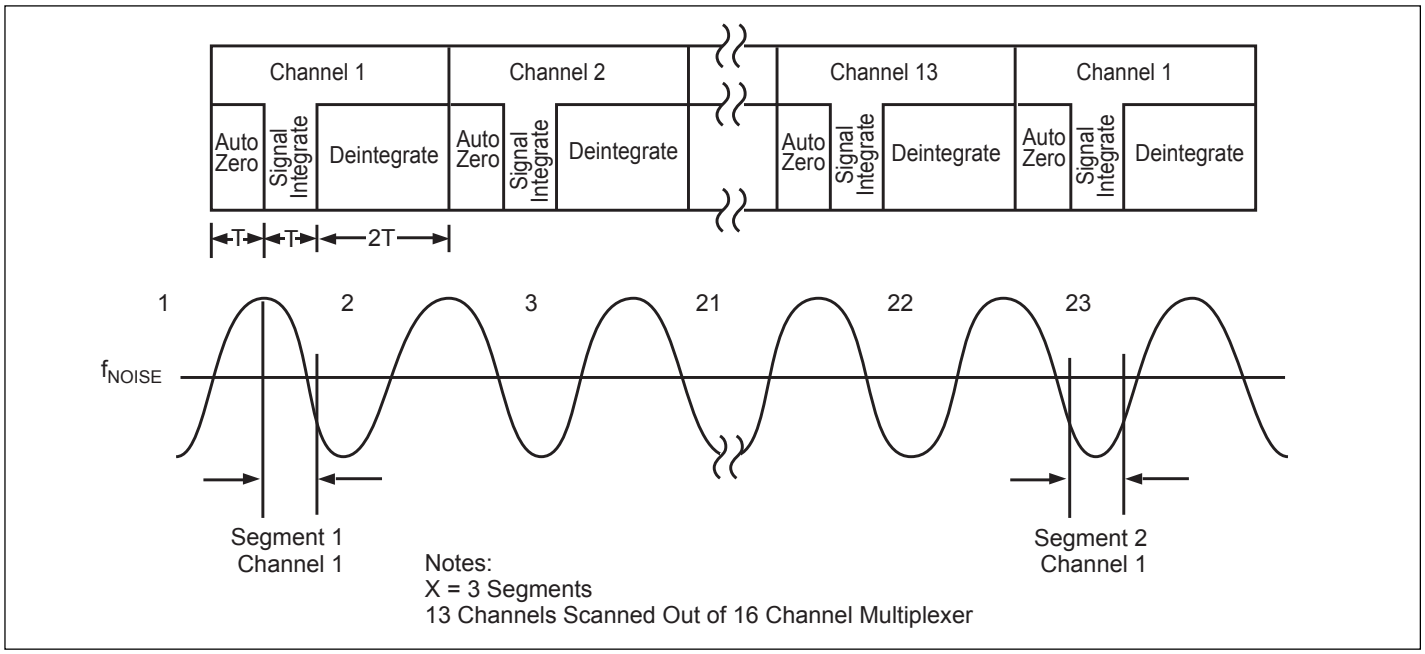
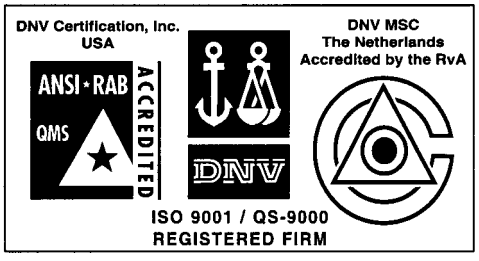


FIGURE 9: You can add multichannel capability to the enhanced-speed A/D-converter designs employing µP-based numerical integration.



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